Ordering number : EN*5402

CMOS LSI

LC82103

Image-Processing LSI for Facsimile, Copier, and OCR Applications

Preliminaly

Overview

The LC82103 converts the analog video signal from the CCD contact image sensor into high-precision binary image data. The LC82103 includes an 8-bit A/D converter and two 6-bit D/A converters. The 6-bit D/A converters are used for setting reference potential (high and low) of the 8-bit A/D converter. The LC82103 converts the input analog data to high precision multilevel data, that is produced by all pixel shading correction process, multi-level image resolution converting process, and γ correction process of user defined curves. That multilevel data is converted to high-precision bi-level image that is produced by using two dimensional filtering, a image separation method, and an error diffusion technique. Finally the LC82103 is able to reduce the image in the horizontal and vertical directions, too. The LC82103 requires absolutely no external memory since it limits the number of pixels processed to 3072/line. This LSI can implement the image processing used by FAX, copier, and OCR applications.

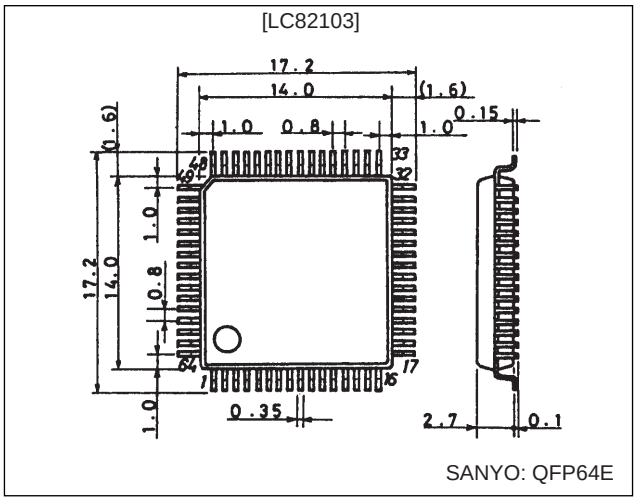
Features

- Number of pixels processed: 3072 pixels/line
- Processing speed: 250 ns/pixel maximum (When CLKIN = 32 MHz)
- Built-in 8-bit A/D converter (with a sensor signal timing adjustment function)
- Built-in two 6-bit D/A converters for setting the A/D converter high and low reference potential
- Sensor drive circuit (supports CCDs and several CIS types)
- Digital clamping (single-point clamping, even/odd clamping)
- Distortion correction (white correction: all pixels, black correction: settable black correction subtracted data)
- γ correction (support user-defined curves: 8-bit data)
- Image area separation (characters, photographs, screened halftone areas)
- Simple binary coding process (fixed threshold, brightness adaptive threshold)
- Intermediate processing error diffusion (64 levels)
- Multilevel image resolution conversion (1/2, 2/3, 3/2, 2/1)
- Binary image reduction (horizontal: thinning, fine black line retaining, fine white line retaining, vertical: thinning, fine black line retaining)
- Single-voltage 5 V supply and low power due to CMOS process fabrication

Package Dimensions

unit: mm

3159-QFP64E



Specifications

Absolute Maximum Ratings at Ta = 25°C, GND = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +7.0	V
Maximum input and output voltages	V_I, V_O max		–0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 70°C	350	mW
Operating temperature	Topr		–30 to +70	°C
Storage temperature	Tstg		–55 to +125	°C
Soldering temperature endurance		Hand soldering: 3 seconds	350	°C
		Reflow soldering: 10 seconds	235	°C

Allowable Operating Ranges at Ta = –30 to +70°C, GND = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		4.5		5.5	V
Input voltage	V_{IN}		0		V_{DD}	V

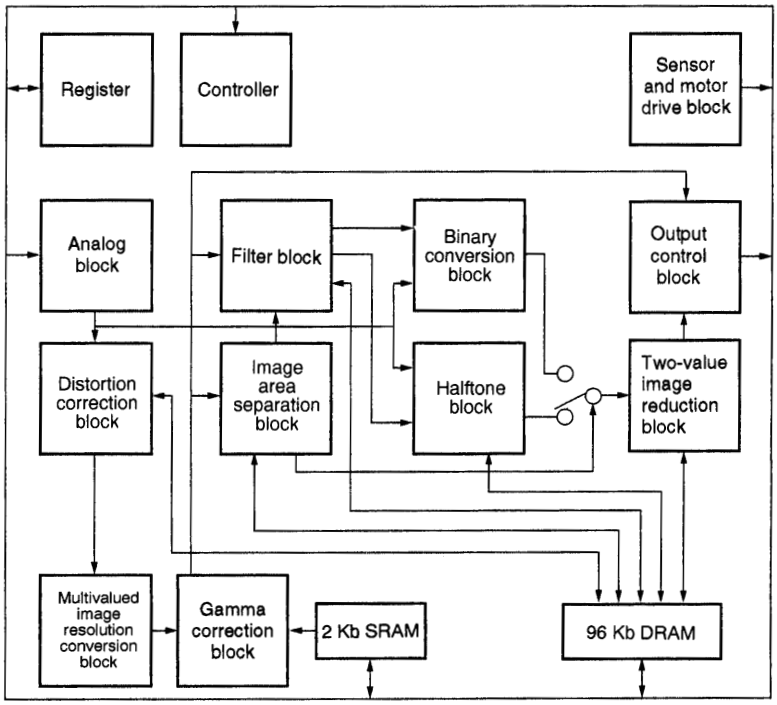
DC Characteristics at Ta = –30 to +70°C, GND = 0 V, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level voltage	V_{IH}		2.2			V
Input low-level voltage	V_{IL}				0.8	V
Input leakage current	$I_{IH, L}$	V_{IN} = V_{DD}, V_{SS}	–10		+10	µA
Output high-level voltage	V_{OH}	I_{OH} = –3 mA	2.4			V
Output low-level voltage	V_{OL}	I_{OL} = 3 mA			0.4	V
Output leakage current	I_{OZ}	At high impedance	–10		+10	µA
Current drain	I_{DD}	CLKIN = 32 MHz		40	70	mA

Analog Characteristics

Parameter	Symbol	Conditions	min	typ	max	Unit
[D/A Converter]						
Resolution				6		bit
Internal resistance				4.8		kΩ
[A/D Converter] When the ATAPL potential = 0.8 V, ATAPH potential = 4.2 V						
Resolution				8		bit
Linearity error					±1	LSB
Differential linearity error					±1	LSB
Internal resistance				330		Ω

Block Diagram



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Pin Functions

Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: No connection

Pin No.	Symbol	I/O	Function
1	D7	B	CPU interface data bus D7 is the MSB, and D0 is the LSB.
2	D6	B	
3	D5	B	
4	D4	B	
5	D3	B	
6	D2	B	
7	D1	B	
8	D0	B	
9	DGND	P	Digital system ground
10	DV_{DD}	P	Digital system power supply
11	A8	I	CPU interface address bus A12 is the MSB, and A0 is the LSB.
12	A7	I	
13	A6	I	
14	A5	I	
15	A4	I	
16	A3	I	
17	DGND	P	Digital system ground
18	A2	I	CPU interface address bus
19	A1	I	
20	A0	I	
21	$\overline{WR}$	I	CPU interface write signal
22	$\overline{RD}$	I	CPU interface read signal
23	A12	I	CPU interface address bus
24	DV_{DD}	P	Digital system power supply
25	CLKIN	I	System clock input
26	A11	I	CPU interface address bus
27	A10	I	
28	A9	I	

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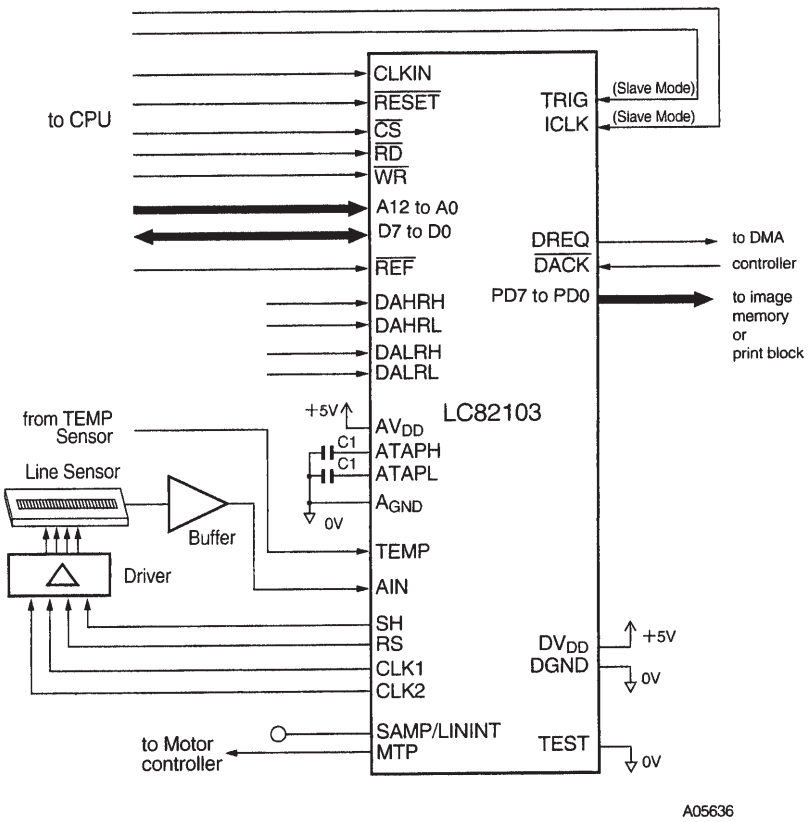
Pin No.	Symbol	I/O	Function
29	$\overline{CS}$	I	CPU interface chip select signal input
30	ICLK	I	External sampling point signal input
31	TRIG	I	External trigger signal input
32	$\overline{RESET}$	I	System reset
33	SAMP/LININT	O	A/D converter sampling point monitor signal output/LINE signal output
34	TEST	I	Test pins (Must be connected to the digital system ground during normal operation.)
35	$\overline{REF}$	I	DRAM refresh signal input
36	AGND	P	Analog system ground
37	DALRL	I	D/A converter low reference input for A/D converter low reference
38	DAHRL	I	D/A converter high reference input for A/D converter high reference
39	AIN	I	Sensor signal input
40	TEMP	I	Temperature signal input
41	ATAPH	O	Analog mid-level signal used as A/D converter high reference
42	DAHRH	I	D/A converter high reference input for A/D converter high reference
43	AV_{DD}	P	Analog system power supply
44	DALRH	I	D/A converter high reference input for A/D converter low reference
45	ATAPL	O	Analog mid-level signal used as A/D converter low reference
46	AGND	P	Analog system ground
47	PD7/SD	O	DMA output/serial data output
48	PD6/SDCK	O	DMA output/serial data transfer clock
49	DGND	P	Digital system ground
50	PD5/SDE	O	DMA output/serial data output valid period indicator
51	PD4/PP4	B	DMA output/general-purpose I/O ports
52	PD3/PP3	B	
53	PD2/PP2	B	
54	PD1/PP1	B	
55	PD0/PP0	B	
56	DV_{DD}	P	Digital system power supply
57	$\overline{DACK}$/PP5	B	DMA data acknowledge signal input/general-purpose I/O port
58	DREQ/PP6	B	DMA data request signal output/general-purpose I/O port
59	MTP/PP7	B	Motor drive timing signal output/general-purpose I/O port
60	CLK2	O	Sensor drive signal outputs
61	CLK1	O	
62	RS	O	
63	SH	O	
64	DGND	P	Digital system ground

Application Example



1. C1 is a 0.01 µF laminated ceramic capacitor
2. The video signal from the image sensor must be set up with a polarity that has white data being the highest potential and black data being the lowest. If the peak level of the video signal from the image sensor does not reach a maximum value of 4.2 V, a level conversion circuit should be inserted to allow the full dynamic range of the A/D converter to be taken advantage of.
3. Although AGND and DGND are fully isolated within the LSI, AV_{DD} and DV_{DD} are connected through the LSI substrate. Accordingly, AV_{DD} and DV_{DD} must be set up so that there is no potential difference between them. Also, the time lag between these signals must be under 3 ms when power is first applied or when power is turned off.