

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

524,288-WORD BY 8-BIT FULL CMOS STATIC RAM

DESCRIPTION

The TC55V040AFT is a 4,194,304-bit static random access memory (SRAM) organized as 524,288 words by 8 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 2.3 to 3.6 V power supply. Advanced circuit technology provides both high speed and low power at an operating current of 3 mA/MHz and a minimum cycle time of 55 ns. It is automatically placed in low-power mode at 0.5 μ A standby current (at $V_{DD} = 3$ V, $T_a = 25^\circ\text{C}$, maximum) when chip enable ($\overline{\text{CE1}}$) is asserted high or (CE2) is asserted low. There are three control inputs. $\overline{\text{CE1}}$ and CE2 are used to select the device and for data retention control, and output enable ($\overline{\text{OE}}$) provides fast memory access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating extreme temperature range of -40° to 85°C , the TC55V040AFT can be used in environments exhibiting extreme temperature conditions. The TC55V040AFT is available in normal and reverse pinout plastic 40-pin thin-small-outline package (TSOP).

FEATURES

- Low-power dissipation
Operating: 10.8 mW/MHz (typical)
- Single power supply voltage of 2.3 to 3.6 V
- Power down features using $\overline{\text{CE1}}$ and CE2
- Data retention supply voltage of 1.5 to 3.6 V
- Direct TTL compatibility for all inputs and outputs
- Wide operating temperature range of -40° to 85°C
- Standby Current (maximum):

3.6 V	7 μ A
3.0 V	5 μ A

- Access Times (maximum):

	TC55V040AFT	
	-55	-70
Access Time	55 ns	70 ns
$\overline{\text{CE1}}$ Access Time	55 ns	70 ns
CE2 Access Time	55 ns	70 ns
$\overline{\text{OE}}$ Access Time	30 ns	35 ns

- Package:

TSOP 40-P-1014-0.50 (AFT) (Weight: 0.32 g typ)

PIN ASSIGNMENT (TOP VIEW)

40 PIN TSOP



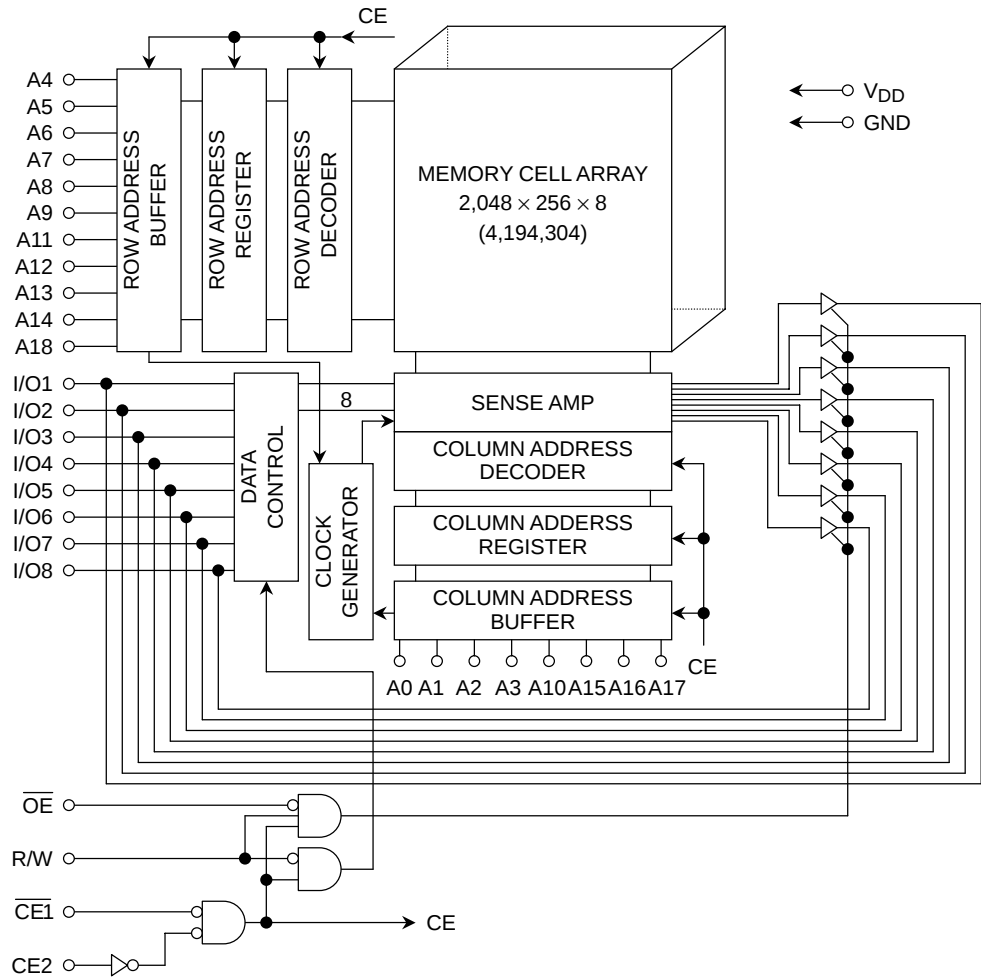
(Normal)

PIN NAMES

A0~A18	Address Inputs
$\overline{\text{CE1}}$, CE2	Chip Enable
R/W	Read/Write Control
$\overline{\text{OE}}$	Output Enable
I/O1~I/O8	Data Inputs/Outputs
V_{DD}	Power
GND	Ground
NC	No Connection

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Pin Name	A16	A15	A14	A13	A12	A11	A9	A8	R/W	CE2	NC	NC	A18	A7	A6	A5	A4	A3	A2	A1
Pin No.	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
Pin Name	A0	$\overline{\text{CE1}}$	GND	$\overline{\text{OE}}$	I/O1	I/O2	I/O3	I/O4	NC	V_{DD}	V_{DD}	I/O5	I/O6	I/O7	I/O8	A10	NC	NC	GND	A17

BLOCK DIAGRAM



OPERATING MODE

MODE	$\overline{\text{CE1}}$	CE2	$\overline{\text{OE}}$	R/W	I/O1-I/O8	POWER
Read	L	H	L	H	Output	I_{DDO}
Write	L	H	*	L	Input	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

* = don't care
H = logic high
L = logic low

MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	-0.3~4.6	V
V_{IN}	Input Voltage	-0.3*~4.6	V
$V_{\text{I/O}}$	Input/Output Voltage	-0.5~ V_{DD} + 0.5	V
P_{D}	Power Dissipation	0.6	W
T_{solder}	Soldering Temperature (10s)	260	°C
T_{stg}	Storage Temperature	-55~150	°C
T_{opr}	Operating Temperature	-40~85	°C

*: -3.0 V when measured at a pulse width of 50ns

DC RECOMMENDED OPERATING CONDITIONS ($T_a = -40^\circ$ to 85°C)

SYMBOL	PARAMETER	2.3 V~3.6 V			UNIT
		MIN	TYP	MAX	
V_{DD}	Power Supply Voltage	2.3	3.0	3.6	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	-0.3*	—	$V_{DD} \times 0.22$	V
V_{DH}	Data Retention Supply Voltage	1.5	—	3.6	V

*: -3.0 V when measured at a pulse width of 50 ns

DC CHARACTERISTICS ($T_a = -40^\circ$ to 85°C , $V_{DD} = 2.3$ to 3.6 V)

SYMBOL	PARAMETER	TEST CONDITION				MIN	TYP	MAX	UNIT
I _{IL}	Input Leakage Current	V _{IN} = 0 V~V _{DD}				—	—	±1.0	μA
I _{OH}	Output High Current	V _{OH} = V _{DD} − 0.5 V				−0.5	—	—	mA
I _{OL}	Output Low Current	V _{OL} = 0.4 V				2.1	—	—	mA
I _{LO}	Output Leakage Current	$\overline{CE1} = V_{IH}$ or CE2 = V _{IL} or R/W = V _{IL} or $\overline{OE} = V_{IH}$, V _{OUT} = 0 V~V _{DD}				—	—	±1.0	μA
I _{DDO1}	Operating Current	$\overline{CE1} = V_{IL}$ and CE2 = V _{IH} and R/W = V _{IH} and I _{OUT} = 0 mA, Other Input = V _{IH} /V _{IL}	V _{DD} = 3 V ± 10%	t _{cycle}	55 ns	—	—	60	mA
					70 ns	—	—	50	
					1 μs	—	—	10	
I _{DDO2}	Operating Current	$\overline{CE1} = 0.2$ V and CE2 = V _{DD} − 0.2 V and R/W = V _{DD} − 0.2 V, I _{OUT} = 0 mA, Other Input = V _{DD} − 0.2 V/0.2 V	V _{DD} = 3 V ± 10%	t _{cycle}	55 ns	—	—	55	mA
					70 ns	—	—	45	
					1 μs	—	—	5	
I _{DDS1}	Standby Current	$\overline{CE} = V_{IH}$ or CE2 = V _{IL}				—	—	2	mA
I _{DDS2} (Note)		$\overline{CE1} = V_{DD} - 0.2$ V or CE2 = 0.2 V V _{DD} = 1.5 V~3.6 V	V _{DD} = 3 V ± 10%	Ta = 25°C	—	—	0.6	μA	
				Ta = −40~85°C	—	—	6		
			V _{DD} = 3.3 V ± 0.3 V	Ta = 25°C	—	—	0.7		
				Ta = −40~85°C	—	—	7		
			V _{DD} = 3.0 V	Ta = 25°C	—	0.05	0.5		
				Ta = −40~40°C	—	—	1		
			Ta = −40~85°C	—	—	5			

Note: In standby mode with $\overline{CE1} \geq V_{DD} - 0.2\text{ V}$, these limits are assured for the condition $CE2 \geq V_{DD} - 0.2\text{ V}$ or $CE2 \leq 0.2\text{ V}$.

CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS AND OPERATING CONDITIONS

 (Ta = -40° to 85°C, V_{DD} = 2.7 to 3.6 V)

READ CYCLE

SYMBOL	PARAMETER	TC55V040AFT				UNIT
		-55		-70		
		MIN	MAX	MIN	MAX	
t _{RC}	Read Cycle Time	55	—	70	—	ns
t _{ACC}	Address Access Time	—	55	—	70	
t _{CO1}	Chip Enable($\overline{\text{CE1}}$) Access Time	—	55	—	70	
t _{CO2}	Chip Enable(CE2) Access Time	—	55	—	70	
t _{OE}	Output Enable Access Time	—	30	—	35	
t _{COE}	Chip Enable Low to Output Active	5	—	5	—	
t _{OOE}	Output Enable Low to Output Active	0	—	0	—	
t _{OD}	Chip Enable High to Output High-Z	—	25	—	30	
t _{ODO}	Output Enable High to Output High-Z	—	25	—	30	
t _{OH}	Output Data Hold Time	10	—	10	—	

WRITE CYCLE

SYMBOL	PARAMETER	TC55V040AFT				UNIT
		-55		-70		
		MIN	MAX	MIN	MAX	
t _{WC}	Write Cycle Time	55	—	70	—	ns
t _{WP}	Write Pulse Width	45	—	50	—	
t _{CW}	Chip Enable to End of Write	50	—	60	—	
t _{AS}	Address Setup Time	0	—	0	—	
t _{WR}	Write Recovery Time	0	—	0	—	
t _{ODW}	R/W Low to Output High-Z	—	25	—	30	
t _{OEW}	R/W High to Output Active	0	—	0	—	
t _{DS}	Data Setup Time	25	—	30	—	
t _{DH}	Data Hold Time	0	—	0	—	

AC TEST CONDITIONS

PARAMETER	TEST CONDITION
Output load	30 pF + 1 TTL Gate
Input pulse level	0.4 V, 2.4 V
Timing measurements	V _{DD} × 0.5
Reference level	V _{DD} × 0.5
t _R , t _F	5 ns

AC CHARACTERISTICS AND OPERATING CONDITIONS

(Ta = -40° to 85°C, V_{DD} = 2.3 to 3.6 V)

READ CYCLE

SYMBOL	PARAMETER	TC55V040AFT				UNIT
		-55		-70		
		MIN	MAX	MIN	MAX	
t _{RC}	Read Cycle Time	70	—	85	—	ns
t _{ACC}	Address Access Time	—	70	—	85	
t _{CO1}	Chip Enable($\overline{\text{CE1}}$) Access Time	—	70	—	85	
t _{CO2}	Chip Enable(CE2) Access Time	—	70	—	85	
t _{OE}	Output Enable Access Time	—	35	—	45	
t _{COE}	Chip Enable Low to Output Active	5	—	5	—	
t _{OOE}	Output Enable Low to Output Active	0	—	0	—	
t _{OD}	Chip Enable High to Output High-Z	—	30	—	35	
t _{ODO}	Output Enable High to Output High-Z	—	30	—	35	
t _{OH}	Output Data Hold Time	10	—	10	—	

WRITE CYCLE

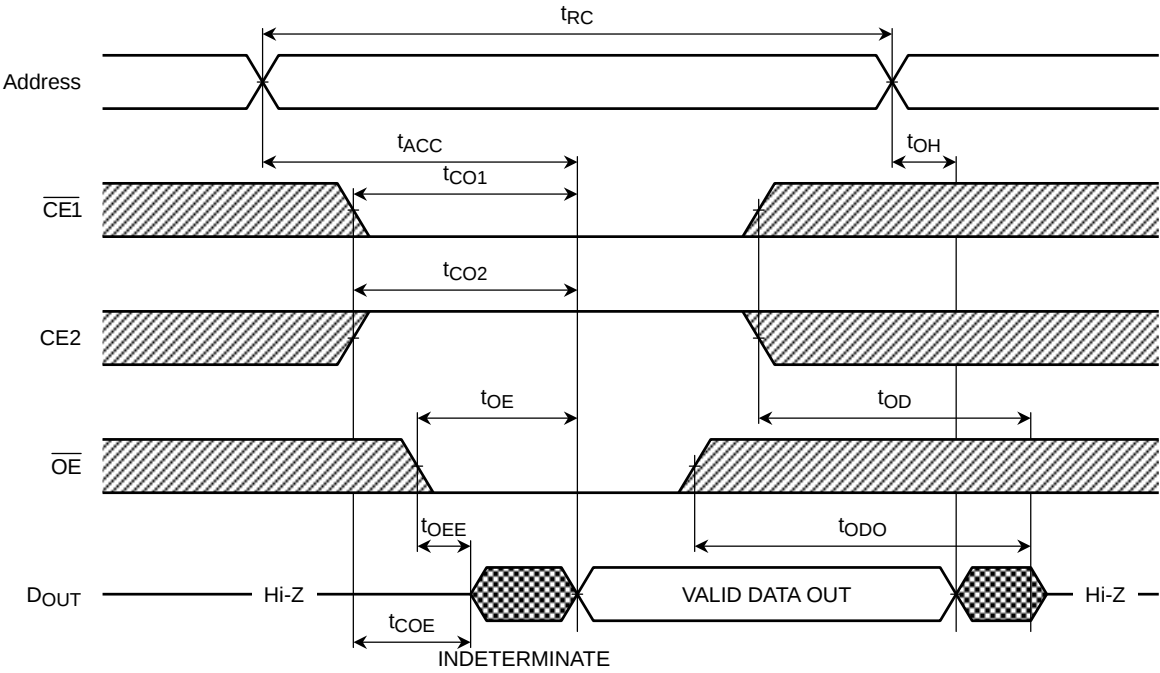
SYMBOL	PARAMETER	TC55V040AFT				UNIT
		-55		-70		
		MIN	MAX	MIN	MAX	
t _{WC}	Write Cycle Time	70	—	85	—	ns
t _{WP}	Write Pulse Width	50	—	55	—	
t _{CW}	Chip Enable to End of Write	60	—	70	—	
t _{AS}	Address Setup Time	0	—	0	—	
t _{WR}	Write Recovery Time	0	—	0	—	
t _{ODW}	R/W Low to Output High-Z	—	30	—	35	
t _{OEW}	R/W High to Output Active	0	—	0	—	
t _{DS}	Data Setup Time	30	—	35	—	
t _{DH}	Data Hold Time	0	—	0	—	

AC TEST CONDITIONS

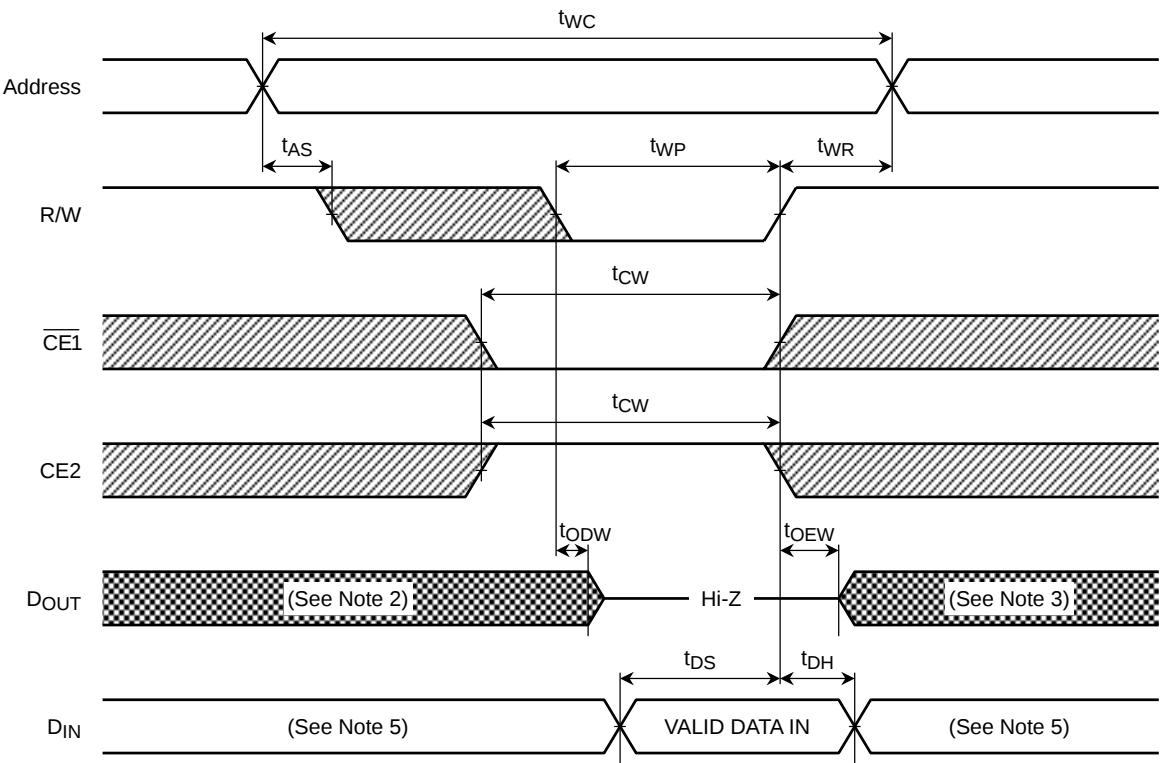
PARAMETER	TEST CONDITION
Output load	30 pF + 1 TTL Gate
Input pulse level	V _{DD} - 0.2 V, 0.2 V
Timing measurements	V _{DD} × 0.5
Reference level	V _{DD} × 0.5
t _R , t _F	5 ns

TIMING DIAGRAMS

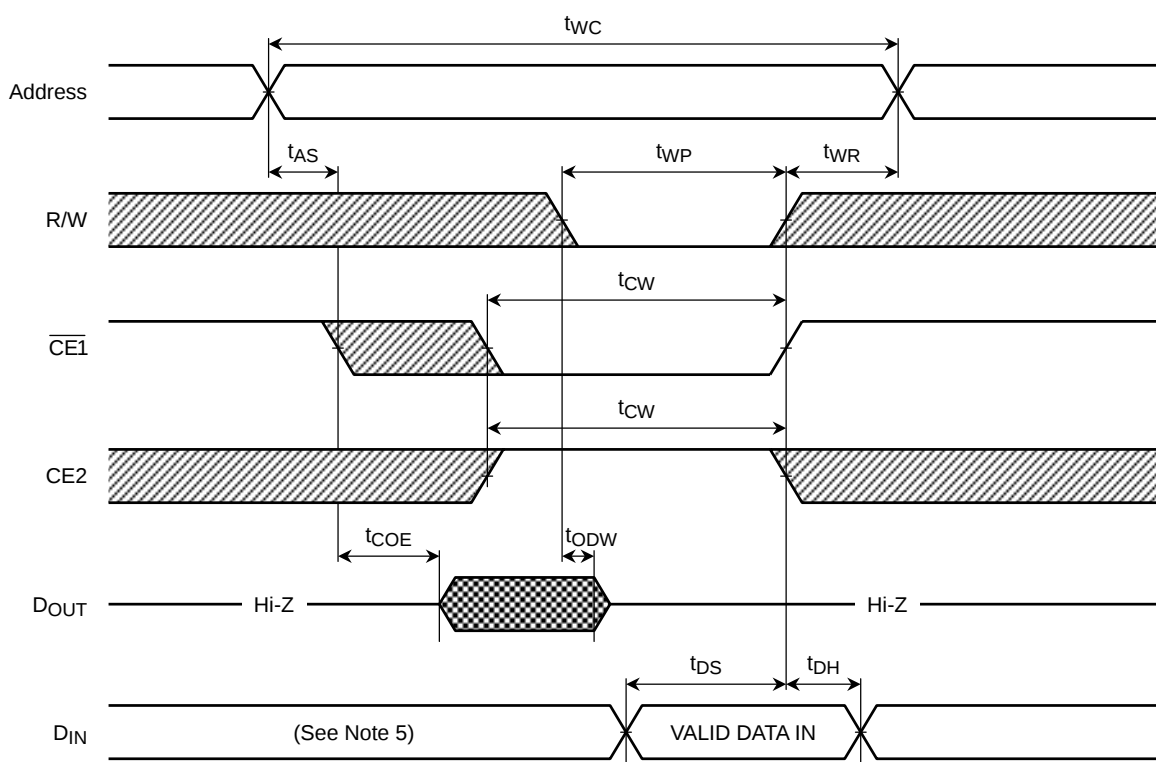
READ CYCLE (See Note 1)



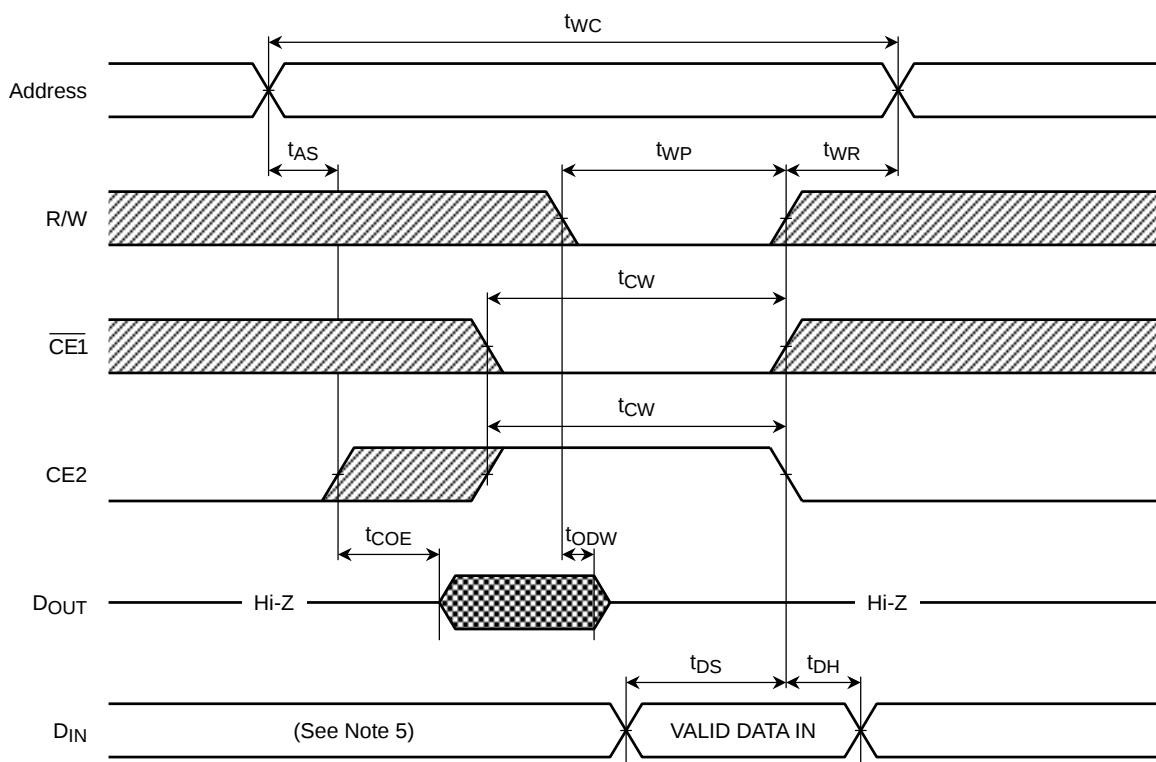
WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)



WRITE CYCLE 2 ($\overline{\text{CE1}}$ CONTROLLED) (See Note 4)



WRITE CYCLE 3 (CE2 CONTROLLED) (See Note 4)



Note:

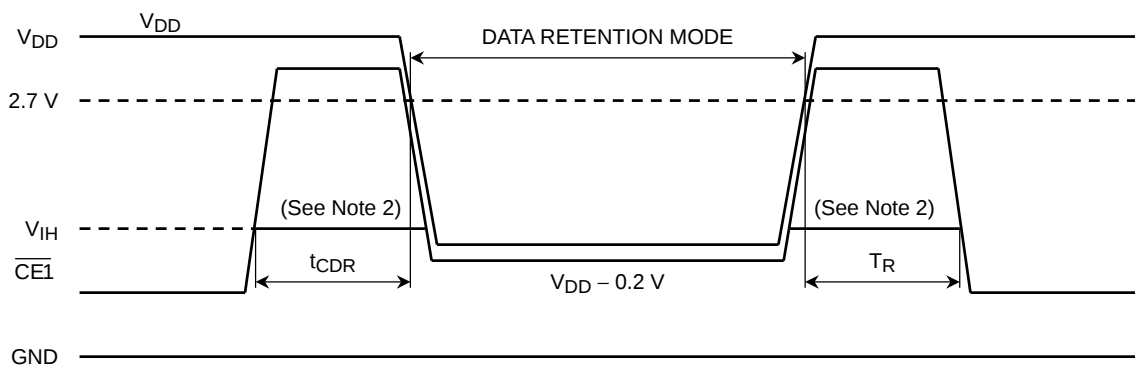
- (1) R/W remains HIGH for the read cycle.
- (2) If $\overline{\text{CE1}}$ goes LOW(or CE2 goes HIGH) coincident with or after R/W goes LOW, the outputs will remain at high impedance.
- (3) If $\overline{\text{CE1}}$ goes HIGH(or CE2 goes LOW) coincident with or before R/W goes HIGH, the outputs will remain at high impedance.
- (4) If $\overline{\text{OE}}$ is HIGH during the write cycle, the outputs will remain at high impedance.
- (5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

DATA RETENTION CHARACTERISTICS (Ta = -40° to 85°C)

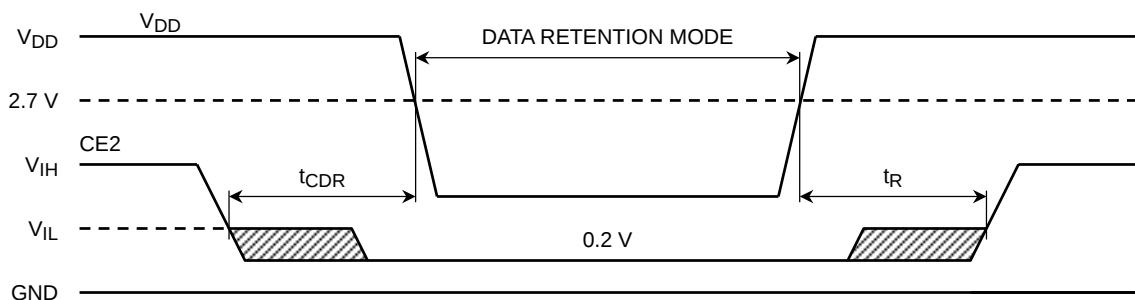
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V _{DH}	Data Retention Supply Voltage		1.5	—	3.6	V
I _{DDS2}	Standby Current	V _{DH} = 3.0 V	Ta = -40~40°C	—	1	μA
			Ta = -40~85°C	—	5	
		V _{DH} = 3.6 V	Ta = -40~85°C	—	7	
t _{CDR}	Chip Deselect to Data Retention Mode Time		0	—	—	ns
t _R	Recovery Time		t _{RC} (See Note)	—	—	ns

Note: Read cycle time

CE1 CONTROLLED DATA RETENTION MODE (See Note 1)



CE2 CONTROLLED DATA RETENTION MODE (See Note 3)



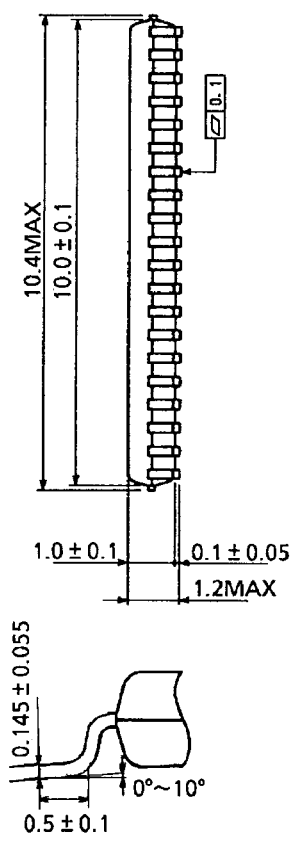
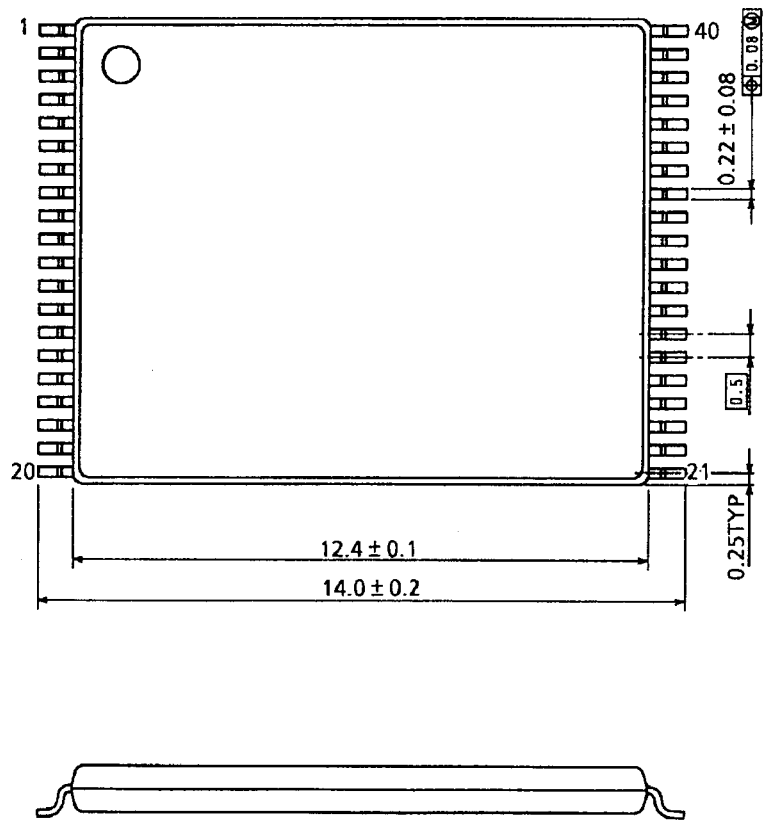
Note:

- (1) In $\overline{\text{CE1}}$ controlled data retention mode, minimum standby current mode is entered when $\text{CE2} \leq 0.2 \text{ V}$ or $\text{CE2} \geq \text{V}_{\text{DD}} - 0.2 \text{ V}$.
- (2) When $\overline{\text{CE1}}$ is operating at the V_{IH} level (2.2V), the operating current is given by I_{DDS1} during the transition of V_{DD} from 3.6 to 2.4V.
- (3) In CE2 controlled data retention mode, minimum standby current mode is entered when $\text{CE2} \leq 0.2 \text{ V}$.

PACKAGE DIMENSIONS

TSOP I 40-P-1014-0.50

Unit : mm



Weight: 0.32 g (typ)

RESTRICTIONS ON PRODUCT USE

030619EBA

- The information contained herein is subject to change without notice.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA for any infringements of patents or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of TOSHIBA or others.
- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc..
- The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury ("Unintended Usage"). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of TOSHIBA products listed in this document shall be made at the customer's own risk.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
- TOSHIBA products should not be embedded to the downstream products which are prohibited to be produced and sold, under any law and regulations.