TOSHIBA

INTEGRATED CIRCUIT

TECHNICAL DATA

TOSHIBA MOS INTEGRATED CIRCUIT

TC58F1001P/F-15 , TC58F1001P/F-20

SILICON STACKED GATE MOS

TENTATIVE DATA

TC58F1001P/F 131,072WORD × 8BIT CMOS FLASH E^2 PROM

DESCRIPTION

The TC58F1001P/F is a 1,048,576 bits, Flash Electrically Erasable and Programmable Read Only Memory (FE^2PROM) organized as 131,072 words by 8 bits. The TC58F1001P/F is fabricated by using advanced CMOS technology which provides the high speed and low power features with access times of 150ns/200ns, an operating current of 30mA at 6.7 MHz and a standby current of 100μA.

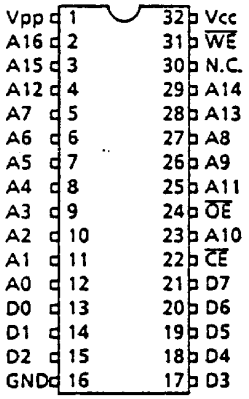
The TC58F1001P/F features a command control mode and an EPROM compatible mode for programming and erasing. The command control mode is used for in-system programming controlled by the MPU timing. A specific software sequence must be executed to enable the program, program-verify, chip-erase, block-erase, erase-verify, signature-read and mode reset operations. The EPROM compatible mode is used for programming and erasing with a conventional EPROM programmer. The programming time is 14-seconds and the erasing time is only 1-second. The TC58F1001P/F is also provided with a block-erase feature. The programming time of 1 block (4K byte) is only 0.5-second.

The TC58F1001P/F has a JEDEC standard pinout configuration and is packaged in either a 32-pin plastic DIP, 32-pin flat package (SOP).

FEATURES

- Access time : 150ns/200ns
- Power dissipation
  - Operating : 30mA
  - Standby : 100μA
- Erase/Write endurance
  - 100 cycles
  - 10,000 cycles (Option)
- High-speed programming
  - 14 second/chip
  - 0.5 second/block
- Electrically erasing mode
  - Chip erase 1 second
  - Block erase 1 second
  - (Block size : 4K Byte × 32 blocks)
- Package type
  - TC58F1001P : DIP32-P-600
  - TC58F1001F : SOP32-P-525
- Program/Erase mode
  - Command control mode
  - EPROM compatible mode

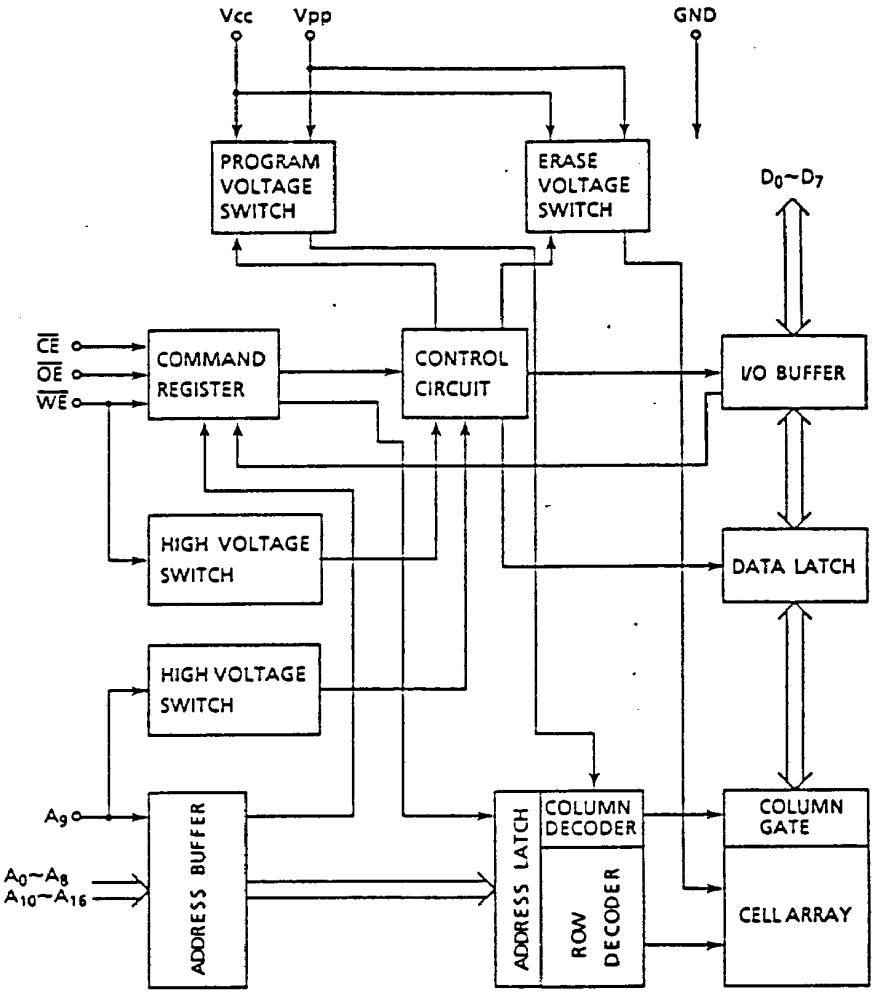
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~16	Address input
D0~7	Data input/output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable/EPROM mode switch
N.C.	No connection
V_{PP}	Program and Erase Power Supply
V_{CC}	Power Supply
GND	Ground

BLOCK DIAGRAM



OPERATING MODE

<Command Control Mode>

① $\overline{WE}$ Control

MODE		$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	D0~7	Power
Read	Read	H	L	L	0V~V_{CC} or 12V	5V	Data Output	Active
	Output Deselect	*	*	H			High-Z	
	Standby	*	H	*				Standby
Command Input		⊓	L	H	12V	5V	Data Input	Active
Program or Erase		H	*	*			**	
Program Verify or Erase Verify		H	L	L			Data Output	
Signature Read		H	L	L			Code Output	

Note : *: V_{IH} or V_{IL}, H: V_{IH}, L: V_{IL}
**: Depend on $\overline{CE}$, $\overline{OE}$

② $\overline{CE}$ Control

MODE		$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	D0~7	Power
Read	Read	H	L	L	0V~V_{CC} or 12V	5V	Data Output	Active
	Output Deselect	*	*	H			High-Z	
	Standby	*	H	*				Standby
Command Input		L	⊓	H	12V	5V	Data Input	Active
Program or Erase		*	H	*			**	
Program Verify or Erase Verify		H	L	L			Data Output	
Signature Read		H	L	L			Code Output	

Note : *: V_{IH} or V_{IL}, H : V_{IH}, L : V_{IL}
**: Depend on $\overline{OE}$, $\overline{WE}$

<EPROM Compatible Mode>

MODE		A9	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	D0~7	Power
Read	Read	*	H	L	L	0V~V_{CC}	5V	Data Output	Active
	Output Deselect	*	*	*	H			High-Z	
	Standby	*	*	H	*				Standby
Program	Program	*	V_{WE}	L	H	12V	5V	Data Input	Active
	Program Inhibit	*	V_{WE}	H	*			High-Z	
	Program Verify	*	V_{WE}	*	L			Data Output	
Erase (Chip Erase)	Erase	V_{ID}	V_{WE}	L	H	12V	5V	**	Active
	Erase inhibit	V_{ID}	V_{WE}	H	*			High-Z	
Signature Read		V_{ID}	H	L	L	0V~V_{CC}	5V	Code Output	Active

Note : *: V_{IH} or V_{IL}, H: V_{IH}, L: V_{IL}
**: Data Input or High-Z
V_{ID}, V_{WE}=12V

MAXIMUM RATING

SYMBOL	CHARACTERISTIC	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program/Erase Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
$V_{I/O}$	Input/Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.0*1)/0.6*2)	W
T_{SOLDER}	Soldering Temperature·Time	260·10	°C·sec
T_{STG}	Storage Temperature	−55~150	°C
T_{OPR}	Operating Temperature	0~70	°C
N_{EW}	Erase Write Endurance	100/10000**	Cycle
V_{ID}/V_{WE}	Input Voltage (A9/$\overline{WE}$)	−0.6~13.5	V

Note : *1) Plastic DIP, *2) Plastic SOP

** 10000 cycle part is optionally screened

CAPACITANCE* (Ta = 25°C, f = 1MHz)

SYMBOL	CHARACTERISTIC	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	−	4	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	−	10	12	

* This parameter is periodically sampled, and is not 100% tested.

D.C. RECOMMENDED OPERATING CONDITION (Ta = 0~70°C)

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNIT
V_{CC}	Vcc Power Supply Voltage	4.5	5.5	V
V_{IH}	Input high Voltage	2.2	V_{CC} + 0.3	
V_{IL}	Input Low Voltage	−0.3	0.8	
V_{ID}	A9 Pin Identifier Mode Voltage	11.4	12.6	
V_{WE}	WE Pin EPROM Compatible Mode Switch Voltage	11.4	12.6	
V_{PP}	V_{PP} Power Supply Voltage (Low Voltage)	0	V_{CC} + 0.6	
	V_{PP} Power Supply Voltage (High Voltage)	11.4	12.6	

D.C. AND OPERATING CHARACTERISTICS (Ta=0~70°C, VCC=5.0V±10%)

SYMBOL	CHARACTERISTIC	TEST CONDITION	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$	-	±10	μA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$	-	±10	
V_{OH}	Output High Voltage	$I_{OH} = -0.400mA$	2.4	-	V
V_{OL}	Output Low Voltage	$I_{OL} = +2.10mA$	-	0.4	
I_{CC1}	V_{CC} Supply Current (Read / Verify / Signature Read Operation)	$V_{IN} = V_{IH} / V_{IL}$, $I_{OUT} = 0mA$, $t_{cycle} = 150ns$	-	30	mA
I_{CC2}	V_{CC} Supply Current (Program / Erase Operation)	$V_{IN} = V_{IH} / V_{IL}$, $I_{OUT} = 0mA$, $t_{cycle} = 90\mu s / 0.9S$	-	30	
I_{CCS1}	V_{CC} Standby Current (Read Operation)	$\overline{CE} = V_{IH}$	-	1	mA
I_{CCS2}		$\overline{CE} = V_{CC} - 0.20V$	-	100	μA
I_{PP}	V_{PP} Supply Current	$0V \leq V_{PP} \leq V_{CC} + 0.6V$	-	±10	μA
		$11.4V \leq V_{PP} \leq 12.6V$	-	200	
I_{PP1}	V_{PP} Operating Current (Each Operation except for Program & Erase)	$0V \leq V_{PP} \leq V_{CC} + 0.6V$, $V_{IN} = V_{IH} / V_{IL}$	-	±10	μA
		$11.4V \leq V_{PP} \leq 12.6V$, $V_{IN} = V_{IH} / V_{IL}$	-	200	
I_{PP2}	V_{PP} Program Current	$11.4V \leq V_{PP} \leq 12.6V$, $V_{IN} = V_{IH} / V_{IL}$	-	50	mA
I_{PP3}	V_{PP} Erase Current	$11.4V \leq V_{PP} \leq 12.6V$, $V_{IN} = V_{IH} / V_{IL}$	-	30	mA
I_{ID}	A9 Pin Identifier Mode Current	$11.4V \leq V_{ID} \leq 12.6V$	-	200	μA
I_{WE}	$\overline{WE}$ Pin EPROM Compatible Mode Switch Current	$11.4V \leq V_{WE} \leq 12.6V$	-	200	

A.C. CHARACTERISTICS

1. READ OPERATION (Ta = 0~70°C, V_{CC} = 5.0V ± 10%, V_{PP} = 0V~V_{CC} or 12.0V ± 5%)

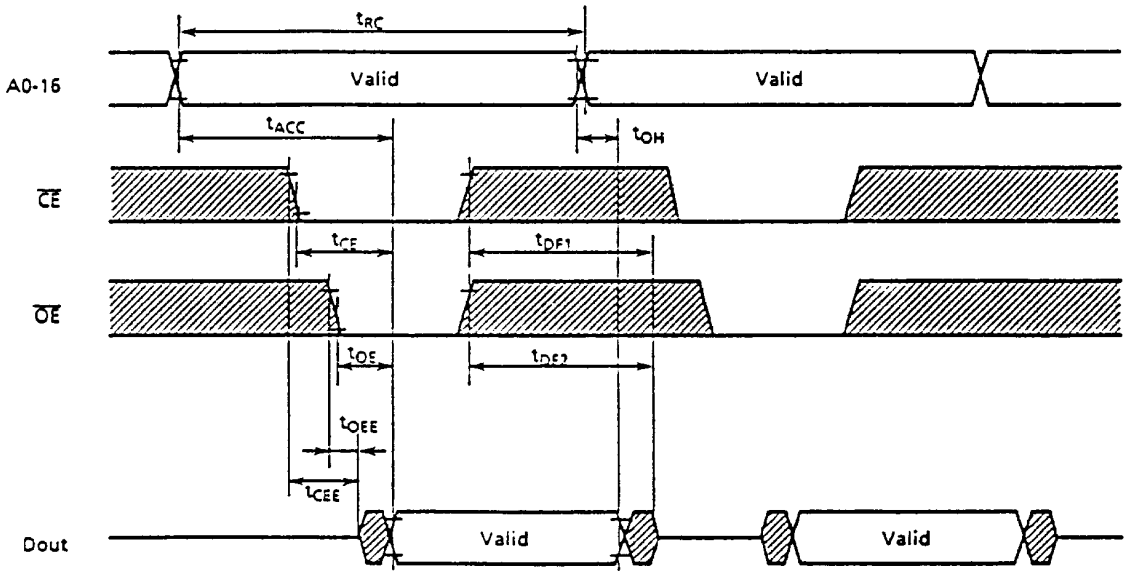
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT
t_{RC}	Read Cycle Time	150/200*	-	-	ns
t_{ACC}	Address Access Time	-	-	150/200*	
t_{CE}	Chip Enable Access Time	-	-	150/200*	
t_{OE}	Output Enable Access Time	-	-	70	
t_{CEE}	Chip Enable to Output in Low-Z	0	-	-	
t_{OEE}	Output Enable to Output in Low-Z	0	-	-	
t_{OH}	Output Data Hold Time	0	-	-	
t_{DF1}	Chip Enable to Output in High-Z	-	-	60	
t_{DF2}	Output Enable to Output in High-Z	-	-	60	

Note : * 150ns for TC58F1000P/F-15
200ns for TC58F1000P/F-20

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Time (10%~90%) : 5ns
- Input Pulse Level : 0.45V to 2.40V
- Timing Measurement Reference Level Input : 0.80V/2.20V
  Output : 0.80V/2.00V

Timing Waveform of Read Cycle



2. COMMAND CONTROL OPERATION (Ta=0~70°C, V_{CC}=5.0V±10%, V_{PP}=12.0V±5%)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT
t_{AS}	Address Setup time	0	–	–	ns
t_{AH}	Address Hold time	60	–	–	
t_{CES}	Chip Enable Setup time ($\overline{WE}$ Control)	0	–	–	
t_{CEH}	Chip Enable Hold time ($\overline{WE}$ Control)	10	–	–	
t_{OES}	Output Enable Setup time	0	–	–	
t_{OEH}	Output Enable Hold time	10	–	–	
t_{WES}	Write Enable Setup time ($\overline{CE}$ Control)	0	–	–	
t_{WEH}	Write Enable Hold time ($\overline{CE}$ Control)	10	–	–	
t_{DS}	Data Setup time	50	–	–	
t_{DH}	Data Hold time	0	–	–	
t_{WELH}	Write Enable Low Level Hold time	~~60~~ 70	–	–	
t_{WEHH}	Write Enable High Level Hold time	20	–	–	
t_{CELH}	Chip Enable Low Level Hold time	~~70~~ 80	–	–	
t_{CEHH}	Chip Enable High Level Hold time	20	–	–	
t_{CMC}	Command Cycle time	150	–	–	
t_{PH}	Programming Hold time	90	100	110	µs
t_{PRV}	Program Recovery time before Program Verify	2	–	–	
t_{EH}	Erasing Hold time	0.9	1.0	1.1	s
t_{ERV}	Erase Recovery time before Erase Verify	500	–	–	µs
t_{ACC}	Address Access time	–	–	150/200*	ns
t_{CE}	Chip Enable Access time	–	–	150/200*	
t_{OE}	Output Enable Access time	–	–	70	
t_{CEE}	Chip Enable to Output in Low-Z	0	–	–	
t_{OEE}	Output Enable to Output in Low-Z	0	–	–	
t_{OH}	Output Data Hold time	0	–	–	
t_{DF1}	Chip Enable to Output in High-Z	–	–	60	
t_{DF2}	Output Enable to Output in High-Z	–	–	60	
t_{VC}	Verify Cycle time	150/200*	–	–	
t_{RC}	Read Cycle time	150/200*	–	–	

Note : * 150ns for TC58F1001P/F-15
200ns for TC58F1001P/F-20

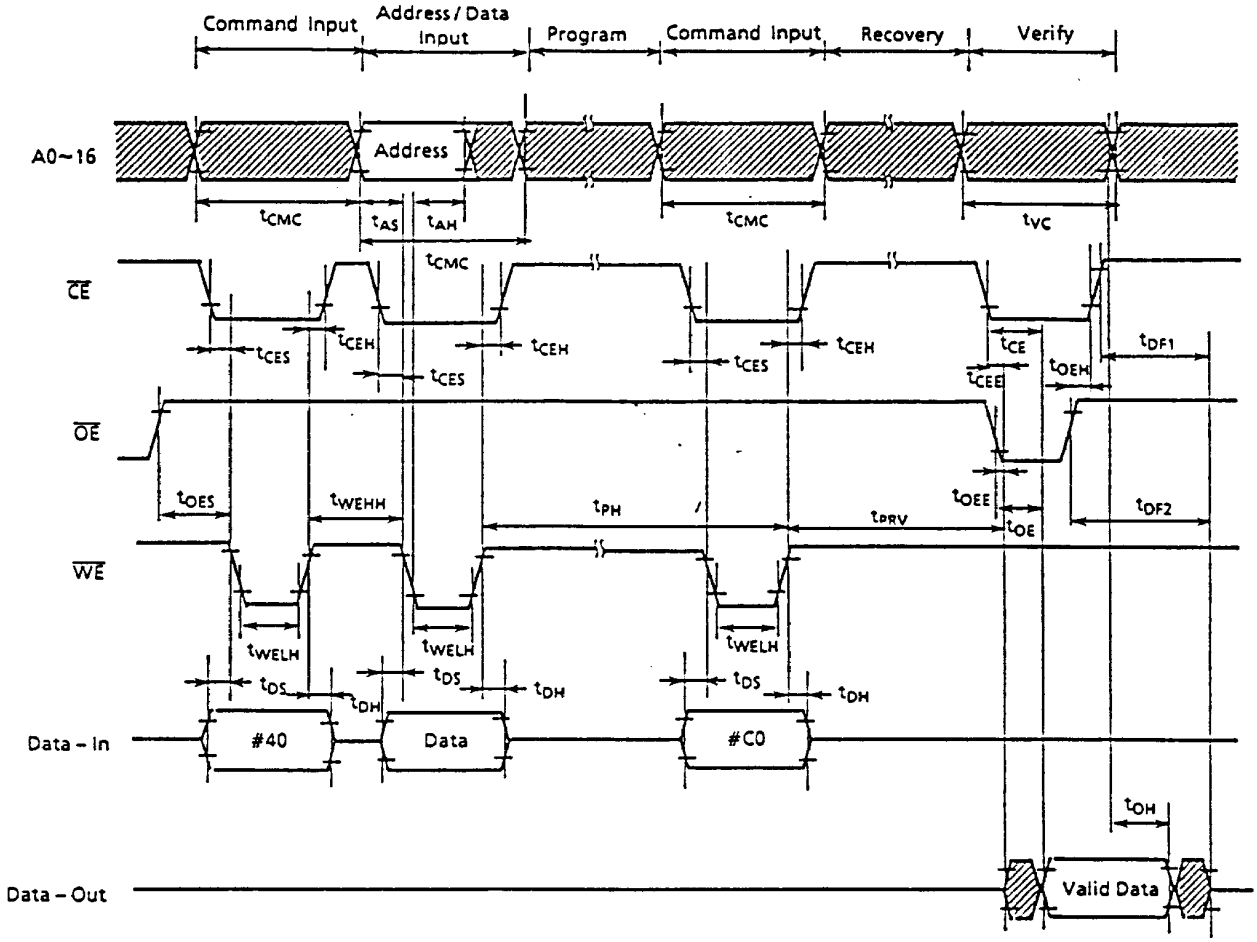
A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Time (10%~90%) : 5ns
- Input Pulse Levels : 0.45V to 2.40V
- Timing Measurement Reference Levels Input : 0.80V/2.20V
  Output : 0.80V/2.00V

Timing Waveform of Command Control Operation

Program Operation

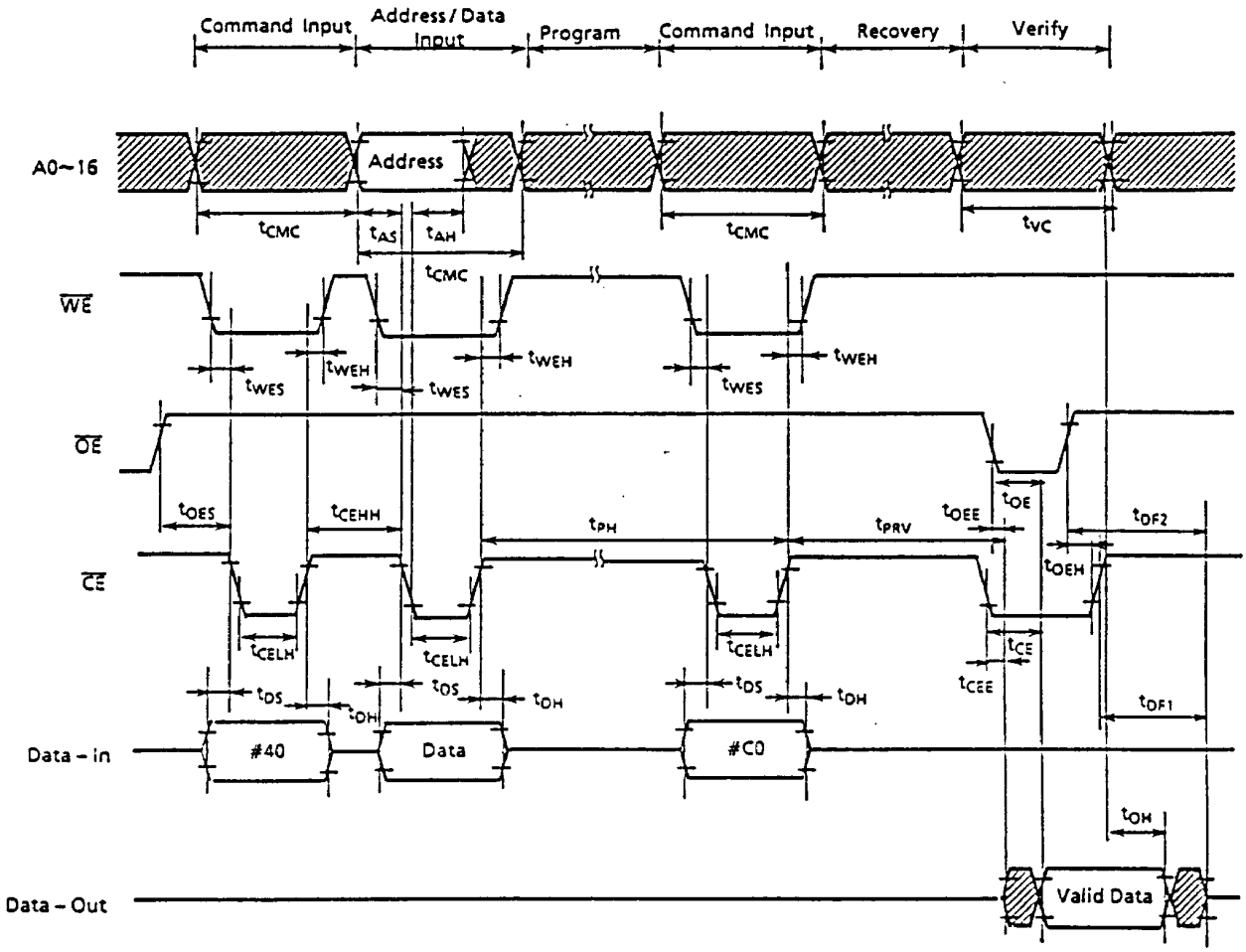
$\overline{WE}$ Control



Timing Waveform of Command Control Operation

Program Operation

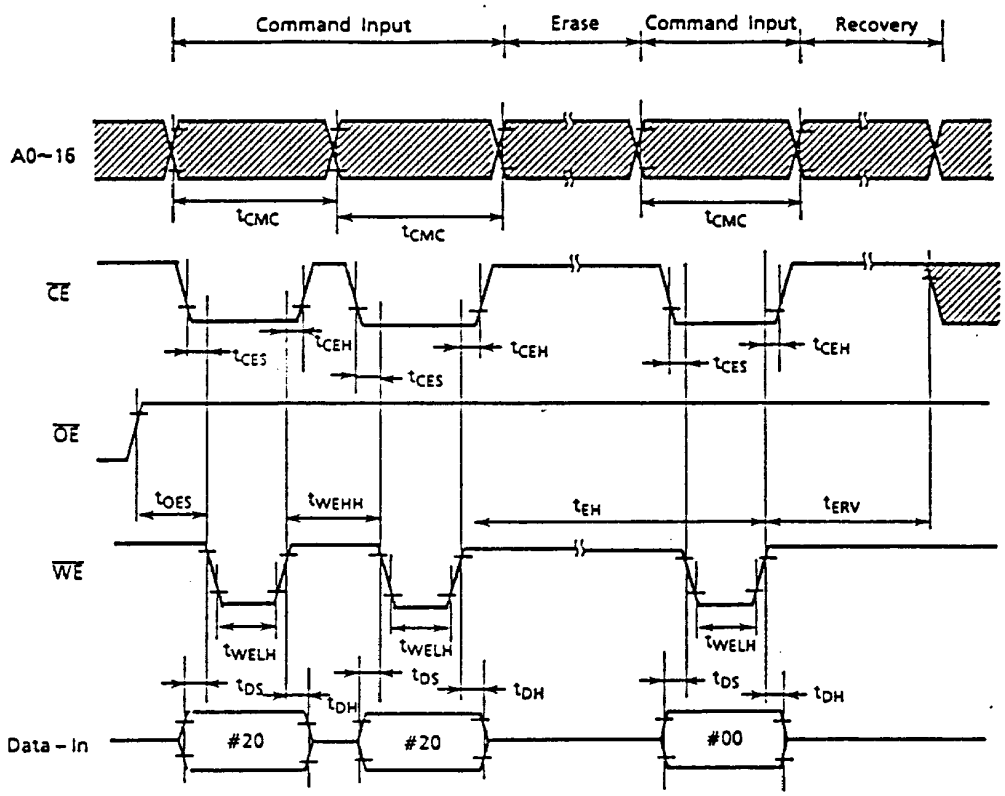
$\overline{CE}$ Control



Timing Waveform of Command Control Operation

Chip Erase Operation

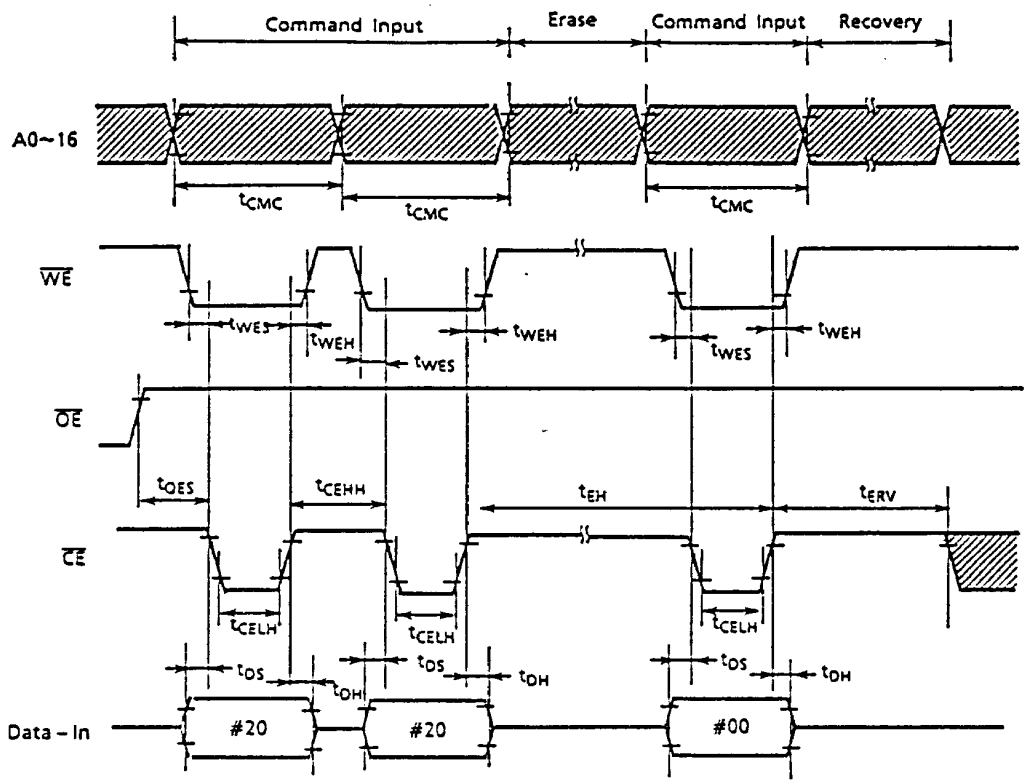
$\overline{WE}$ Control



Timing Waveform of Command Control Operation

Chip Erase Operation

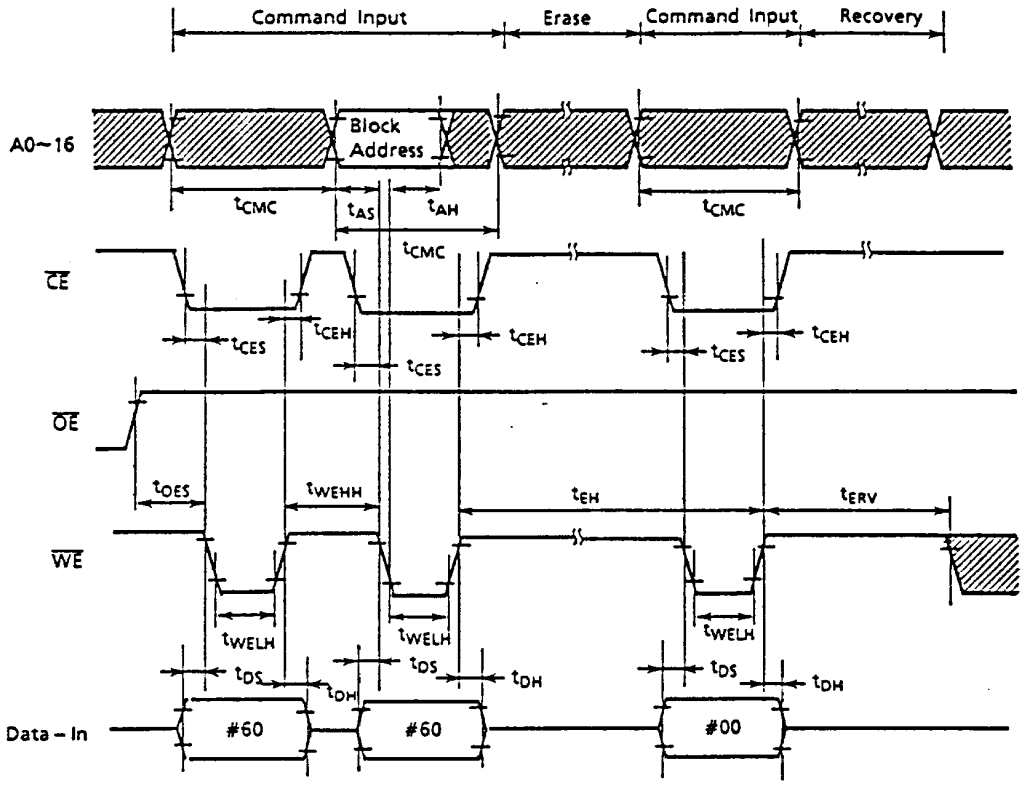
$\overline{CE}$ Control



Timing Waveform of Command Control Operation

Block Erase Operation

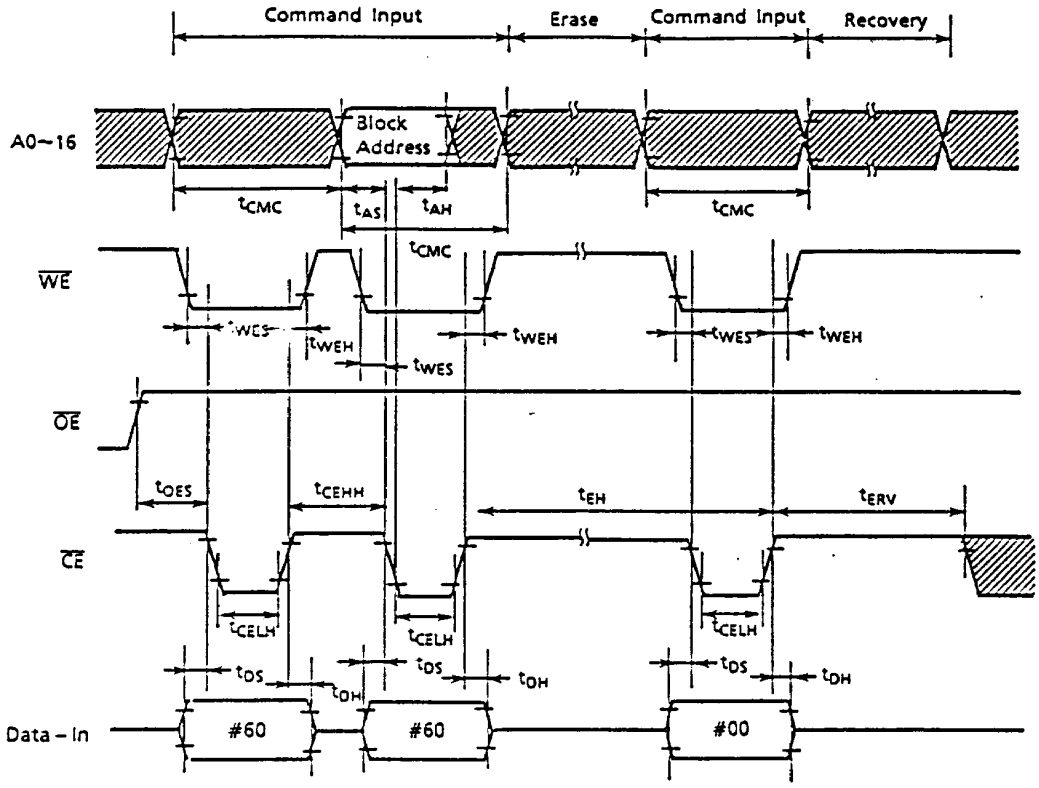
$\overline{WE}$ Control



Timing Waveform of Command Control Operation

Block Erase Operation

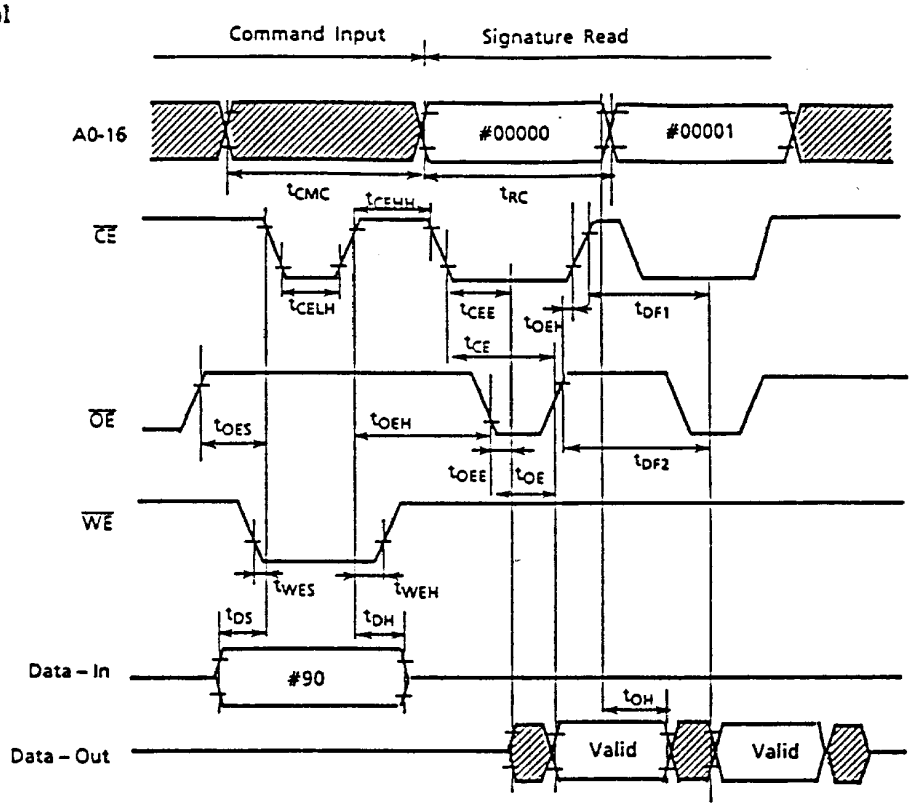
$\overline{CE}$ Control



Timing Waveform of Command Control Operation

Signature Read Operation

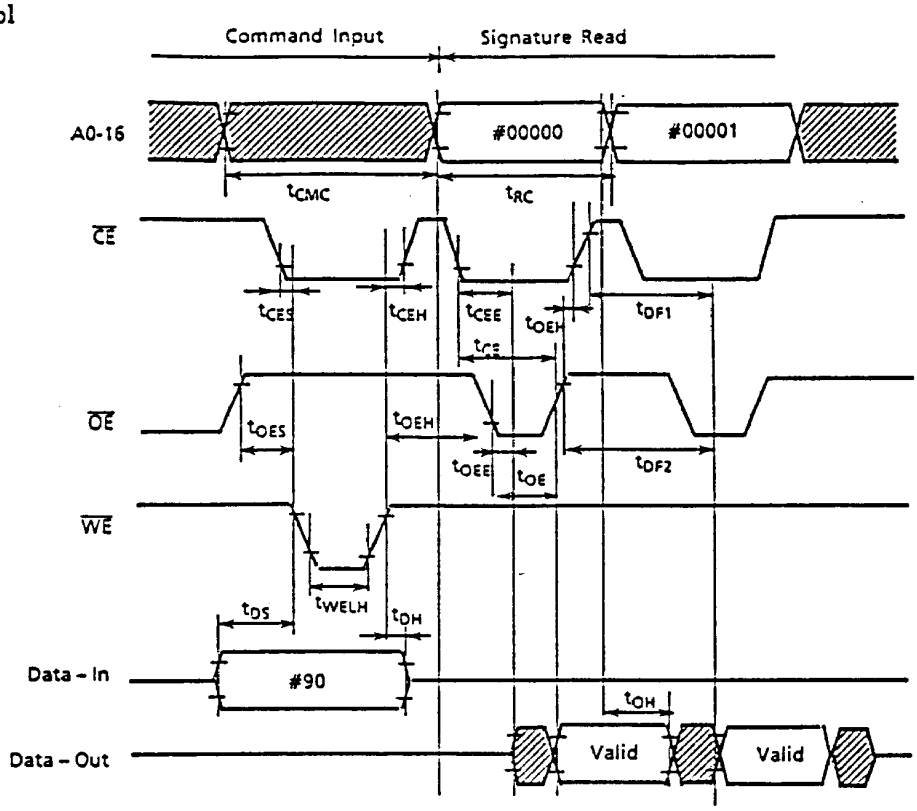
$\overline{CE}$ Control



Timing Waveform of Command Control Operation

Signature Read Operation

$\overline{WE}$ Control



3. EPROM COMPATIBLE OPERATION

($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{PP} = 12.0V \pm 5\%$, $V_{WE} = 12.0V \pm 5\%$)

SYMBOL	CHARACTERISTIC	MIN.	TYP	MAX	UNIT
t_{AS}	Address Setup time	2	-	-	μs
t_{AH}	Address Hold time	0	-	-	
t_{WP}	Programming Pulse Width	90	100	110	μs
t_{OESP}	Output Enable Setup time on Program Operation	2.0	-	-	
t_{CES}	Chip Erase Setup time on Verify Operation	0	-	-	ns
t_{CEH}	Chip Erase Hold time Verify Operation	0	-	-	
t_{DS}	Data Setup time	50	-	-	
t_{DH}	Data Hold time	0	-	-	
t_{EW}	Erasing Pulse Width	0.9	1.0	1.1	s
t_{OESE}	Output Enable Setup time on Erase Operation	0	-	-	ns
t_{OEHE}	Output Enable Hold time on Erase Operation	500	-	-	μs
t_{ACC}	Address Access time	-	-	150/200*	ns
t_{CE}	Chip Enable Access time	-	-	150/200*	
t_{OE}	Output Enable Access time	-	-	70	
t_{CEE}	Chip Enable to Output in Low-Z	0	-	-	
t_{OEE}	Output Enable to Output in Low-Z	0	-	-	
t_{OH}	Output Data Hold time	0	-	-	
t_{DF1}	Chip Enable to Output in High-Z	-	-	60	
t_{DF2}	Output Enable to Output in High-Z	-	-	60	
t_{RC}	Read cycle time	150/200*	-	-	
t_{VS}	V_{PP} Setup time	2.0	-	-	μs
t_{A9S}	V_{ID} Setup time	2.0	-	-	
t_{WES}	V_{WE} Setup time	2.0	-	-	

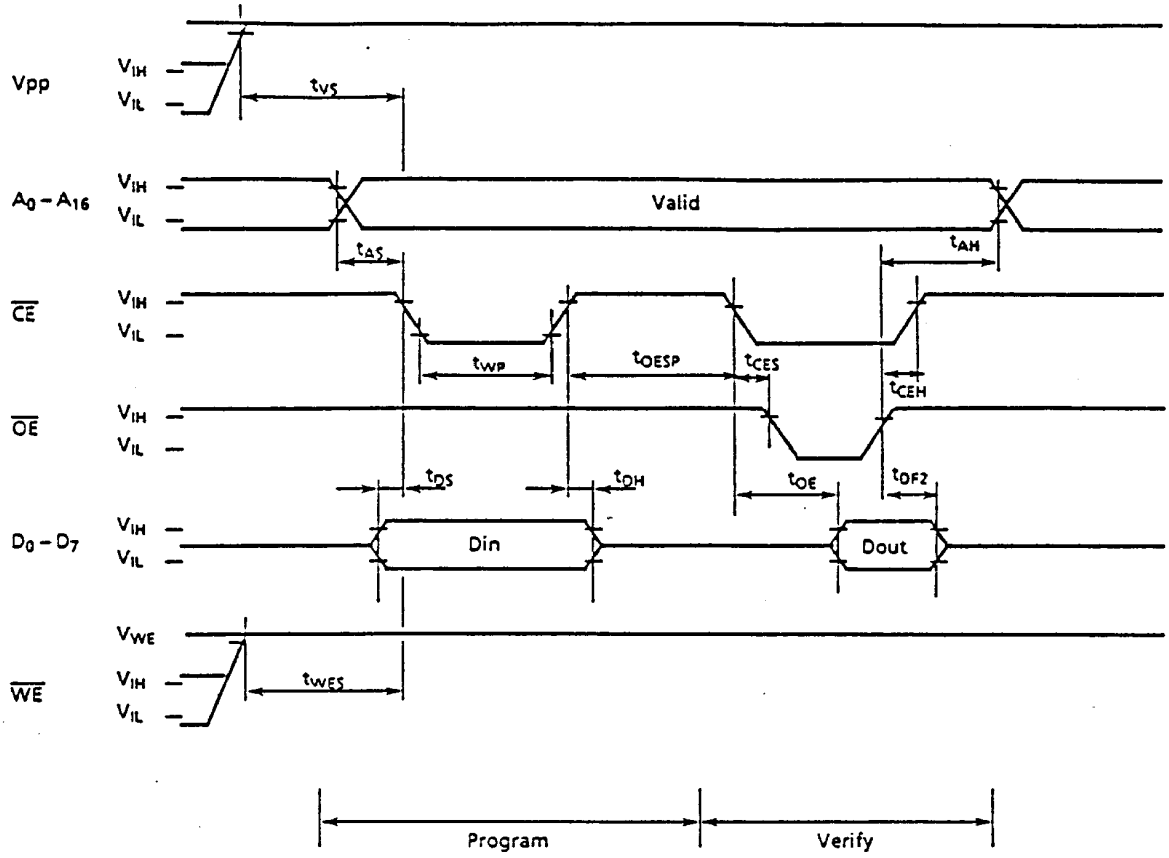
Note : * 150ns for TC58F1001P/F-15
200ns for TC58F1001P/F-20

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Time (10%~90%) : 5ns
- Input Pulse Level : 0.45V to 2.40V
- Timing Measurement Reference Level Input : 0.80V/2.20V
  Output : 0.80V/2.00V

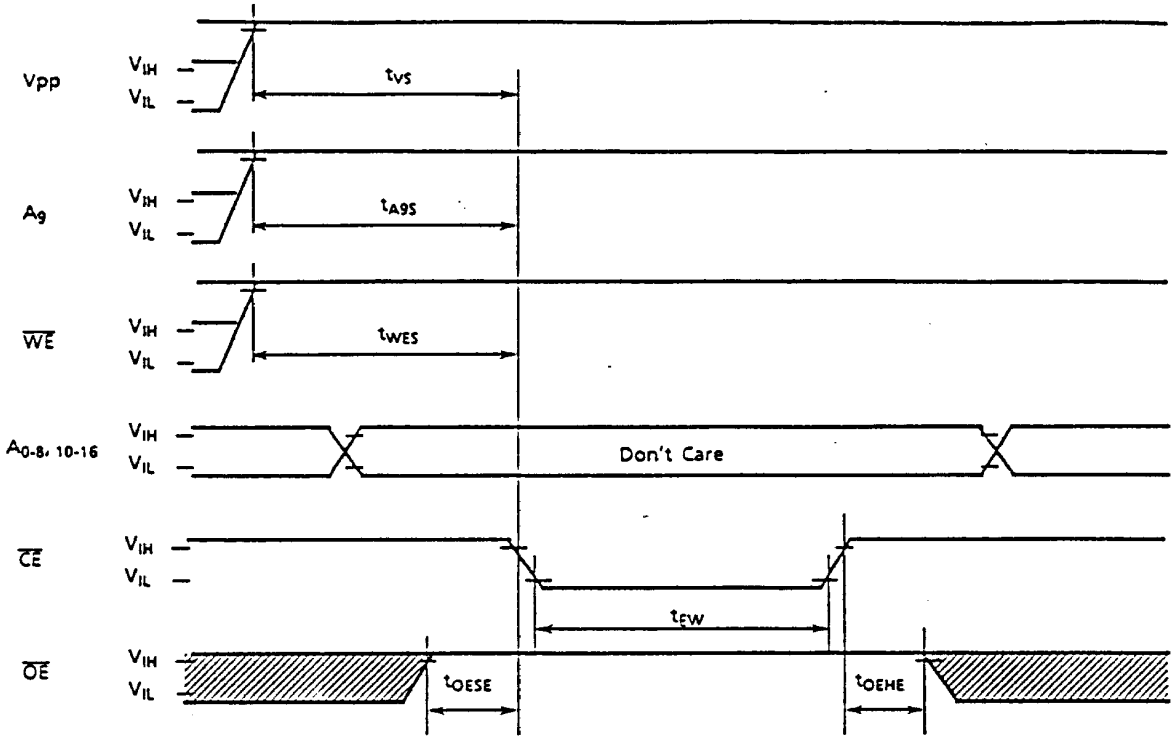
Timing Waveform of EPROM Compatible Operation

Program and Verify Operation



Timing Waveform of EPROM Compatible Operation

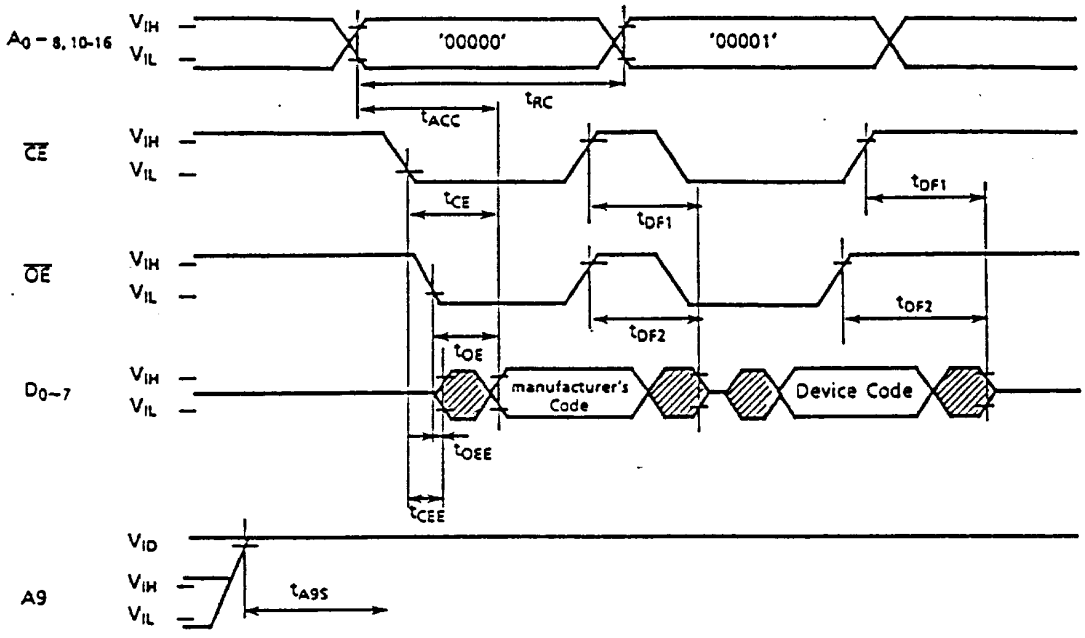
Erase Operation



Note : Din is don't care (H or L)

Timing Waveform of EPROM Compatible Operation

Signature Read Operation

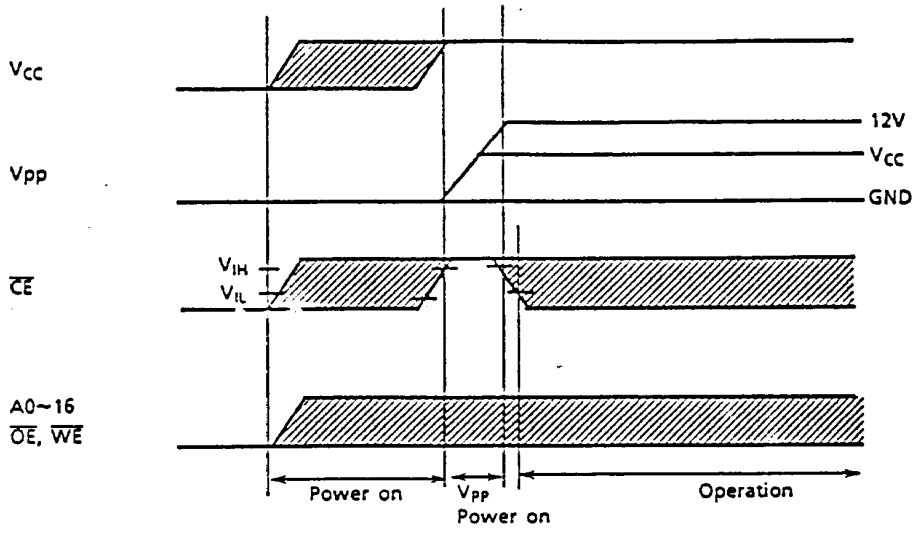


Note : $\overline{WE}=V_{IH}$, $V_{PP}=0V\sim V_{CC}$

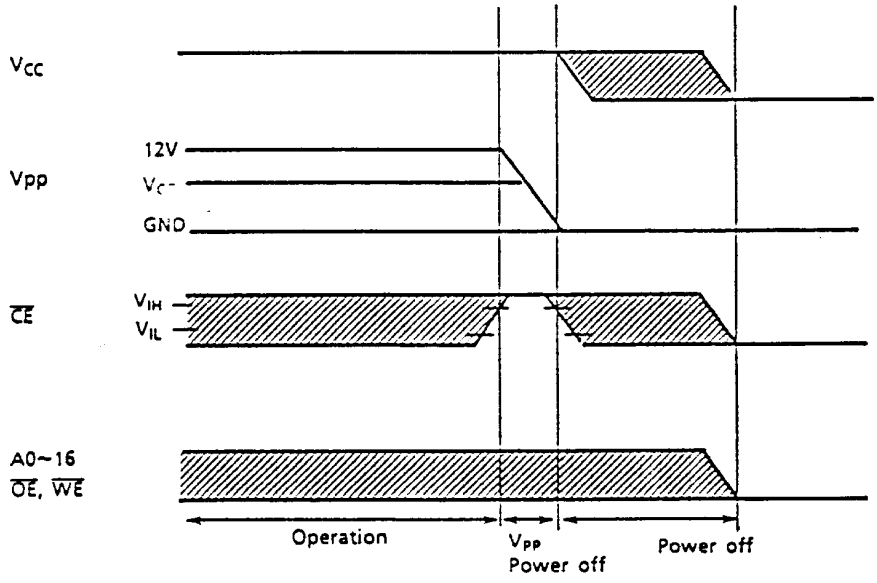
POWER ON/OFF SEQUENCE

This power on/off sequence protects against inadvertent programming or erasure.
In case of power on, V_{CC} and $\overline{CE}$ must be high level before V_{PP} becomming to be high level.
In case of power off, V_{CC} and $\overline{CE}$ must remain high level after V_{PP} becomming to be low level.

(1) Power on



(2) Power off



OPERATIONS

READ

The TC58F1001P/F has $\overline{CE}$ and $\overline{OE}$ pins. The chip enable ($\overline{CE}$) controls the operating power and should be used for device selection / deselection. The $\overline{CE}$ access time (t_{CE}) is equal to the address access time (t_{ACC}). The output enable ($\overline{OE}$) controls the output buffers. The output data is valid after a delay of t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT

When the $\overline{OE}$ input is high, the outputs are placed in the high-impedance state.

STANDBY

The TC58F1001P/F has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC58F1001P/F is placed in the standby mode and the outputs are in the high-impedance state, independent of the $\overline{OE}$ and $\overline{WE}$ inputs.

PROGRAM / PROGRAM-VERIFY / ERASE / ERASE-VERIFY / SIGNATURE-READ

The TC58F1001P/F features a command control mode and an EPROM compatible mode. The command control mode is used to enable the program, program-verify, chip-erase, block-erase, erase-verify, signature-read and reset operations, and the EPROM compatible mode controls the program, program-verify, chip-erase and signature-read operations.

1. COMMAND CONTROL MODE

The command code must be entered into the TC58F1001P/F before performing program, program-verify, erase (chip-erase and block-erase), erase-verify, signature-read, reset operations.

The command control is a useful for software protection method to protect from inadvertent operation. The command control mode is enabled when a high voltage (12V) is applied to V_{PP}.

TC58F1001P/F has an internal command register circuit and the operation mode is defined by the command codes. The specific data provided to the TC58F1001P/F is latched in the command registers and then the operation mode is defined. Data codes is latched by the $\overline{WE}$ signal.

1) PROGRAM OPERATION

The program operation is setup by the first step command code "40" and the address and data are latched at the second step, and then programming is performed. The program operation finishes at the time of receiving the program-verify command.

The command codes are as follows.

STEP (Bus Cycle)	Mode	Address	D0~7
1	Write	-	40(H)
2	Write	Address to be programmed	Data-in to be programmed

2) PROGRAM-VERIFY OPERATION

The program-verify operation is setup by providing the first step command code "C0" and performed at next step after recovery time of 2μs.

The program-verify address is already latched at the program operation.

The address is released after finished the program-verify.

The command codes are as follows.

STEP (Bus Cycle)	Mode	Address	D0~7
1	Write	-	C0
Recovery	-	-	-
2	Read	Don't Care	Data-out

3) ERASE OPERATION

The chip erase operation is setup by providing the two setup commands "20", "20" and then performed.

The chip erase command code consists of data code only.

The block erase operation is setup by providing the first step command "60" and second step command.

The block address is defined at second step command input.

The erase operation finishes at the time of receiving the erase-verify or read command.

The memory cell array is divided into 32 blocks (4K byte/block) and block address is assigned with A_{12}~A_{16}.

The command codes are as follows.

a) Chip erase operation

STEP (Bus Cycle)	Mode	Address	D0~7
1	Write	-	20(H)
2	Write	-	20(H)

b) Block erase operation

STEP (Bus Cycle)	Mode	Address	D0~7
1	Write	-	60(H)
2	Write	Block Address	60(H)

4) ERASE-VERIFY OPERATION

The erase verify operation is setup by providing the setup erase-verify command and performed at next step after recovery time of 500μs. The erase verify operation is helpful for confirming to be erased.

Once the erase-verify operation is performed, the next erase verify operation can be performed by subsequently providing the next address without command.

The command codes are as follows.

STEP (Bus Cycle)	Mode	Address	D0~7
1	Write	–	A0
Recovery	–	–	–
2	Read	Address	Data-out

5) SIGNATURE READ OPERATION

The signature-read operation is setup by providing the setup command of signature-read and performed to read the manufacture code by providing address 00000 (H) at the second step and to read the device code by providing address 00001 (H) at the third step.

The command codes are as follows.

STEP (Bus Cycle)	Mode	Address	D0~7
1	Write	–	90(H)
2	Read	00000 (H)	Manufacture's Code-Out
3	Read	00001 (H)	Device Code-Out

6) RESET

The reset command is used for aborting program, program-verify, erase, block erase, and erase-verify operations, and then the device turns to be read mode.

The command codes are as follows.

STEP (Bus Cycle)	Mode	Address	D0~7
1	Write	–	FF(H)
2	Write	–	FF(H)

7) READ OPERATION

The read operation is performed by providing the read command with Vpp at 12V.

The command codes are as follows.

STEP (Bus Cycle)	Mode	Address	D0~7
1	Write	–	00(H)
2	Read	Address	Data-Out

<Command Control Code Table>

Mode \ Step		Command step 1	Command step 2
Program	Mode	Write	Write
	Address	–	Program Address
	Data	#40	Program Data
Program – Verify	Mode	Write	Read
	Address	–	–
	Data	#C0	Data out
Signature – Read	Mode	Write	Read
	Address	–	–
	Data	#90	Data out
Chip Erase	Mode	Write	Write
	Address	–	–
	Data	#20	#20
Block Erase	Mode	Write	Write
	Address	–	Block Address
	Data	#60	#60
Erase – Verify	Mode	Write	Read
	Address	–	Verify Address
	Data	#A0	Data out

Mode \ Step		Command step 1	Command step 2
Read	Mode	Write	–
	Address	–	–
	Data	#00	–
Reset	Mode	Write	Write
	Address	–	–
	Data	#FF	#FF

<Block Address Table>

Block No.	Addresss Area	Hex Adresss	A16	A15	A14	A13	A12	A11~A0
1	00000~00FFF	00XXX	0	0	0	0	0	Don't Care
2	01000~01FFF	01XXX	0	0	0	0	1	Don't Care
3	02000~02FFF	02XXX	0	0	0	1	0	Don't Care
4	03000~03FFF	03XXX	0	0	0	1	1	Don't Care
5	04000~04FFF	04XXX	0	0	1	0	0	Don't Care
6	05000~05FFF	05XXX	0	0	1	0	1	Don't Care
7	06000~06FFF	06XXX	0	0	1	1	0	Don't Care
8	07000~07FFF	07XXX	0	0	1	1	1	Don't Care
9	08000~08FFF	08XXX	0	1	0	0	0	Don't Care
10	09000~09FFF	09XXX	0	1	0	0	1	Don't Care
11	0A000~0AFFF	0AXXX	0	1	0	1	0	Don't Care
12	0B000~0BFFF	0BXXX	0	1	0	1	1	Don't Care
13	0C000~0CFFF	0CXXX	0	1	1	0	0	Don't Care
14	0D000~0DFFF	0DXXX	0	1	1	0	1	Don't Care
15	0E000~0EFFF	0EXXX	0	1	1	1	0	Don't Care
16	0F000~0FFFF	0FXXX	0	1	1	1	1	Don't Care
17	10000~10FFF	10XXX	1	0	0	0	0	Don't Care
18	11000~11FFF	11XXX	1	0	0	0	1	Don't Care
19	12000~12FFF	12XXX	1	0	0	1	0	Don't Care
20	13000~13FFF	13XXX	1	0	0	1	1	Don't Care
21	14000~14FFF	14XXX	1	0	1	0	0	Don't Care
22	15000~15FFF	15XXX	1	0	1	0	1	Don't Care
23	16000~16FFF	16XXX	1	0	1	1	0	Don't Care
24	17000~17FFF	17XXX	1	0	1	1	1	Don't Care
25	18000~18FFF	18XXX	1	1	0	0	0	Don't Care
26	19000~19FFF	19XXX	1	1	0	0	1	Don't Care
27	1A000~1AFFF	1AXXX	1	1	0	1	0	Don't Care
28	1B000~1BFFF	1BXXX	1	1	0	1	1	Don't Care
29	1C000~1CFFF	1CXXX	1	1	1	0	0	Don't Care
30	1D000~1DFFF	1DXXX	1	1	1	0	1	Don't Care
31	1E000~1EFFF	1EXXX	1	1	1	1	0	Don't Care
32	1F000~1FFFF	1FXXX	1	1	1	1	1	Don't Care

X : Don't care

2. EPROM COMPATIBLE MODE

This mode is the same as Toshiba's 256K FE²PROM, the TC58257A. When a high-voltage (12V) is applied to the $\overline{WE}$ pin of the TC58F1001P/F, the program and erase operations can be easily performed by conventional EPROM programmer.

(1) PROGRAM OPERATION

TC58F1001P/F is placed in the programming mode by applying a high voltage (12V) to the V_{PP} and $\overline{WE}$ pins. During the programming operation, the addresses and input data must be held the $\overline{OE}$ signal must be held high and the $\overline{CE}$ input must be low. The programming time is controlled by the $\overline{CE}$ pulse width.

(2) PROGRAM-VERIFY OPERATION

The programmed data is verified with the V_{PP} and $\overline{WE}$ pins held at high voltage (12V) level and with $\overline{CE}$ and $\overline{OE}$ held at V_{IL}.

(3) CHIP ERASE OPERATION

TC58F1001P/F is placed in the chip erase mode by applying a high voltage (12V) to the V_{PP}, $\overline{WE}$ and A9 pins. During the chip erase operation, address A0~A8 and A10~A16 are "don't care", $\overline{OE}$ must be held high and $\overline{CE}$ must be low. The erase time is controlled by $\overline{CE}$ pulse width.

(4) ELECTRIC SIGNATURE READ

With V_{PP} held at a voltage between 0V and V_{CC}, $\overline{WE}$ held at V_{IH}, the manufacturer's code can be read by specifying address 00000(H) and the device code can be read by specifying address 00001(H) by applying a high voltage (12V) to the A9 address input. Toshiba's manufacturer code and the TC58F1001P/F device code are shown in the table below.

TC58F1001P/F

Signature	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Manufacturer's Code	0	1	0	0	1	1	0	0	0	98
Device Code	1	0	0	1	0	0	1	1	0	26

APPLICATIONS

Toshiba's TC58F1001P/F Flash-E²PROM offers a cost-competitive and reliable alternative for applications which have traditionally employed the U.V. EPROM or O.T. PROM.

The Flash-E²PROM adds electrical erasure capability and eliminates the time consuming and labor intensive process of U.V. light exposure for erasing EPROMs. Furthermore, the Flash-E²PROM is electrically reprogrammable and thus eliminates the one-time programmable limitation of the O.T. PROM.

The TC58F1001P/F is offered in plastic DIP and surface mount packages (SOP) which can be processed through the automated assembly line process. The electrically programmable and erasable features of the Flash-E²PROM eliminate the need for sockets both at the prototype stage and at the production stage. The major application advantages offered by the Flash-E²PROM in system design are listed below.

In-System Programming

The TC58F1001P/F is provided with a command control mode which makes it possible to program and erase data by using the system MPU timing. The TC58F1001P/F can be used for updating the system operating code or data in the system through a telecommunication line or a floppy disk interface. In this case, a 12V power supply must be available in the system.

On-Board Programming with an External Programmer

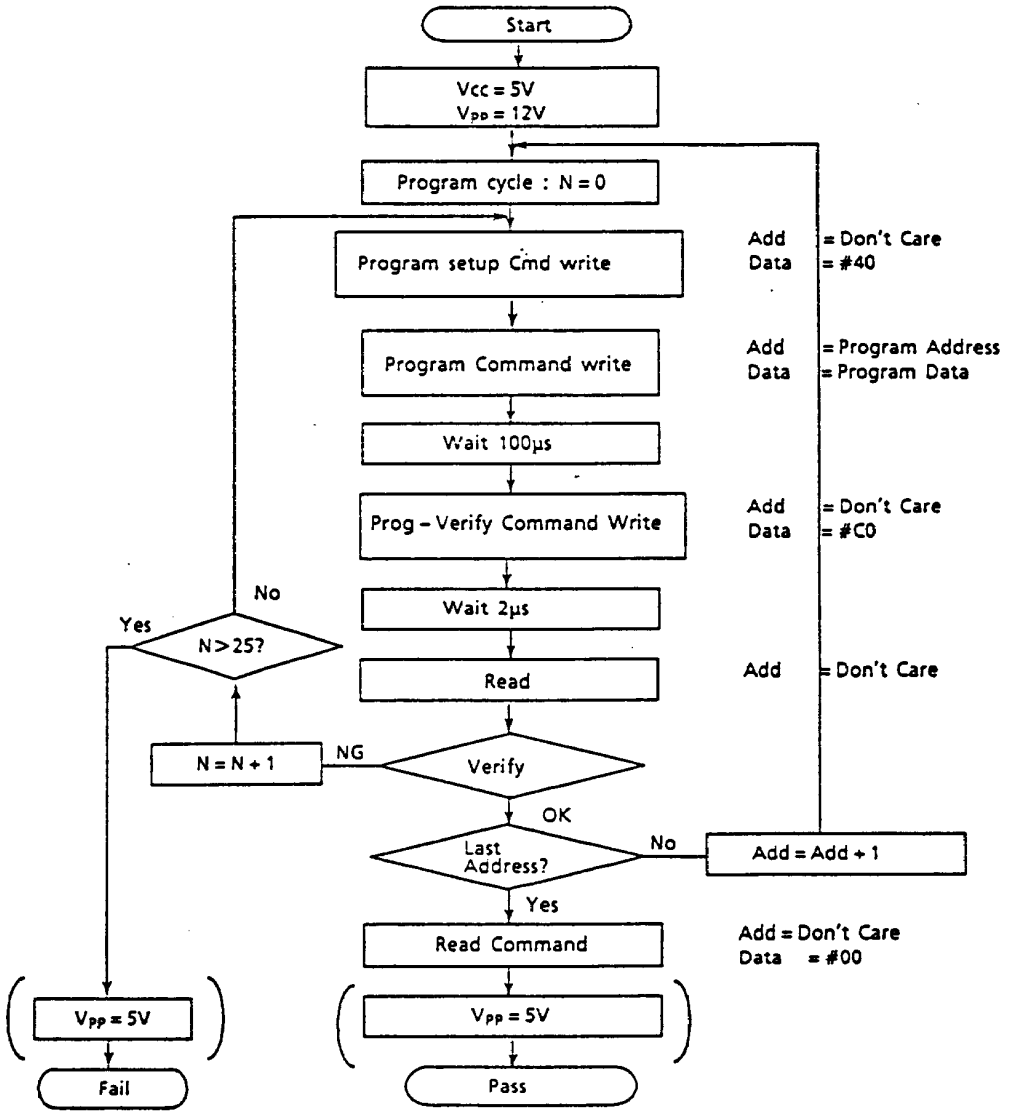
The TC58F1001P/F can be mounted directly onto the system board and all subsequent program and erase operations can be handled by an external PROM programmer through a connector. Since the TC58F1001P/F supports an EPROM compatible programming mode, a conventional PROM programmer can be used for this operation.

Card and Cartridge Applications

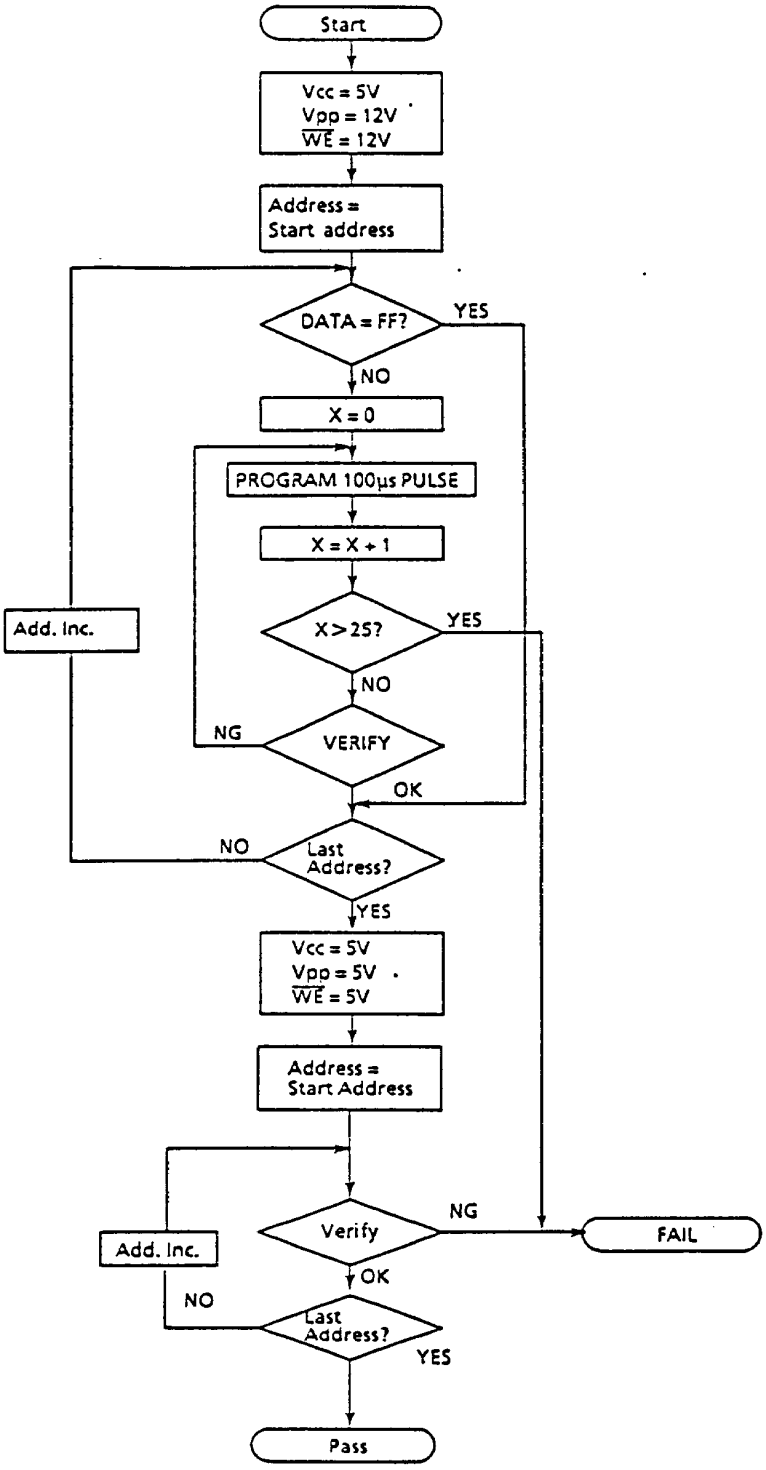
High density non-volatile memory cards and cartridges can be assembled by using the SOP surface mount version of Toshiba's TC58F1001. These cards and cartridges can be erased and reprogrammed using either the in-system programming method or an external programmer.

Program Flow Chart

① Command Control mode

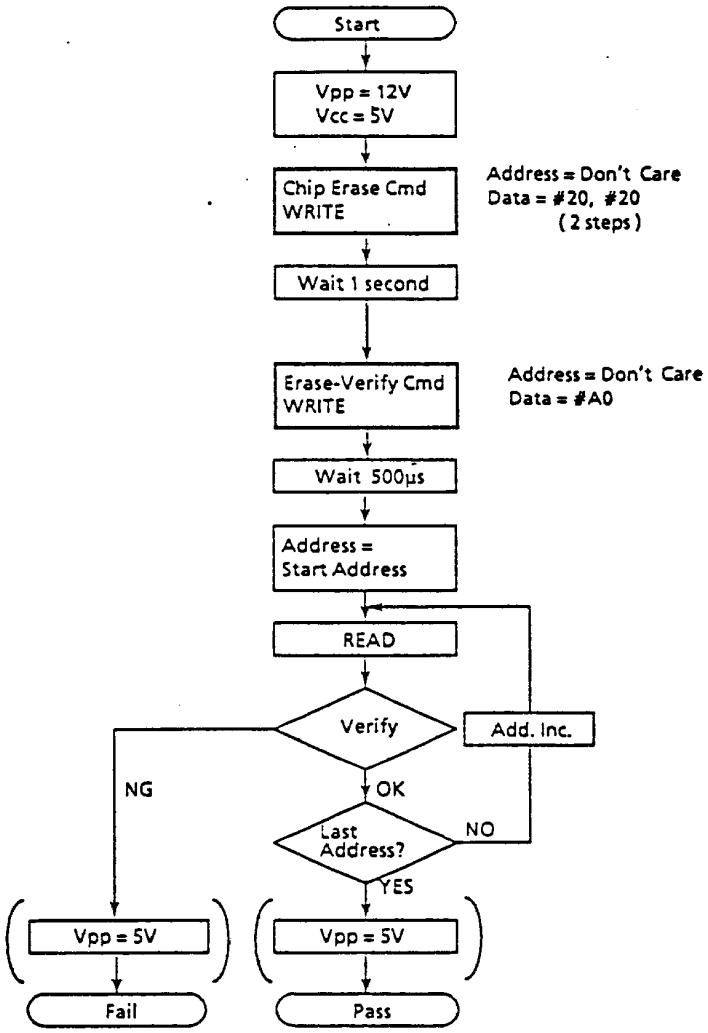


② EPROM Compatible mode

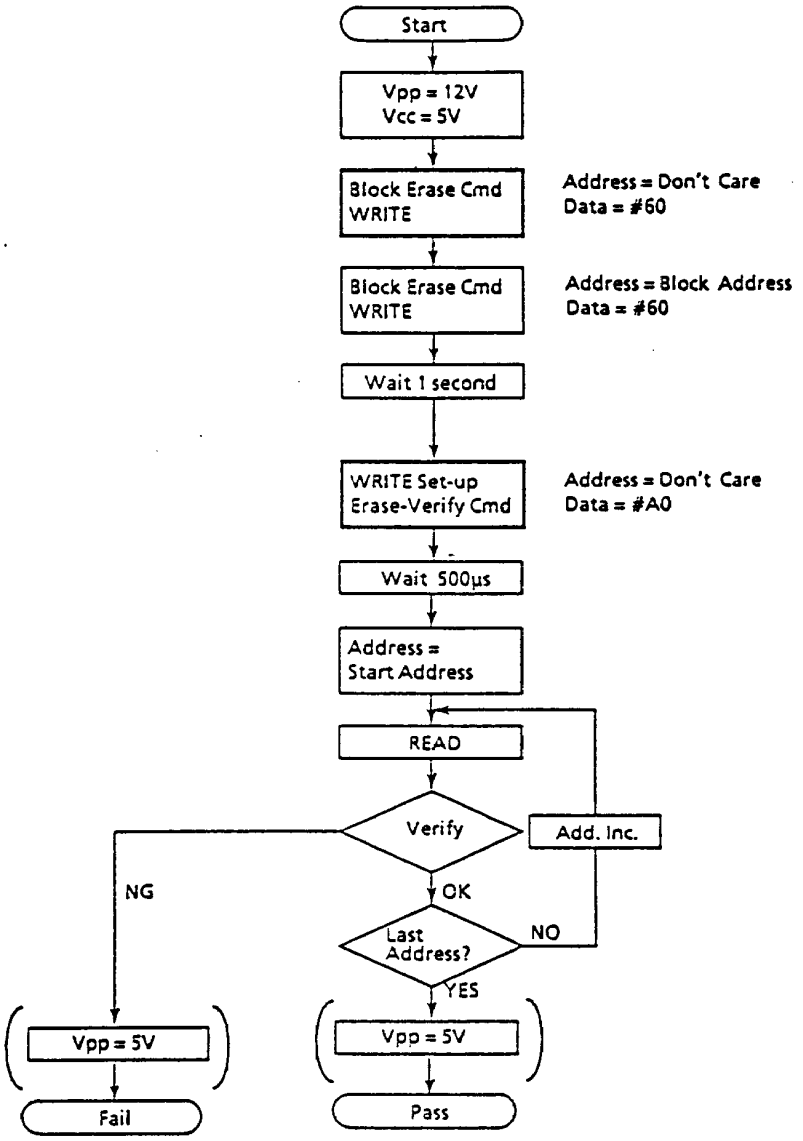


Electrical Erase Flow Chart

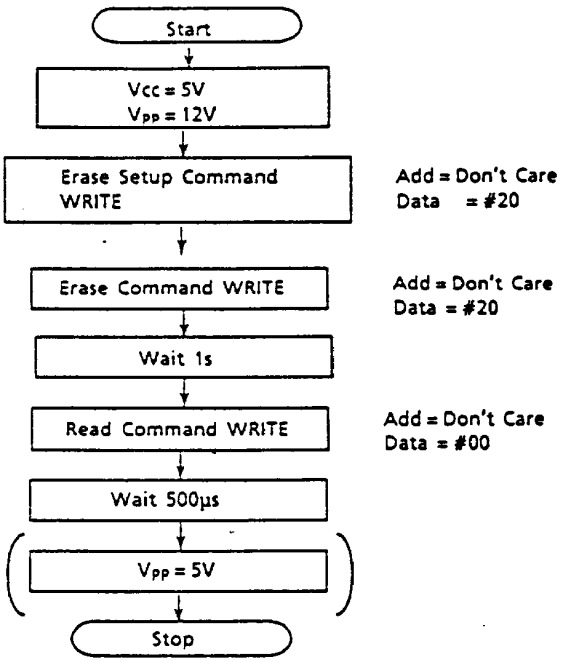
1) Chip Erase–Erase Verify



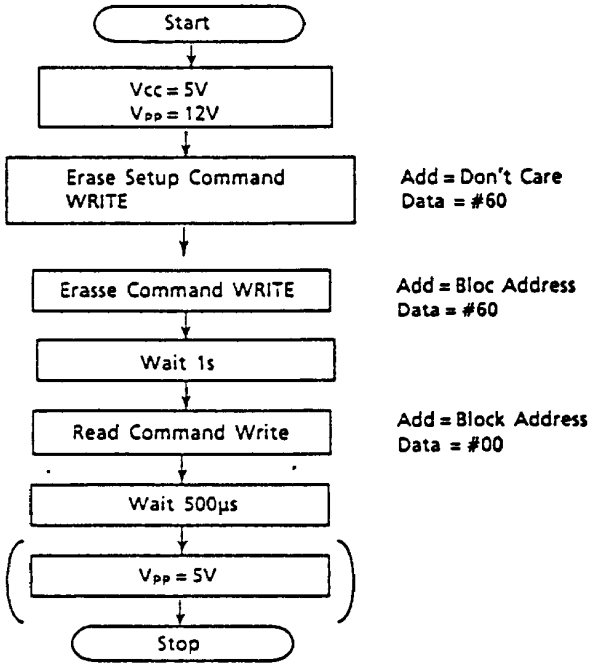
2) Block Erase–Erase Verify



3) Chip Erase without Erase–Verify



4) Block Erase without Erase–Verify

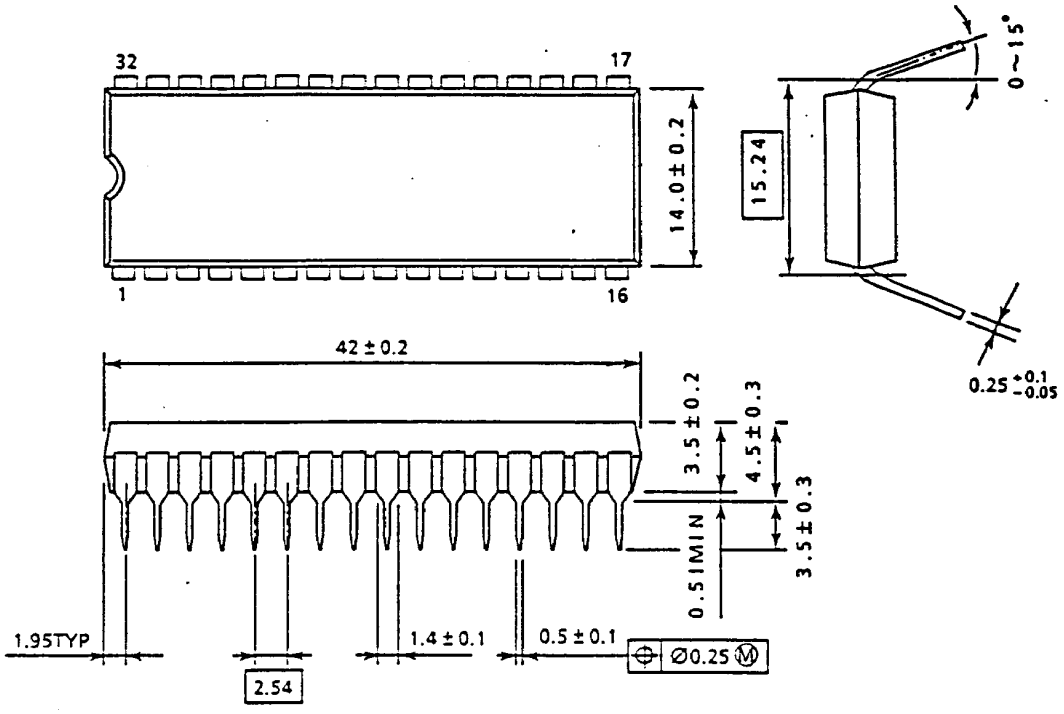


OUTLINE DRAWINGS

- Plastic DIP

DIP32-P-600

UNIT : mm



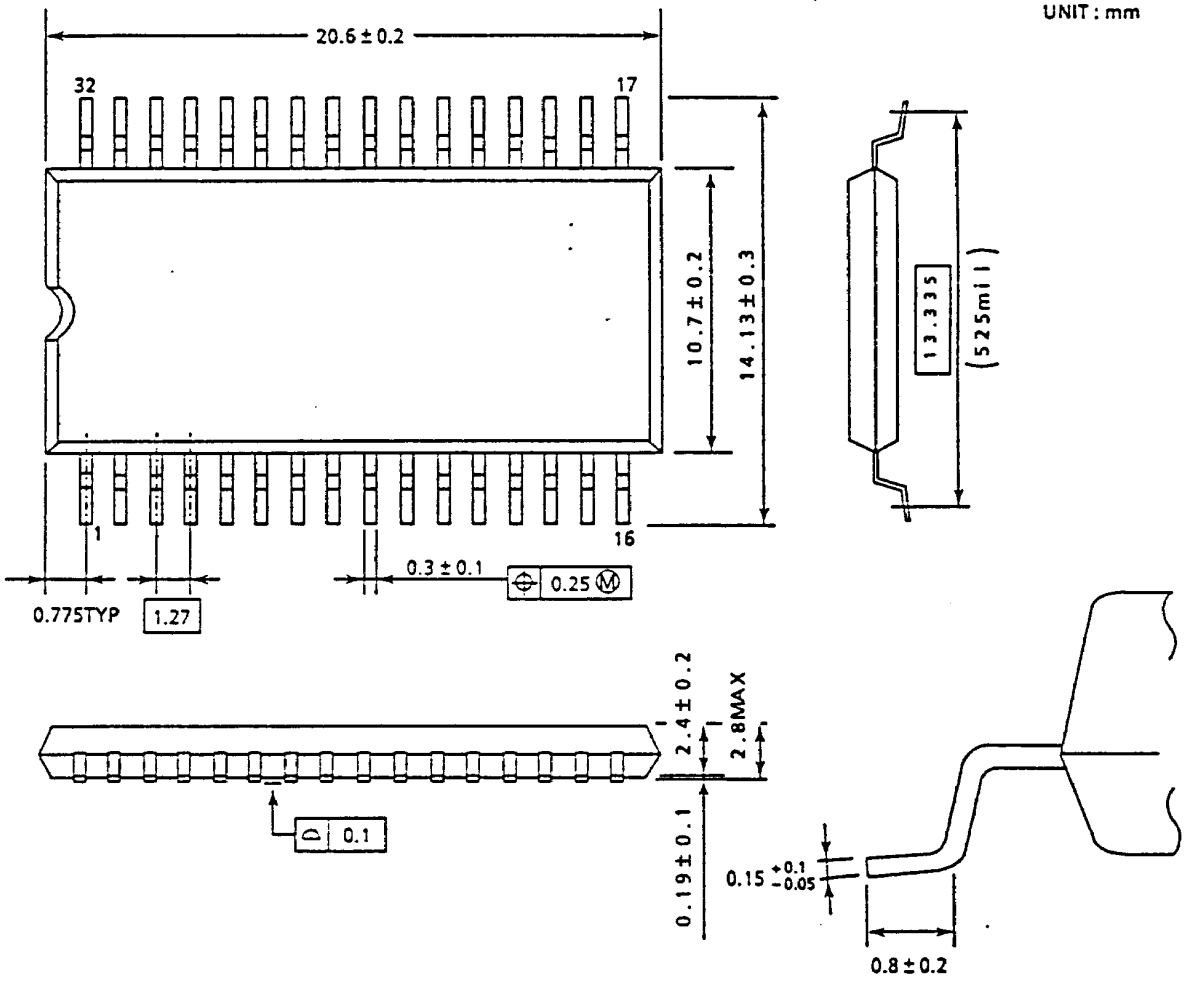
Note : Package width and length do not include mold protrusion, allowable mode protrusion is 0.15mm.

OUTLINE DRAWINGS

- Plastic SOP

  SOP32-P-525

UNIT : mm



Note : Package width and length do not includ protrusion, allowable mold protrusion is 0.15mm.