19-2396; Rev 0; 4/02

MAXIM

Quad Bus LVDS Transceiver in 44 QFN

General Description

The MAX9158 is a quad bus LVDS (BLVDS) transceiver for heavily loaded, half-duplex multipoint buses. A 44-lead QFN package and flow-through pinout allow the transceiver to be placed near the connector. The MAX9158 drives LVDS levels into a 27Ω load (double terminated, heavily loaded LVDS bus) at up to 200Mbps. An input fail-safe circuit ensures the receiver output is high when the differential inputs are open, or undriven and shorted, or undriven and terminated. The MAX9158 operates from a single 3.3V supply, consuming 77mA supply current with drivers enabled, and 19.9mA with drivers disabled.

The MAX9158's high-impedance I/Os (except for receiver outputs) when V_{CC} = 0V or open, combined with glitch-free power-up and power-down, allow hot swapping of cards in multicard bus systems; 7.3pF (max) BLVDS I/O capacitance minimizes bus loading.

The MAX9158 is offered in a 7mm × 7mm 44-lead QFN package, and is fully specified for the -40°C to +85°C extended temperature range. Refer to the MAX9157 data sheet for a quad BLVDS transceiver with hysteresis in 32-lead QFN and TQFP packages. Refer to the MAX9129 data sheet for a quad BLVDS driver, ideal for dual multipoint full-duplex buses.

Applications

- Add/Drop Muxes
- Digital Cross-Connects
- Network Switches/Routers
- Cellular Phone Base Stations
- DSLAMs
- Multipoint Buses

Functional Diagram appears at end of data sheet.

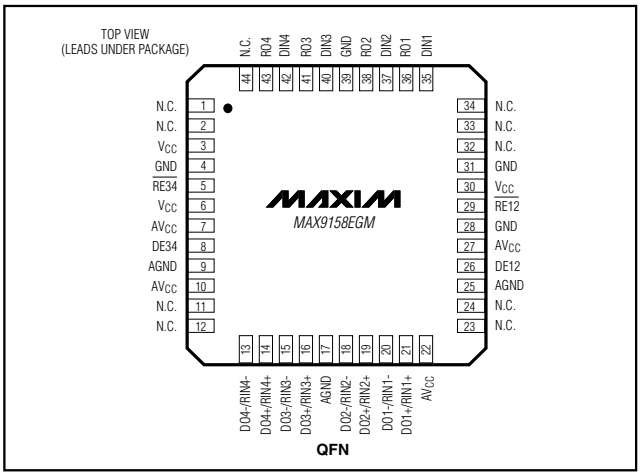
Features

- **44-Lead QFN Package**
- **1ns (min) Driver Transition Time (0% to 100%) Minimizes Reflections**
- **Guaranteed 7.3pF (max) Bus Load Capacitance**
- **Glitch-Free Power-Up and Power-Down**
- **Hot-Swappable, High-Impedance I/O with V_{CC} = 0V or Open**
- **Guaranteed 200Mbps Driver Data Rate**
- **Low-Jitter Fail-Safe Circuit**
- **Flow-Through Pinout**

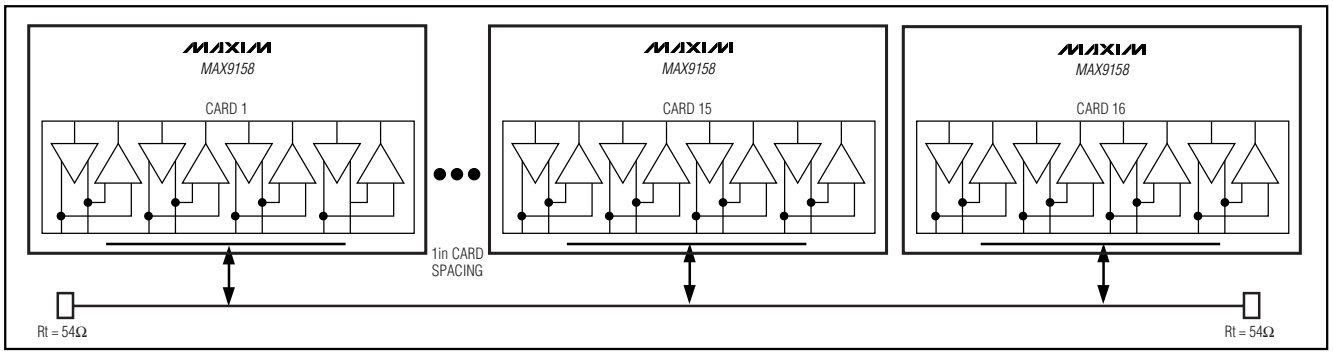
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9158EGM	-40°C to +85°C	44 QFN (7mm × 7mm)

Pin Configuration



Typical Operating Circuit



Quad Bus LVDS Transceiver in 44 QFN

ABSOLUTE MAXIMUM RATINGS

V_{CC}, AV_{CC} to GND .....-0.3V to +4.0V
DO_+/RIN_+, DO_-/RIN_- to GND .....-0.3V to +4.0V
DIN_, DE_, $\overline{RE}$_ to GND.....-0.3V to +4.0V
RO_ to GND.....-0.3V to (V_{CC} + 0.3V)
AGND to GND .....-0.3V to +0.3V
Short-Circuit Duration (DO_+/RIN_+, DO_-/RIN_-) ....Continuous
Continuous Power Dissipation (T_A = +70°C)
44-Lead QFN (derate 24.3mW/°C above +70°C) 2105mW
Storage Temperature Range .....-65°C to +150°C
Maximum Junction Temperature .....+150°C
Operating Temperature Range .....-40°C to +85°C
ESD Protection
Human Body Model (DO_+/RIN_+, DO_-/RIN_-).....±4kV
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 3.6V, R_L = 27Ω ±1%, receiver differential input voltage $|V_{ID}|$ = 0.1V to 3.0V, receiver input common-mode voltage V_{CM} = 0.05V to 2.4V, receiver input voltage range = 0V to 3.0V, DE_ = high, $\overline{RE}$_ = low, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, and T_A = +25°C.) (Notes 1 and 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BLVDS (DO_+/RIN_+, DO_-/RIN_-)						
Differential Input High Threshold	V_{TH}	DE_ = low		4.0	100	mV
Differential Input Low Threshold	V_{TL}	DE_ = low	-100	-4.3		mV
Input Current	I_{IN+}, I_{IN-}	0.1V ≤ $\|V_{ID}\|$ ≤ 0.6V, DE_ = low	-15	±1.7	+15	µA
		0.6V < $\|V_{ID}\|$ ≤ 1.2V, DE_ = low	-20	±2.3	+20	
Input Resistance	R_{IN1}	V_{CC} = 3.6V, 0V or open, Figure 1	53			kΩ
	R_{IN2}	V_{CC} = 3.6V, 0V or open, Figure 1	148			
Power-Off Input Current	I_{INO+}, I_{INO-}	0.1V ≤ $\|V_{ID}\|$ ≤ 0.6V, V_{CC} = 0V or open	-15	±0.9	+15	µA
		0.6V < $\|V_{ID}\|$ ≤ 1.2V, V_{CC} = 0V or open	-20	±1.9	+20	
Differential Output Voltage	V_{OD}	Figure 2	250	398	460	mV
Change in Magnitude of V_{OD} for Complementary Output States	ΔV_{OD}	Figure 2		1	25	mV
Offset Voltage	V_{OS}	Figure 2	1.185	1.274	1.435	V
Change in Magnitude of V_{OS} for Complementary Output States	ΔV_{OS}	Figure 2		1.9	25	mV
Output High Voltage	V_{OH}	Figure 2		1.473	1.650	V
Output Low Voltage	V_{OL}	Figure 2	0.950	1.075		V
Output Short-Circuit Current	I_{OS}	DIN_ = high, DO_+/RIN_+ = 0V or V_{CC}, DO_-/RIN_- = 0V or V_{CC}	-30		+30	mA
		DIN_ = low, DO_-/RIN_- = 0V or V_{CC}, DO_+/RIN_+ = 0V or V_{CC}	-30		+30	

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.0V to 3.6V, R_L = 27Ω ±1%, receiver differential input voltage $|V_{ID}|$ = 0V.1V to 3.0V, receiver input common-mode voltage V_{CM} = 0.05V to 2.4V, receiver input voltage range = 0V to 3.0V, DE_ = high, $\overline{RE}$_ = low, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, and T_A = +25°C.) (Notes 1 and 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Output Short-Circuit Current Magnitude (Note 3)	I_{OSD}	DIN_ = high or low, V_{OD} = 0V			14.8	30	mA
Capacitance at Bus Pins (Note 3)	C_{OUTPUT}	Capacitance from DO_+/RIN_+ or DO_-/RIN_- to GND, V_{CC} = 3.6V or 0V				7.3	pF
LVCMOS/LVTTL OUTPUTS (RO_)							
Output High Voltage	V_{OH}	I_{OH} = -4.0mA, DE_ = low	Open, undriven short, or undriven 27Ω parallel termination	V_{CC} - 0.3	V_{CC} - 0.138		V
			V_{ID} = 100mV	V_{CC} - 0.3	V_{CC} - 0.138		
Output Low Voltage	V_{OL}	I_{OL} = 4.0mA, V_{ID} = -100mV, DE_ = low			0.176	0.25	V
Dynamic Output Current	I_{OD}	V_{ID} = 100mV, $V_{RO\_}$ = V_{CC} - 1.0V, DE_ = low		-15	-25.8	-40	mA
		V_{ID} = -100mV, $V_{RO\_}$ = 1.0V, DE_ = low		12	20.7	40	
Output Short-Circuit Current (Note 4)	I_{OS}	V_{ID} = 100mV, $V_{RO\_}$ = 0V, DE_ = low			-45	-130	mA
Output High-Impedance Current	I_{OZ}	$\overline{RE}$_ = high, V_{RO} = 0V or V_{CC}		-10	0.1	+10	µA
Capacitance at Receiver Output (Note 3)	C_{OUTPUT}	Capacitance from RO_ to GND, V_{CC} = 3.6V or 0V				4.6	pF
LVCMOS/LVTTL INPUTS (DIN, DE, $\overline{RE}$)							
Input High Voltage	V_{IH}			2.0		V_{CC}	V
Input Low Voltage	V_{IL}			GND		0.8	V
Input Current	I_{IN}	$V_{DE\_}$, $V_{\overline{RE}\_}$, $V_{DIN\_}$ = high or low		-20		+20	µA
Power-Off Input Current	I_{INO}	$V_{DE\_}$, $V_{\overline{RE}\_}$, $V_{DIN\_}$ = 3.6V or 0V, V_{CC} = 0V or open		-20		+20	µA
SUPPLY							
Supply Current Drivers and Receivers Enabled	I_{CC}	DE_ = high, $\overline{RE}$_ = low, R_L = 27Ω			77	95	mA
Supply Current Drivers Enabled and Receivers Disabled	I_{CCD}	DE_ = high, $\overline{RE}$_ = high, R_L = 27Ω			77	95	mA
Supply Current Drivers Disabled and Receivers Enabled	I_{CCR}	DE_ = low, $\overline{RE}$_ = low			19.9	30	mA
Supply Current Drivers Disabled and Receivers Disabled	I_{CCZ}	DE_ = low, $\overline{RE}$_ = high			19.9	30	mA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 3.6V, R_L = 27Ω ±1%, receiver differential input voltage $|V_{ID}|$ = 0.15V to V_{CC}, receiver input voltage range = 0V to V_{CC}, input frequency to differential inputs = 100MHz, input frequency to LVCMOS/LVTTL inputs = 100MHz, LVCMOS/LVTTL inputs = 0V to V_{CC} with 2ns (10% to 90%) transition times. Differential input voltage transition time = 1ns (20% to 80%). Receiver input common-mode voltage V_{CM} = 0.075V to 2.4V, DE_ = high, $\overline{RE}$_ = low, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, and T_A = +25°C.) (Notes 3 and 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DRIVER						
Differential Propagation Delay High to Low	t_{PHLD}	$\overline{RE}$_ = high, C_L = 10pF, Figures 3, 4	1.2	1.96	2.5	ns
Differential Propagation Delay Low to High	t_{PLHD}	$\overline{RE}$_ = high, C_L = 10pF, Figures 3, 4	1.1	1.87	2.4	ns
Differential Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$ (Note 6)	t_{SKD1}	$\overline{RE}$_ = high, C_L = 10pF, Figures 3, 4		91	250	ps
Channel-to-Channel Skew (Note 7)	t_{CCSK}	$\overline{RE}$_ = high, C_L = 10pF, Figures 3, 4		119	350	ps
Chip-to-Chip Skew (Note 8)	t_{SKD2}	$\overline{RE}$_ = high, C_L = 10pF, Figures 3, 4		0.45	0.90	ns
Chip-to-Chip Skew (Note 9)	T_{SKD3}	$\overline{RE}$_ = high, C_L = 10pF, Figures 3, 4			1.4	ns
Rise Time	t_{TLH}	$\overline{RE}$_ = high, C_L = 10pF, Figures 3, 4	0.6	1.07	1.4	ns
Fall Time	t_{THL}	$\overline{RE}$_ = high, C_L = 10pF, Figures 3, 4	0.6	1.10	1.4	ns
Disable Time High to Z	t_{PHZ}	$\overline{RE}$_ = high, C_L = 10pF, Figures 5, 6		2.8	5	ns
Disable Time Low to Z	t_{PLZ}	$\overline{RE}$_ = high, C_L = 10pF, Figures 5, 6		2.8	5	ns
Enable Time Z to High	t_{PZH}	$\overline{RE}$_ = high, C_L = 10pF, Figures 5, 6		4.6	6	ns
Enable Time Z to Low	t_{PZL}	$\overline{RE}$_ = high, C_L = 10pF, Figures 5, 6		4.5	6	ns
Maximum Operating Frequency (Note 10)	f_{MAX}	$\overline{RE}$_ = high, C_L = 10pF, Figures 5, 6	100			MHz
RECEIVER						
Differential Propagation Delay High to Low	t_{PHLD}	DE_ = low, Figures 7, 8; C_L = 15pF	1.5	2.21	3.5	ns
Differential Propagation Delay Low to High	t_{PLHD}	DE_ = low, Figures 7, 8; C_L = 15pF	1.5	2.13	3.5	ns
Differential Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$ (Note 6)	t_{SKD1}	DE_ = low, Figures 7, 8; C_L = 15pF		74	250	ps
Channel-to-Channel Skew (Note 7)	t_{CCSK}	DE_ = low, Figures 7, 8; C_L = 15pF		96	350	ps
Chip-to-Chip Skew (Note 8)	t_{SKD2}	DE_ = low, Figures 7, 8; C_L = 15pF		0.63	1.6	ns
Chip-to-Chip Skew (Note 9)	t_{SKD3}	DE_ = low, Figures 7, 8; C_L = 15pF			2.0	ns
Rise Time	t_{TLH}	DE_ = low, Figures 7, 8; C_L = 15pF	0.5	1.09	1.6	ns

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.0V to 3.6V, R_L = 27Ω ±1%, receiver differential input voltage $|V_{ID}|$ = 0.15V to V_{CC}, receiver input voltage range = 0V to V_{CC}, input frequency to differential inputs = 100MHz, input frequency to LVCMOS/LVTTL inputs = 100MHz, LVCMOS/LVTTL inputs = 0V to V_{CC} with 2ns (10% to 90%) transition times. Differential input voltage transition time = 1ns (20% to 80%). Receiver input common-mode voltage V_{CM} = 0.075V to 2.4V, DE_ = high, $\overline{RE}$_ = low, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, and T_A = +25°C.) (Notes 3 and 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Fall Time	t_{THL}	DE_ = low, Figures 7, 8, C_L = 15pF	0.7	1.24	1.8	ns
Disable Time High to Z	t_{PHZ}	DE_ = low, R_L = 500Ω, C_L = 15pF, Figures 9, 10		6.0	8	ns
Disable Time Low to Z	t_{PLZ}	DE_ = low, R_L = 500Ω, C_L = 15pF, Figures 9, 10		6.5	8	ns
Enable Time Z to High	t_{PZH}	DE_ = low, R_L = 500Ω, C_L = 15pF, Figures 9, 10		4.3	7	ns
Enable Time Z to Low	t_{PZL}	DE_ = low, R_L = 500Ω, C_L = 15pF, Figures 9, 10		4.3	7	ns
Maximum Operating Frequency (Note 10)	f_{MAX}	DE_ = low, C_L = 15pF	100			MHz

Note 1: Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except V_{TH}, V_{TL}, V_{ID}, V_{OD}, and ΔV_{OD}.

Note 2: Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are production tested at T_A = +25°C.

Note 3: Guaranteed by design and characterization.

Note 4: Short only one output at a time. Do not exceed the absolute maximum junction temperature specification.

Note 5: C_L includes scope probe and test fixture capacitance.

Note 6: t_{SKD1} is the magnitude difference of differential propagation delays in a channel. $t_{SKD1} = | t_{PHLD} - t_{PLHD} |$.

Note 7: t_{CCSK} is the magnitude difference of the t_{PLHD} or t_{PHLD} of one channel and the t_{PLHD} or t_{PHLD} of any other channel on the same part.

Note 8: t_{SKD2} is the magnitude difference of any differential propagation delays between parts operating over rated conditions at the same V_{CC} and within 5°C of each other.

Note 9: t_{SKD3} is the magnitude difference of any differential propagation delays between parts operating over rated conditions.

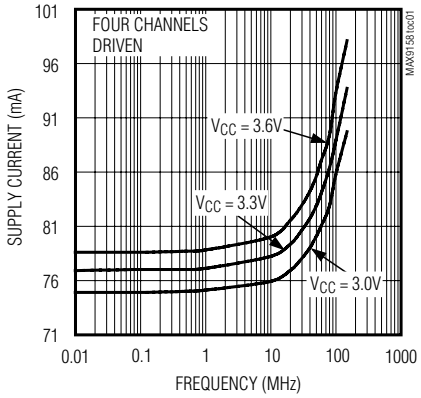
Note 10: Meets data sheet specifications while operating at minimum f_{MAX} rating.

Quad Bus LVDS Transceiver in 44 QFN

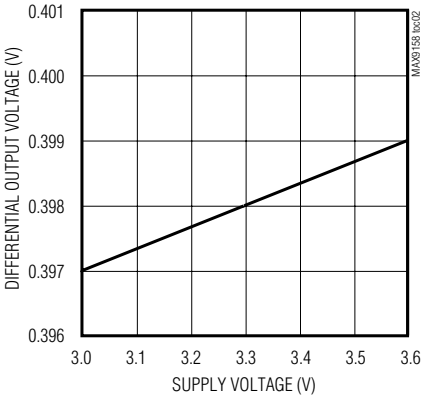
Typical Operating Characteristics

(V_{CC} = 3.3V, R_L = 27Ω, driver C_L = 10pF, receiver C_L = 15pF, $|V_{ID}|$ = 200mV, V_{CM} = 1.2V, f_{IN} = 20MHz, T_A = +25°C, unless otherwise noted.)

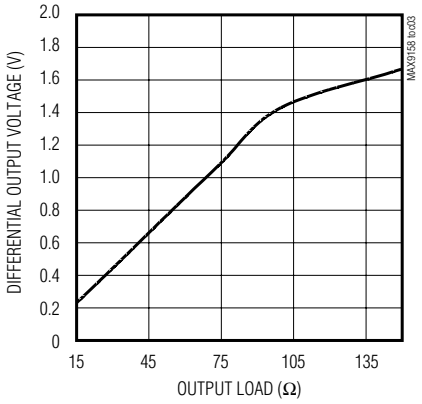
SUPPLY CURRENT vs. FREQUENCY



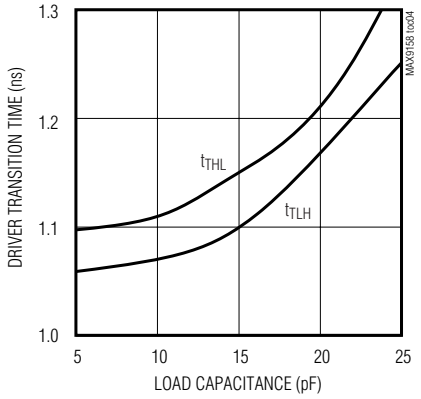
DIFFERENTIAL OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



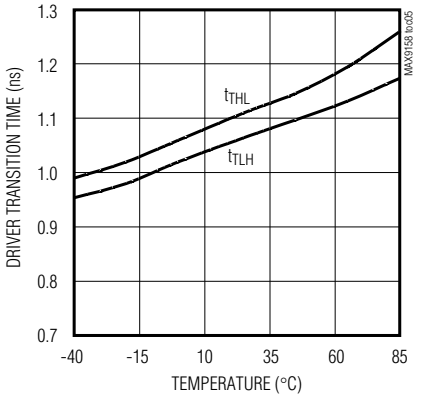
DIFFERENTIAL OUTPUT VOLTAGE vs. OUTPUT LOAD



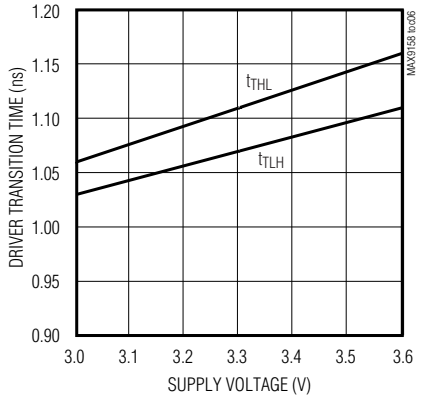
DRIVER TRANSITION TIME vs. LOAD CAPACITANCE



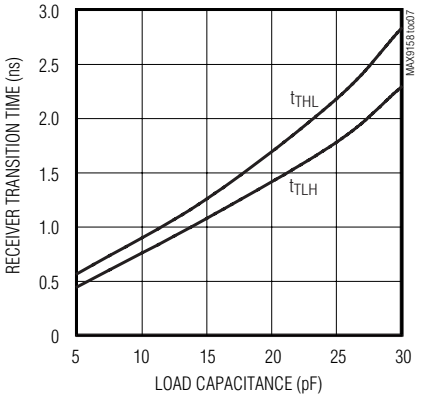
DRIVER TRANSITION TIME vs. TEMPERATURE



DRIVER TRANSITION TIME vs. SUPPLY VOLTAGE



RECEIVER TRANSITION TIME vs. LOAD CAPACITANCE



Pin Description

PIN	NAME	FUNCTION
1, 2, 11, 12, 23, 24, 32, 33, 34, 44	N.C.	No Connection. Not internally connected.
3, 6, 30	V_{CC}	Digital Power Supply
4, 28, 31, 39	GND	Digital Ground
5	$\overline{RE34}$	Receiver Channels 3 and 4 Enable (Enable Low). Drive $\overline{RE34}$ low to enable receiver channels 3 and 4. Internal pullup to V_{CC}.
7, 10, 22, 27	AV_{CC}	Analog Power Supply. Connect to board V_{CC}.
8	DE34	Driver Channels 3 and 4 Enable (Enable High). Drive DE34 high to enable driver channels 3 and 4. Internal pullup to V_{CC}.
9, 17, 25	AGND	Analog Ground. Connect to board ground.
13	DO4-/RIN4-	Channel 4 Inverting BLVDS Input/Output
14	DO4+/RIN4+	Channel 4 Noninverting BLVDS Input/Output
15	DO3-/RIN3-	Channel 3 Inverting BLVDS Input/Output
16	DO3+/RIN3+	Channel 3 Noninverting BLVDS Input/Output
18	DO2-/RIN2-	Channel 2 Inverting BLVDS Input/Output
19	DO2+/RIN2+	Channel 2 Noninverting BLVDS Input/Output
20	DO1-/RIN1-	Channel 1 Inverting BLVDS Input/Output
21	DO1+/RIN1+	Channel 1 Noninverting BLVDS Input/Output
26	DE12	Driver Channels 1 and 2 Enable (Enable High). Drive DE12 high to enable driver channels 1 and 2. Internal pullup to V_{CC}.
29	$\overline{RE12}$	Receiver Channels 1 and 2 Enable (Enable Low). Drive $\overline{RE12}$ low to enable receiver channels 1 and 2. Internal pullup to V_{CC}.
35	DIN1	Driver Channel 1 Input
36	RO1	Receiver Channel 1 Output
37	DIN2	Driver Channel 2 Input
38	RO2	Receiver Channel 2 Output
40	DIN3	Driver Channel 3 Input
41	RO3	Receiver Channel 3 Output
42	DIN4	Driver Channel 4 Input
43	RO4	Receiver Channel 4 Output
EP	EXPOSED PAD	Exposed Pad. Solder exposed pad to GND.

Quad Bus LVDS Transceiver in 44 QFN

Detailed Description

The MAX9158 is a four-channel, 200Mbps, 3.3V BLVDS transceiver in a 44-lead QFN package, ideal for driving heavily loaded multipoint buses, typically 16 to 20 cards plugged into a backplane. The MAX9158 receivers accept a differential input and have a fail-safe input circuit. The devices detect differential signals as low as 100mV and as high as V_{CC}.

The MAX9158 driver outputs use a current-steering configuration to generate a 9.25mA to 17mA output current. This current-steering approach induces less ground bounce and no shoot-through current, enhancing noise margin and system speed performance. The outputs are short-circuit current limited.

The MAX9158 current-steering output requires a resistive load to terminate the signal and complete the transmission loop. Because the devices switch the direction of current flow and not voltage levels, the output voltage swing is determined by the value of the termination resistor multiplied by the output current. With a typical 14.75mA output current, the MAX9158 produces a 398mV output voltage when driving a bus terminated with two 54Ω resistors (14.75mA × 27Ω = 398mV). Logic states are determined by the direction of current flow through the termination resistor.

Fail-Safe Receiver Inputs

The fail-safe feature of the MAX9158 sets the receiver output high when the receiver differential input is:

- Open
- Undriven and shorted
- Undriven and terminated

Without a fail-safe circuit, when the input is undriven, noise at the input may switch the output and it may appear to the system that data is being received. Open or undriven terminated input conditions can occur when a cable is disconnected or cut, or when a driver is in high impedance. A shorted input can occur because of a cable failure.

When the input is driven with a differential signal with a common-mode voltage of 0.05V to 2.4V, the fail-safe circuit is not activated. If the input is open, undriven and shorted, or undriven and parallel terminated, an internal resistor in the fail-safe circuit pulls both inputs above V_{CC} - 0.3V, activating the fail-safe circuit and forcing the output high (Figure 1).

Effect of Capacitive Loading

The characteristic impedance of a differential PC board trace is uniformly reduced when equal capacitive loads are attached at equal intervals (provided the transition time of the signal being driven on the trace is longer than the delay between loads). This kind of loading is typical of multipoint buses where cards are attached at 1in or 0.8in intervals along the length of a backplane.

The reduction in characteristic impedance is approximated by the following formula:

$$Z_{DIFF}\text{-loaded} = Z_{DIFF}\text{-unloaded} \times \text{SQRT}\left[Co / (Co + N \times C_L / L)\right]$$

where:

Z_{DIFF}-unloaded = unloaded differential characteristic impedance

Co = unloaded trace capacitance (pF/unit length)

C_L = value of each capacitive load (pF)

N = number of capacitive loads

L = trace length

For example, if Co = 2.5pF/in, C_L = 10pF, N = 18, L = 18in, and Z_{DIFF}-unloaded = 120Ω, the loaded differential impedance is:

$$Z_{DIFF}\text{-loaded} = 120\Omega \times \text{SQRT}\left[2.5pF / (2.5pF + 18 \times 10pF / 18in)\right]$$

$$ZDIFF\text{-loaded} = 54\Omega$$

In this example, capacitive loading reduces the characteristic impedance from 120Ω to 54Ω. The load seen by

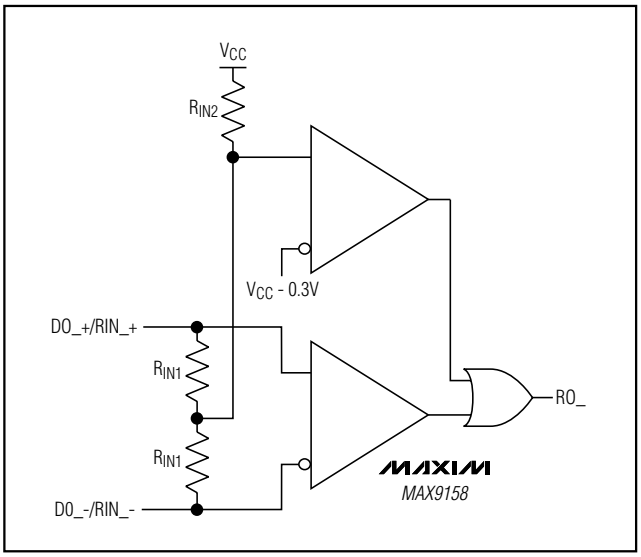


Figure 1. Internal Fail-Safe Circuit

a driver located on a card in the middle of the bus is 27Ω because the driver sees two 54Ω loads in parallel. A typical LVDS driver (rated for a 100Ω load) would not develop a large enough differential signal to be reliably detected by an LVDS receiver. The MAX9158 BLVDS drivers are designed and specified to drive a 27Ω load to differential voltage levels of 250mV to 460mV. A standard LVDS receiver is able to detect this level of differential signal. Short extensions off the bus, called stubs, contribute to capacitive loading. Keep stubs less than 1in for a good balance between ease of component placement and good signal integrity.

The MAX9158 driver outputs are current-source drivers and drive larger differential signal levels into loads lighter than 27Ω and smaller levels into loads heavier than 27Ω (see *Typical Operating Characteristics* curves). To keep loading from reducing bus impedance below the rated 27Ω load, PC board traces can be designed for higher unloaded characteristic impedance.

Effect of Transition Times

For transition times (measured from 0% to 100%) shorter than the delay between capacitive loads, the loads are seen as low-impedance discontinuities from which the driven signal is reflected. Reflections add and subtract from the signal being driven, causing jitter and decreased noise margin. The MAX9158 output drivers are designed for a minimum transition time of 1ns (rated 0.6ns from 20% to 80%, or 1ns from 0% to 100%) to reduce reflections while being fast enough for high-speed backplane data transmission.

Power-On Reset

The power-on reset voltage of the MAX9158 is typically 2.25V. When the supply falls below this voltage, the devices are disabled and the receiver inputs/driver outputs are in high impedance. The power-on reset ensures glitch-free power-up and power-down, allowing hot swapping of cards in a multicard bus system without disrupting communications.

Operating Modes

The MAX9158 features driver/receiver enable inputs that select the bus I/O function (Table 1). Tables 2 and 3 show the driver and receiver operating modes.

Input Internal Pullup/Pulldown Resistors

The MAX9158 includes pullup or pulldown resistors (300kΩ) to ensure that unconnected inputs are defined (Table 4).

Applications Information

Supply Bypassing

Bypass each supply pin with high-frequency surface-mount ceramic 0.1µF and 1nF capacitors in parallel as close to the device as possible, with the smaller value capacitor closest to the device.

Termination

In the example given in the *Effect of Capacitive Loading* section, the loaded differential impedance of a bus is reduced to 54Ω. Since the bus can be driven from any card position, the bus must be terminated at each end. A parallel termination of 54Ω at each end of the bus placed across the traces that make up the differential pair provides a proper termination. The total load seen by the driver is 27Ω. The MAX9158 drives higher differential signal levels into lighter loads. (See the Differential Output Voltage vs. Output Load graph in the *Typical Operating Characteristics* section.) A multidrop bus with the driver at one end and receivers connected at regular intervals along the bus has a lowered impedance due to capacitive loading. Assuming a 54Ω impedance, the multidrop bus can be terminated with a single, parallel-connected 54Ω resistor at the far end from the driver. Only a single resistor is required because the driver sees one 54Ω differential trace. The signal swing is larger with a 54Ω load. In general, parallel terminate each end of the bus with a resistor matching the differential impedance of the bus (taking into account any reduced impedance due to loading).

Table 1. I/O Enable Functional Table

MODE SELECTED	DE_	$\overline{RE\_}$
Driver Mode	H	H
Receiver Mode	L	L
High-Impedance Mode	L	H
Loopback Mode	H	L

Table 2. Driver Mode

INPUTS		OUTPUTS	
DE_	DIN_	DO_+/RIN_+	DO_-/RIN_-
H	L	L	H
H	H	H	L
L	X	Z	Z

Quad Bus LVDS Transceiver in 44 QFN

Table 3. Receiver Mode

INPUTS		OUTPUTS
$\overline{RE\_}$	$V_{ID} = (V_{DO\_+}/R_{IN\_+}) - (V_{DO\_-}/R_{IN\_-})$	RO_
L	V_{ID} < -100mV	L
L	V_{ID} > 100mV	H
L	Fail-safe operation guaranteed when DO_+/RIN_+ and DO_-/RIN_- are open, undriven and shorted, or undriven and parallel terminated	H
H	X	Z

Table 4. Input Internal Pullup/Pulldown Resistors

PIN	INTERNAL RESISTOR
DE12	Pullup to V_{CC}
DE34	Pullup to V_{CC}
$\overline{RE12}$	Pullup to V_{CC}
$\overline{RE34}$	Pullup to V_{CC}
DIN_	None (floating)

Traces, Cables, and Connectors

The characteristics of input and output connections affect the performance of the MAX9158. Use controlled-impedance traces, cables, and connectors with matched characteristic impedance.

Ensure that noise couples as common mode by running the traces of a differential pair close together. Reduce within-pair skew by matching the electrical length of the traces of a differential pair. Excessive skew can result in a degradation of magnetic field cancellation. Maintain the distance between traces of a differential pair to avoid discontinuities in differential impedance. Minimize the number of vias to further prevent impedance discontinuities.

Avoid the use of unbalanced cables, such as ribbon cable. Balanced cables, such as twisted pair, offer superior signal quality and tend to generate less EMI due to canceling effects. Balanced cables tend to pick up noise as common mode, which is rejected by the receiver.

Board Layout

A four-layer PC board that provides separate power, ground, input, and output signals is recommended. Keep the LVTTL/LVCMOS and BLVDS signals separated to prevent coupling.

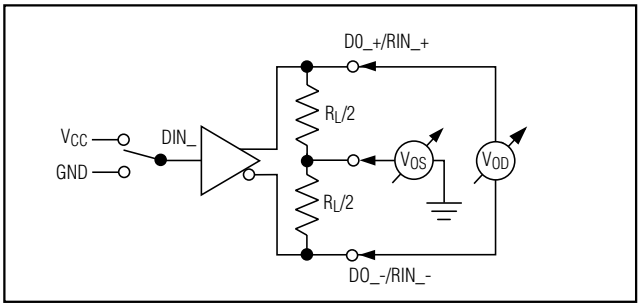


Figure 2. Driver V_{OD} and V_{OS} Test Circuit

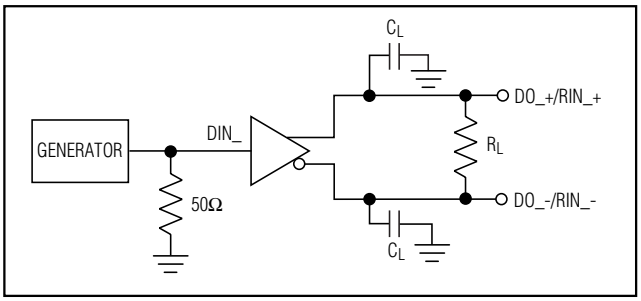


Figure 3. Driver Propagation Delay and Transition Time Test Circuit

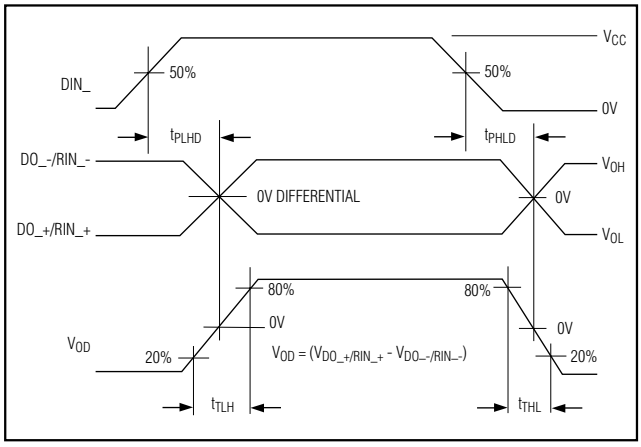


Figure 4. Driver Propagation Delay and Transition Time Waveforms

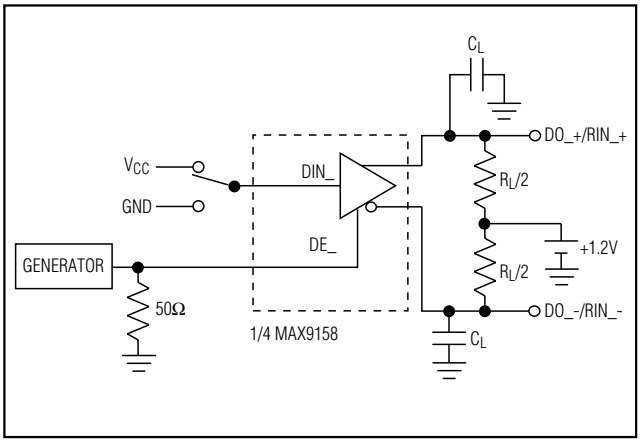


Figure 5. Driver High-Impedance Delay Test Circuit

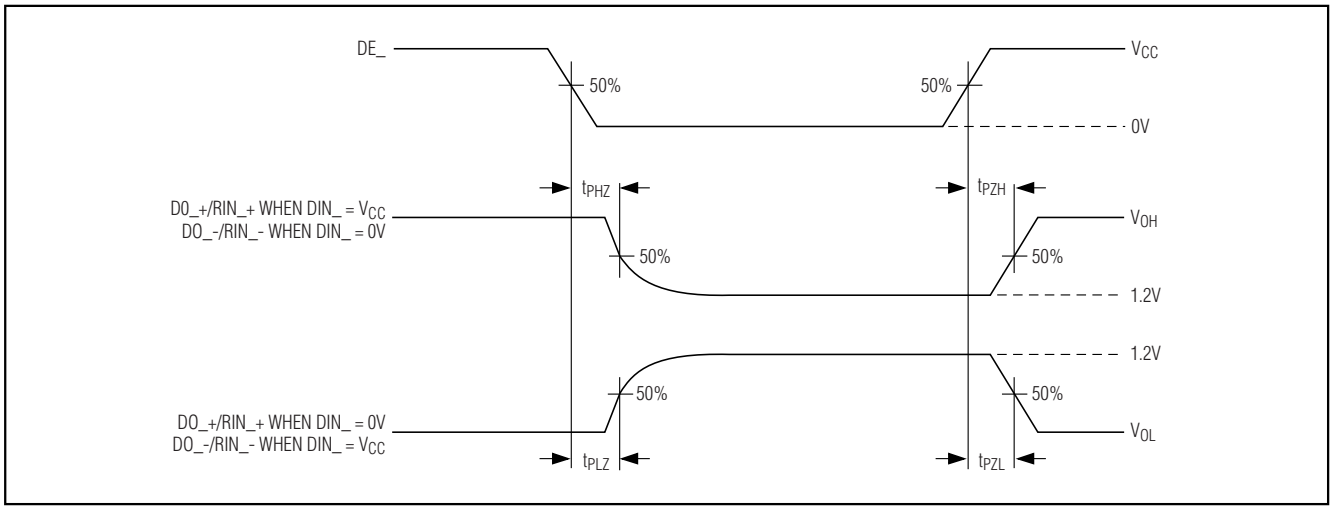


Figure 6. Driver High-Impedance Delay Waveform

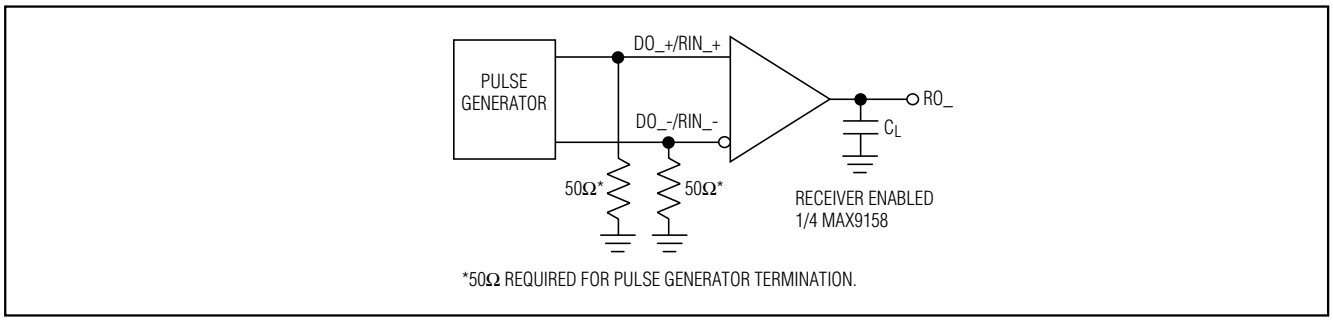


Figure 7. Receiver Transition Time and Propagation Delay Test Circuit

Quad Bus LVDS Transceiver in 44 QFN

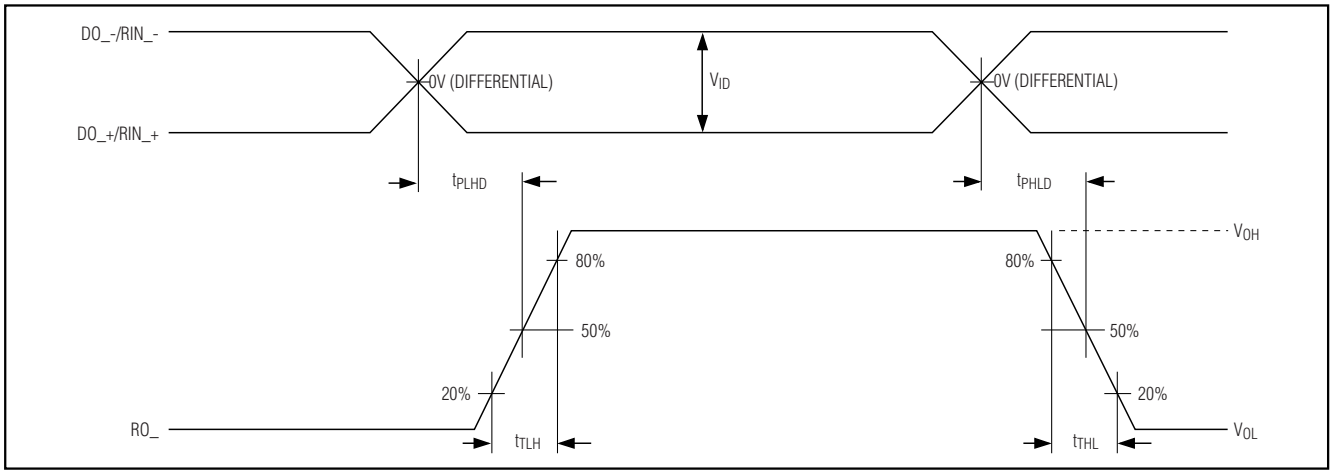


Figure 8. Receiver Transition Time and Propagation Delay Timing Diagram

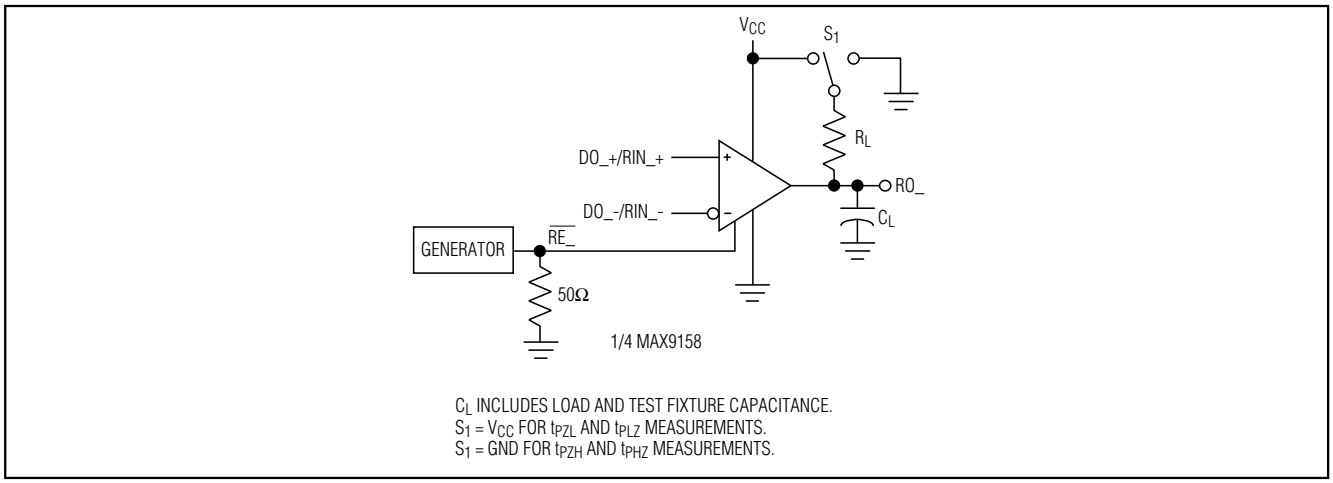


Figure 9. Receiver High-Impedance Delay Test Circuit

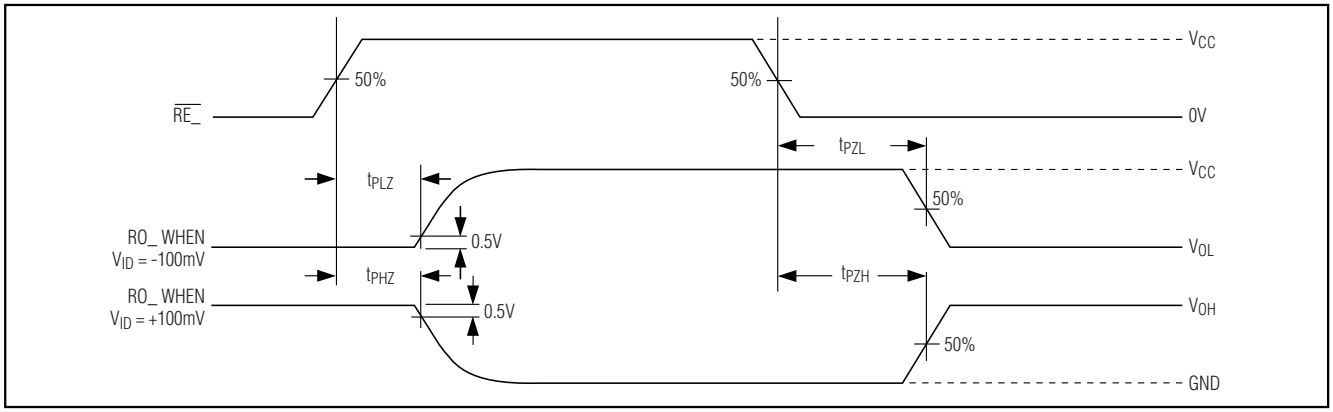
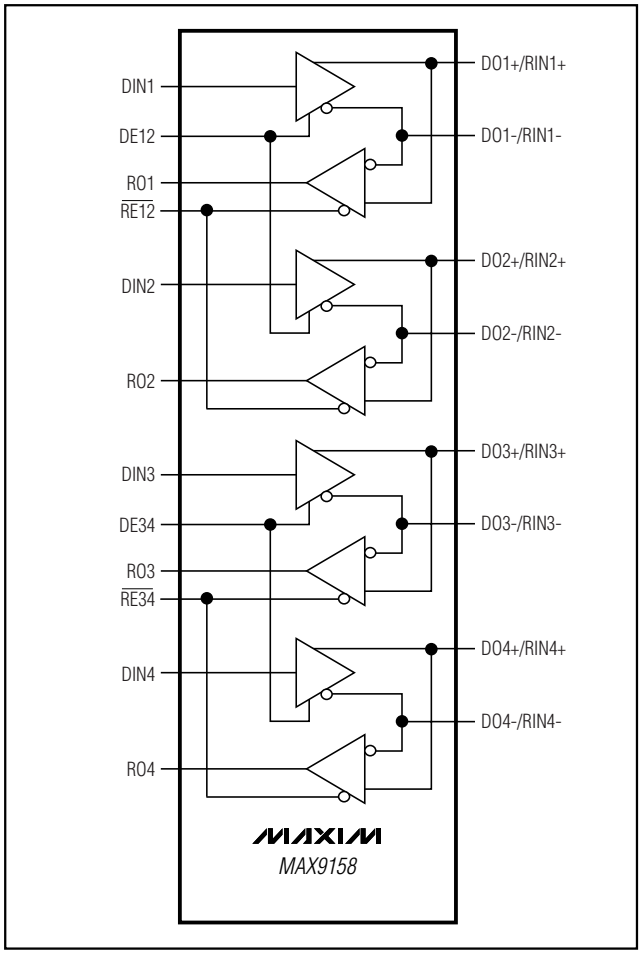


Figure 10. Receiver High-Impedance Waveforms

Functional Diagram



Chip Information

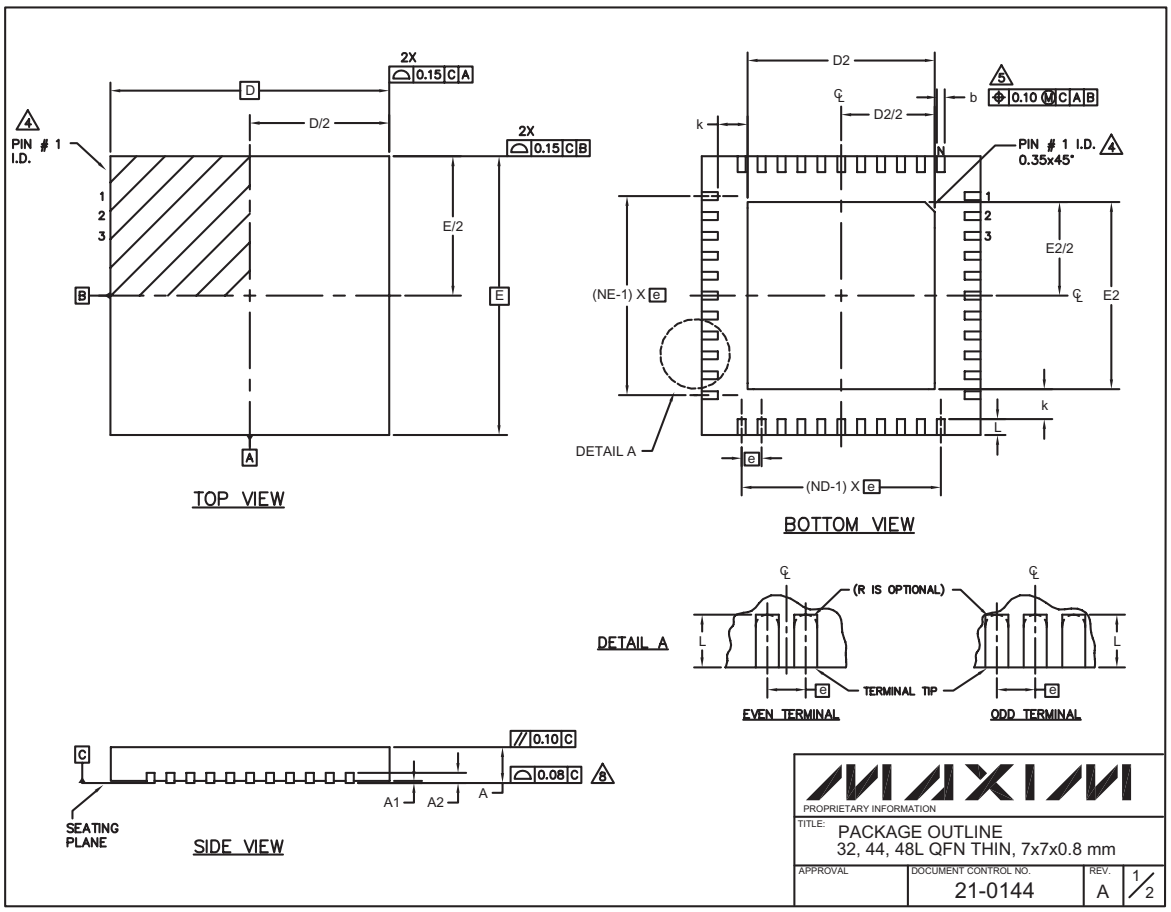
TRANSISTOR COUNT: 1796

PROCESS: CMOS

Quad Bus LVDS Transceiver in 44 QFN

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS

PKG	32L 7x7			44L 7x7			48L 7x7			CUSTOM PKG. (T4877-1) 48L 7x7		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.20	0.25	0.30
D	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
E	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.45	0.55	0.65
N	32			44			48			44		
ND	8			11			12			10		
NE	8			11			12			12		

EXPOSED PAD VARIATIONS

PKG. CODES	DEPOPULATED LEADS	D2			E2			JEDEC MO220 REV. C
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T3277-1	-	4.55	4.70	4.85	4.55	4.70	4.85	-
T4477-1	-	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1
T4877-1**	13, 24, 37, 48	4.20	4.30	4.40	4.20	4.30	4.40	-
T4877-2	-	5.45	5.60	5.75	5.45	5.60	5.75	WKKD-2

** NOTE: T4877-1 IS A CUSTOM 48L PKG. WITH 4 LEADS DEPOPULATED. TOTAL NUMBER OF LEADS ARE 44.

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95–1 SPP–012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE 32, 44, 48L QFN THIN, 7x7x0.8 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0144	A	2/2