FOR NEW DESIGNS, INTERSIL RECOMMENDS THE HI5767/4CB OR HI5746KCB

November 1998 File Number 3950.7

10-Bit, 40 MSPS A/D Converter

The HI5703 is a monolithic, 10-bit, analog-to-digital converter fabricated in Intersil's BiCMOS process. It is designed for high speed applications where wide bandwidth and low power consumption are essential. Its 40 MSPS speed is made possible by a fully differential pipeline architecture with an internal sample and hold.

The HI5703 has excellent dynamic performance while consuming only 400mW power at 40 MSPS. Data output latches are provided which present valid data to the output bus with a latency of 7 clock cycles. It is pin-to-pin compatible with the HI5702.

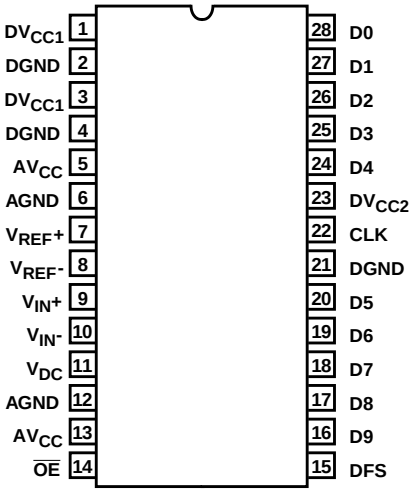
For lower power consumption or internal reference, please refer to the HI5746 or HI5767.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI5703KCB	0 to 70	28 Ld SOIC (W)	M28.3
HI5703EVAL	25	Evaluation Board	

Pinout

HI5703
(SOIC)
TOP VIEW



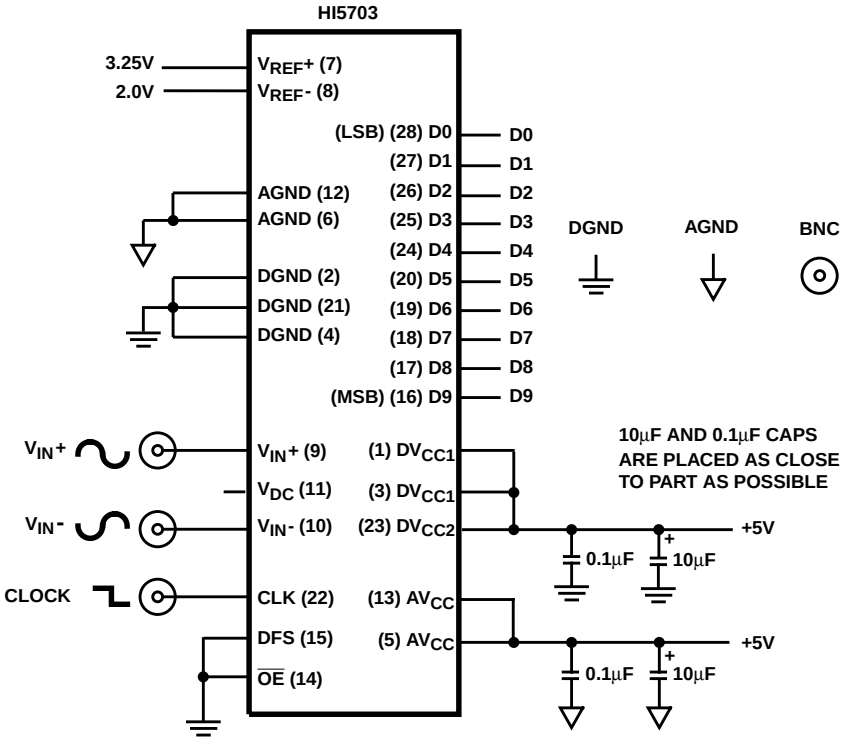
Features

- Sampling Rate . . . . . 40 MSPS
- 8.55 Bits Guaranteed at f_{IN} = 10MHz
- Low Power
- Wide Full Power Input Bandwidth. 250MHz
- On Chip Sample and Hold
- Fully Differential or Single-Ended Analog Input
- Single Supply Voltage. . . . . +5V
- TTL Compatible Interface
- 3.3V Digital Outputs Available

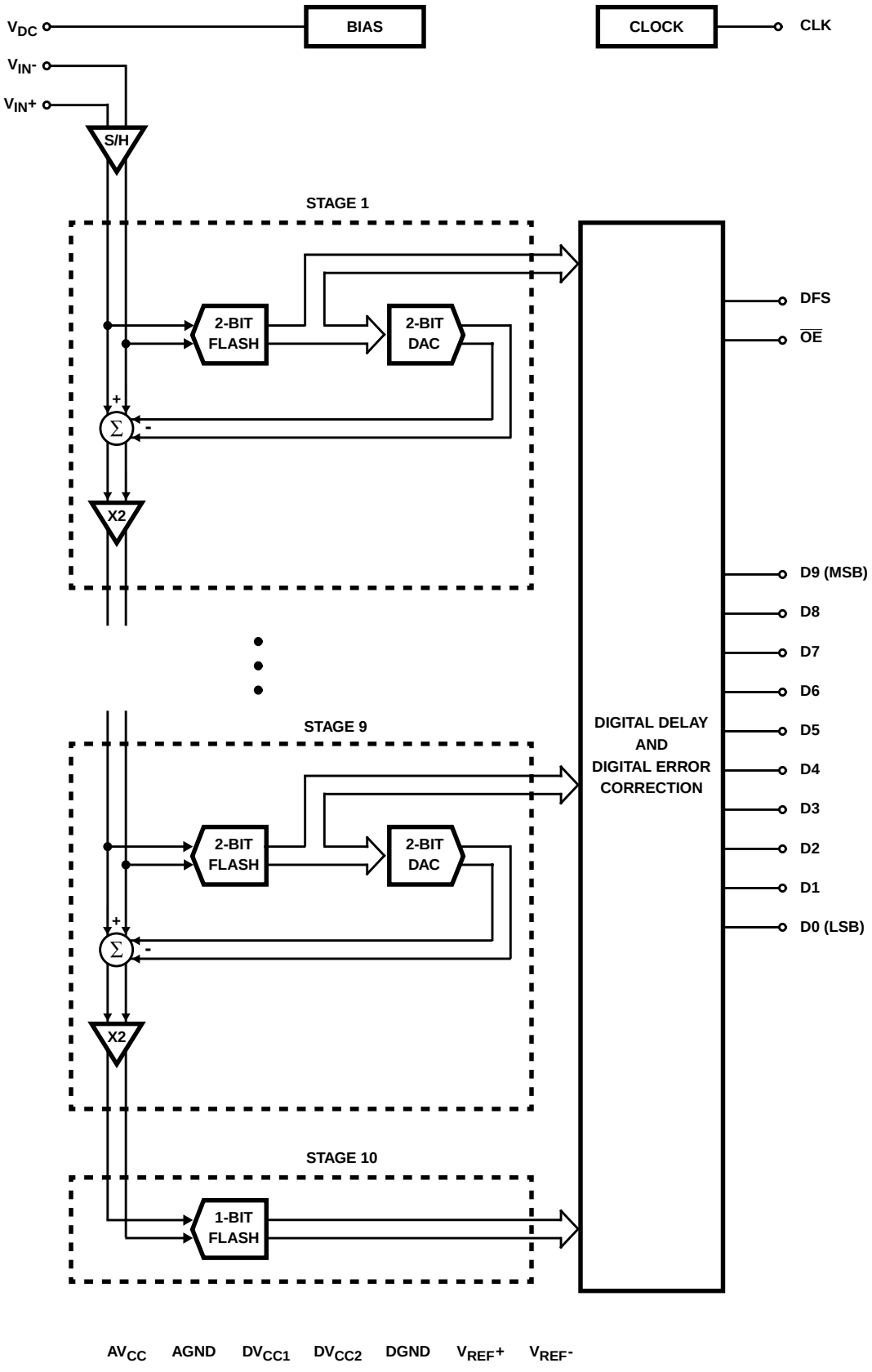
Applications

- Professional Video Digitizing
- Medical Imaging
- Digital Communication Systems
- High Speed Data Acquisition
- Additional Reference Documents
  - AN9534 Using the HI5703 Evaluation Board
  - AN9413 Driving the Analog Input of the HI5702
  - AN9214 Using Intersil High Speed A/D Converters

Typical Application Schematic



Functional Block Diagram



Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage, AV_{CC} or DV_{CC} to AGND or DGND . . . . . +6V
DGND to AGND 0.3V
Digital I/O Pins . . . . . DGND to DV_{CC}
Analog I/O Pins . . . . . AGND to AV_{CC}

Operating Conditions

Temperature Range, HI5703KCB . . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
SOIC Package	70

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$AV_{CC} = DV_{CC1} = DV_{CC2} = +5.0V$; $V_{REF}+ = 3.25V$; $V_{REF}- = 2.0V$; $f_S = 36$ MSPS at 50% Duty Cycle; $C_L = 20pF$; $T_A = 25^oC$; Differential Analog Input; Unless Otherwise Specified

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
ACCURACY					
Resolution		10	-	-	Bits
Integral Linearity Error, INL	f_{IN} = DC	-	±1	±2.0	LSB
Differential Linearity Error, DNL (Guaranteed No Missing Codes)	f_{IN} = DC	-	±0.5	±1	LSB
Offset Error, V_{OS}	f_{IN} = DC	-	4	-	LSB
Full Scale Error, FSE	f_{IN} = DC	-	1	-	LSB
DYNAMIC CHARACTERISTICS					
Minimum Conversion Rate	No Missing Codes	-	0.5	1	MSPS
Maximum Conversion Rate	No Missing Codes	40	-	-	MSPS
Effective Number of Bits, ENOB	f_{IN} = 1MHz	-	9.2	-	Bits
	f_{IN} = 5MHz	-	9.2	-	Bits
	f_{IN} = 10MHz	8.55	8.9	-	Bits
Signal to Noise and Distortion Ratio, SINAD = $\frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	f_{IN} = 1MHz	-	57	-	dB
	f_{IN} = 5MHz	-	57	-	dB
	f_{IN} = 10MHz	53.2	55	-	dB
Signal to Noise Ratio, SNR = $\frac{\text{RMS Signal}}{\text{RMS Noise}}$	f_{IN} = 1MHz	-	58	-	dB
	f_{IN} = 5MHz	-	58	-	dB
	f_{IN} = 10MHz	53.2	57	-	dB
Total Harmonic Distortion, THD	f_{IN} = 1MHz	-	-64	-	dBc
	f_{IN} = 5MHz	-	-63	-	dBc
	f_{IN} = 10MHz	-	-60	-	dBc
2nd Harmonic Distortion	f_{IN} = 1MHz	-	-75	-	dBc
	f_{IN} = 5MHz	-	-75	-	dBc
	f_{IN} = 10MHz	-	-73	-	dBc
3rd Harmonic Distortion	f_{IN} = 1MHz	-	-66	-	dBc
	f_{IN} = 5MHz	-	-64	-	dBc
	f_{IN} = 10MHz	-	-63	-	dBc

Electrical Specifications

$AV_{CC} = DV_{CC1} = DV_{CC2} = +5.0V$; $V_{REF}+ = 3.25V$; $V_{REF}- = 2.0V$; $f_S = 36$ MSPS at 50% Duty Cycle; $C_L = 20pF$; $T_A = 25^oC$; Differential Analog Input; Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Spurious Free Dynamic Range, SFDR	f_{IN} = 1MHz	-	66	-	dBc
	f_{IN} = 5MHz	-	64	-	dBc
	f_{IN} = 10MHz	54	63	-	dBc
Intermodulation Distortion, IMD	f_1 = 1MHz, f_2 = 1.02MHz	-	-59	-	dBc
Differential Gain Error	f_S = 17.72MHz, 6 Step, Mod Ramp	-	0.5	-	%
Differential Phase Error	f_S = 17.72MHz, 6 Step, Mod Ramp	-	0.1	-	Degree
Transient Response		-	1	-	Cycle
Over-Voltage Recovery	0.2V Overdrive	-	1	-	Cycle
ANALOG INPUT					
Maximum Peak-to-Peak Differential Analog Input Range ($V_{IN+} - V_{IN-}$)		-	±1.25	-	V
Maximum Peak-to-Peak Single-Ended Analog Input Range		-	2.5	-	V
Analog Input Resistance, R_{IN}	(Note 3)	-	1	-	MΩ
Analog Input Capacitance, C_{IN}		-	7	-	pF
Analog Input Bias Current, I_B+ or I_B-	(Note 3)	-10	-	+10	µA
Differential Analog Input Bias Current $I_{B\ DIFF} = (I_{B+} - I_B-)$		-	±0.5	-	µA
Analog Input Common Mode Voltage Range ($V_{IN}+ + V_{IN}-$) / 2	Differential Mode (Note 1)	0.625	-	4.375	V
Full Power Input Bandwidth (FPBW)		-	250	-	MHz
REFERENCE INPUT					
Total Reference Resistance, R_L		300	400	500	Ω
Reference Current		2.5	3.125	4.2	mA
Positive Reference Voltage Input, $V_{REF}+$	(Note 2)	-	3.25	3.3	V
Negative Reference Voltage Input, $V_{REF}-$	(Note 2)	1.95	2.0	-	V
Reference Common Mode Voltage ($V_{REF}+ + V_{REF}-$) / 2	(Note 2)	2.575	2.625	2.675	V
DC BIAS VOLTAGE					
DC Bias Voltage Output, V_{DC}		-	2.8	-	V
Max Output Current		-	-	1	mA
DIGITAL INPUTS					
Input Logic High Voltage, V_{IH}		2.0	-	-	V
Input Logic Low Voltage, V_{IL}		-	-	0.8	V
Input Logic High Current, I_{IH}	V_{IH} = 5V	-	-	10.0	µA
Input Logic Low Current, I_{IL}	V_{IL} = 0V	-	-	10.0	µA
Input Capacitance, C_{IN}		-	7	-	pF
DIGITAL OUTPUTS					
Output Logic Sink Current, I_{OL}	$V_O = 0.4V$; $DV_{CC2} = 5V$	1.6	-	-	mA
Output Logic Source Current, I_{OH}	$V_O = 2.4V$; $DV_{CC2} = 5V$	-0.2	-	-	mA
Output Three-State Leakage Current, I_{OZ}	$V_O = 0/5V$; $DV_{CC2} = 5V$	-	±1	±10	µA
Output Logic Sink Current, I_{OL}	$V_O = 0.4V$; $DV_{CC2} = 3.3V$	1.6	-	-	mA
Output Logic Source Current, I_{OH}	$V_O = 2.4V$; $DV_{CC2} = 3.3V$	-0.2	-	-	mA
Output Three-State Leakage Current, I_{OZ}	$V_O = 0/3.3V$; $DV_{CC2} = 3.3V$	-	±1	±10	µA
Output Capacitance, C_{OUT}		-	5	-	pF

Electrical Specifications

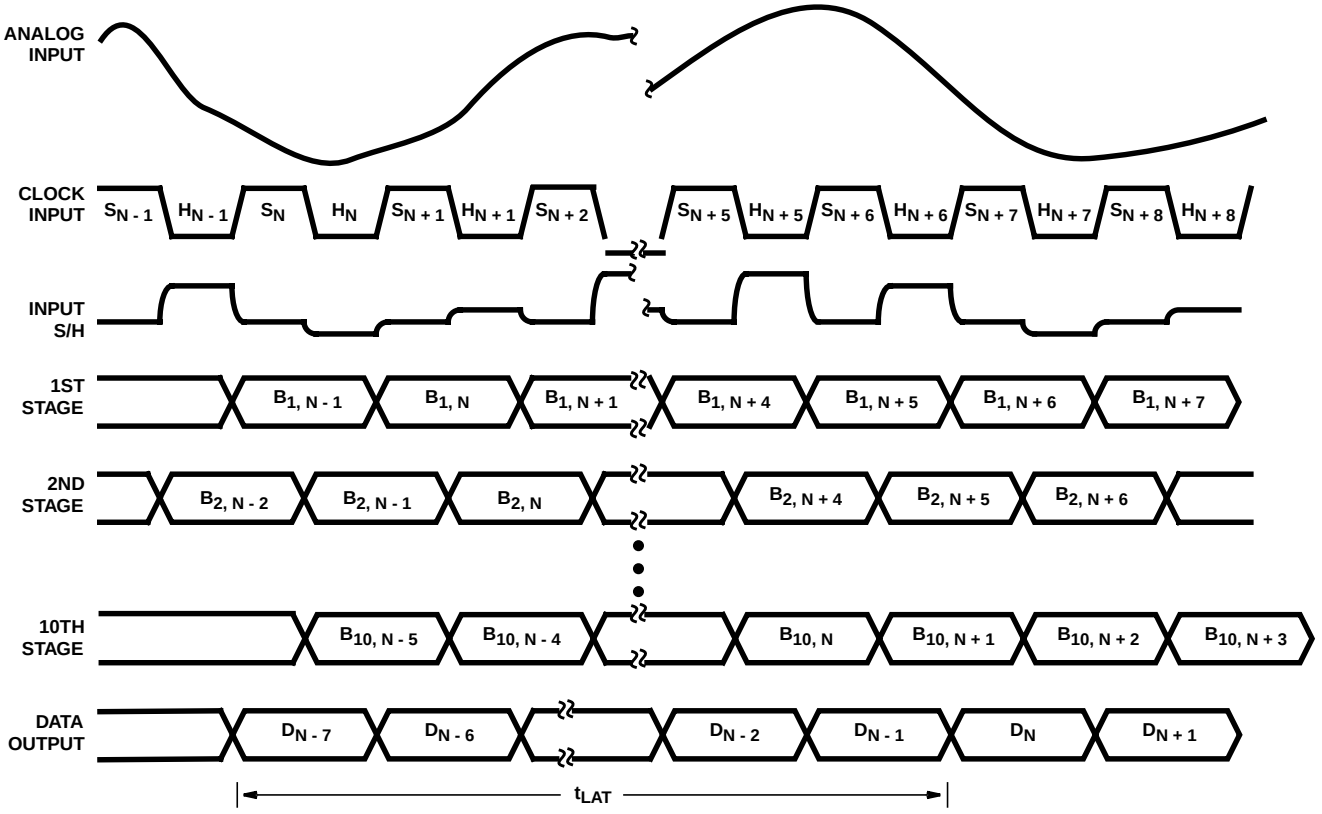
$AV_{CC} = DV_{CC1} = DV_{CC2} = +5.0V$; $V_{REF}+ = 3.25V$; $V_{REF}- = 2.0V$; $f_S = 36$ MSPS at 50% Duty Cycle; $C_L = 20pF$; $T_A = 25^oC$; Differential Analog Input; Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS					
Aperture Delay, t_{AP}		-	5	-	ns
Aperture Jitter, t_{AJ}		-	5	-	ps
Data Output Delay, t_{OD}		-	7	-	ns
	$AV_{CC} = DV_{CC1} = 5V \pm 10\%$, $DV_{CC2} = 3.3V \pm 5\%$, $0^oC \le T_A \le 70^oC$	5	7	18	ns
Data Output Hold, t_H		-	4	-	ns
Data Output Enable Time, t_{EN}		-	7	-	ns
Data Output Enable Time, t_{DIS}		-	7	-	ns
Clock Pulse Width (Low)	40 MSPS Clock	11.875	12.5	13.125	ns
Clock Pulse Width (High)	40 MSPS Clock	11.875	12.5	13.125	ns
Data Latency, t_{LAT}	For a Valid Sample (Note 2)	-	-	7	Cycles
Power-Up Initialization	Data Invalid Time (Note 2)	-	-	20	Cycles
POWER SUPPLY CHARACTERISTICS					
Analog Supply Voltage, AV_{CC}		4.75	5.0	5.25	V
Digital Supply Voltage, DV_{CC1}		4.75	5.0	5.25	V
Digital Output Supply Voltage, DV_{CC2}	At 3.30V	3.135	3.3	3.465	V
	At 5.0V	4.75	5.0	5.25	V
Total Supply Current, I_{CC}	$V_{IN}+ - V_{IN}- = +1.25V$ and DFS = “0”	-	80	-	mA
Analog Supply Current, AI_{CC}	$V_{IN}+ - V_{IN}- = +1.25V$ and DFS = “0”	-	48	-	mA
Digital Supply Current, DI_{CC1}	$V_{IN}+ - V_{IN}- = +1.25V$ and DFS = “0”	-	30	-	mA
Digital Output Supply Current, DI_{CC2}	$V_{IN}+ - V_{IN}- = +1.25V$ and DFS = “0”	-	2	-	mA
Power Dissipation	$V_{IN}+ - V_{IN}- = +1.25V$ and DFS = “0”	-	400	-	mW
Offset Error Sensitivity, ΔV_{OS}	AV_{CC} or $DV_{CC} = 5V \pm 5\%$	-	±1.5	-	LSB
Full Scale Error Sensitivity, ΔFSE	AV_{CC} or $DV_{CC} = 5V \pm 5\%$	-	±0.2	-	LSB

NOTES:

2. Parameter guaranteed by design or characterization and not production tested.
3. With the clock low and DC input.

Timing Waveforms



NOTES:

4. S_N: N-th sampling period.
5. H_N: N-th holding period.
6. $B_{M, N}$: M-th stage digital output corresponding to N-th sampled input.
7. D_N: Final data output corresponding to N-th sampled input.

FIGURE 1. HI5703 INTERNAL CIRCUIT TIMING

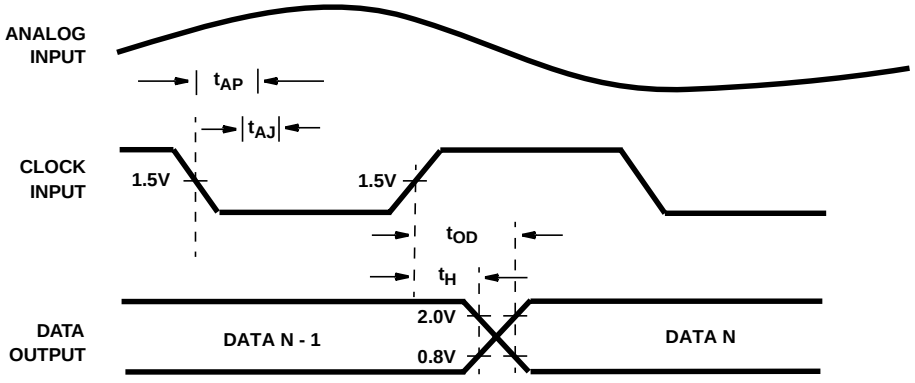


FIGURE 2. INPUT-TO-OUTPUT TIMING

Typical Performance Curves

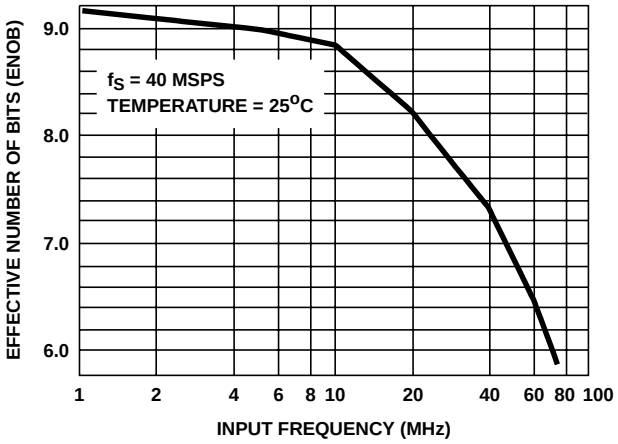
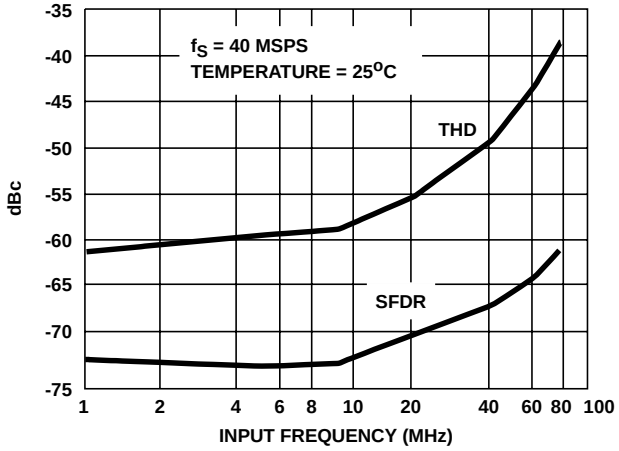


FIGURE 3. EFFECTIVE NUMBER OF BITS (ENOB) vs INPUT FREQUENCY



NOTE: SFDR depicted here does not include any harmonic distortion.

FIGURE 4. TOTAL HARMONIC DISTORTION (THD) AND SPURIOUS FREE DYNAMIC RANGE (SFDR) vs INPUT FREQUENCY

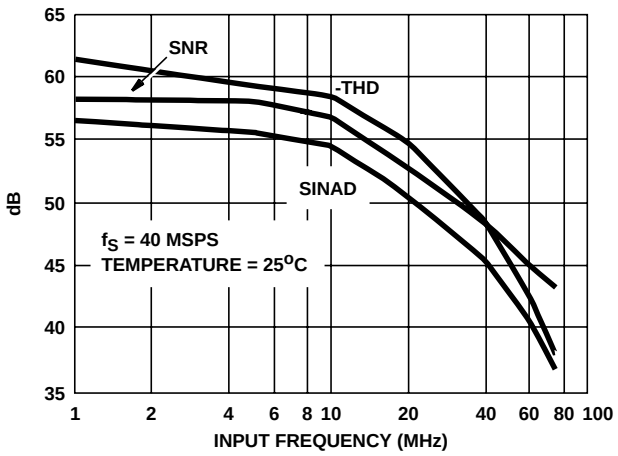


FIGURE 5. SINAD, SNR, AND -THD vs INPUT FREQUENCY

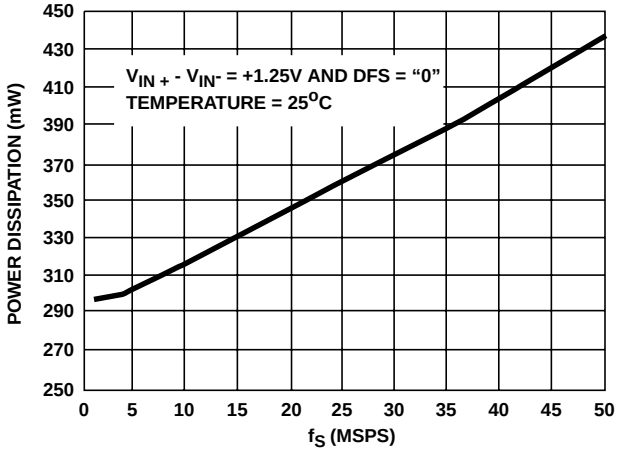


FIGURE 6. POWER DISSIPATION vs SAMPLE FREQUENCY

Typical Performance Curves (Continued)

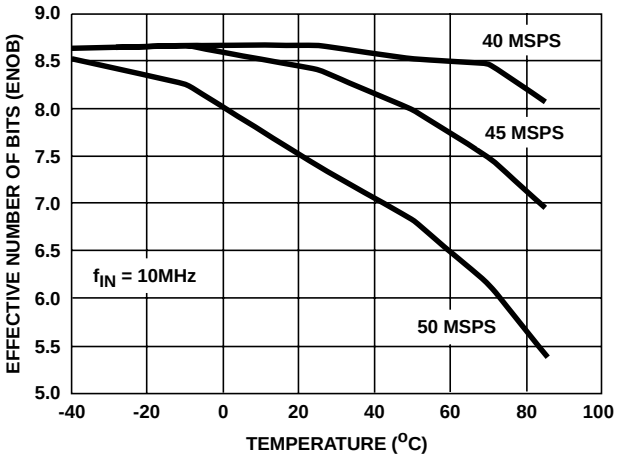


FIGURE 7. EFFECTIVE NUMBER OF BITS (ENOB) vs TEMPERATURE AND SAMPLE FREQUENCY

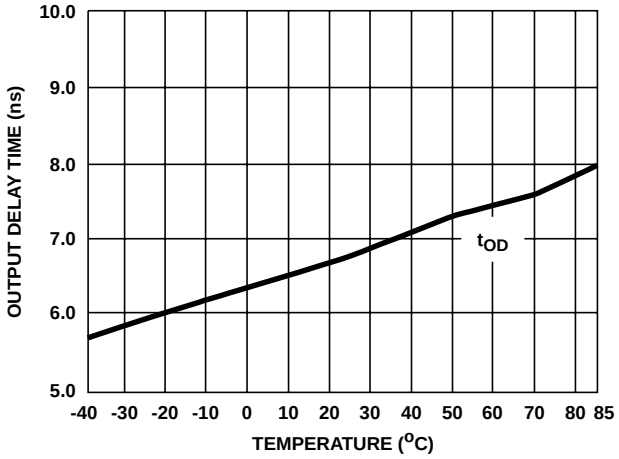


FIGURE 8. OUTPUT DELAY TIME (T_{OD}) vs TEMPERATURE

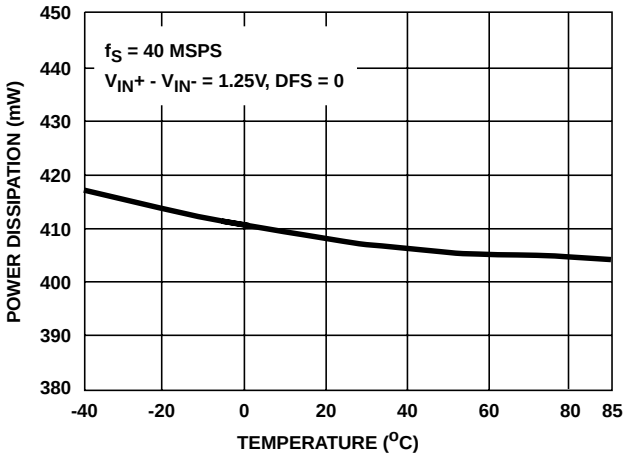


FIGURE 9. POWER DISSIPATION vs TEMPERATURE

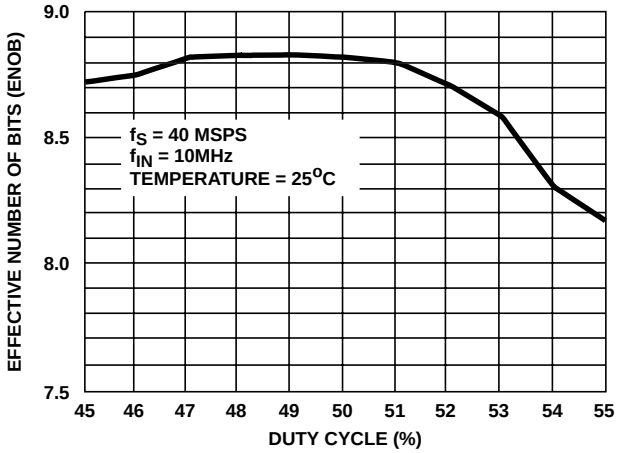


FIGURE 10. EFFECTIVE NUMBER OF BITS (ENOB) vs DUTY CYCLE (T_H/T_{TOTAL})

Typical Performance Curves (Continued)

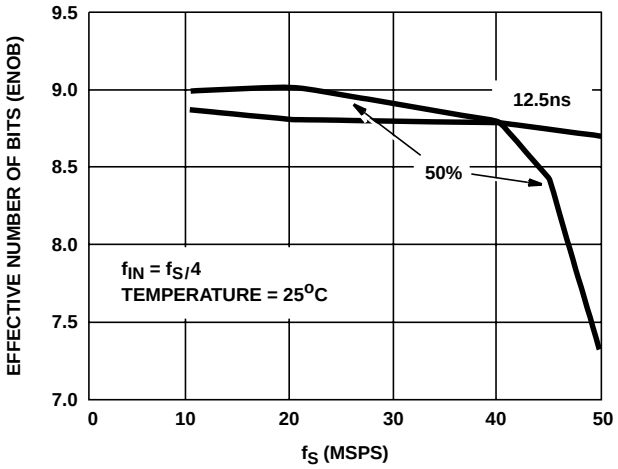


FIGURE 11. EFFECTIVE NUMBER OF BITS (ENOB) vs SAMPLE FREQUENCY

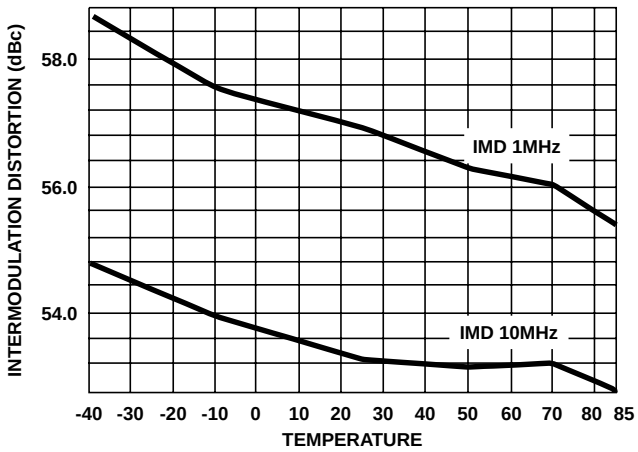


FIGURE 12. INTERMODULATION DISTORTION (IMD) vs TEMPERATURE

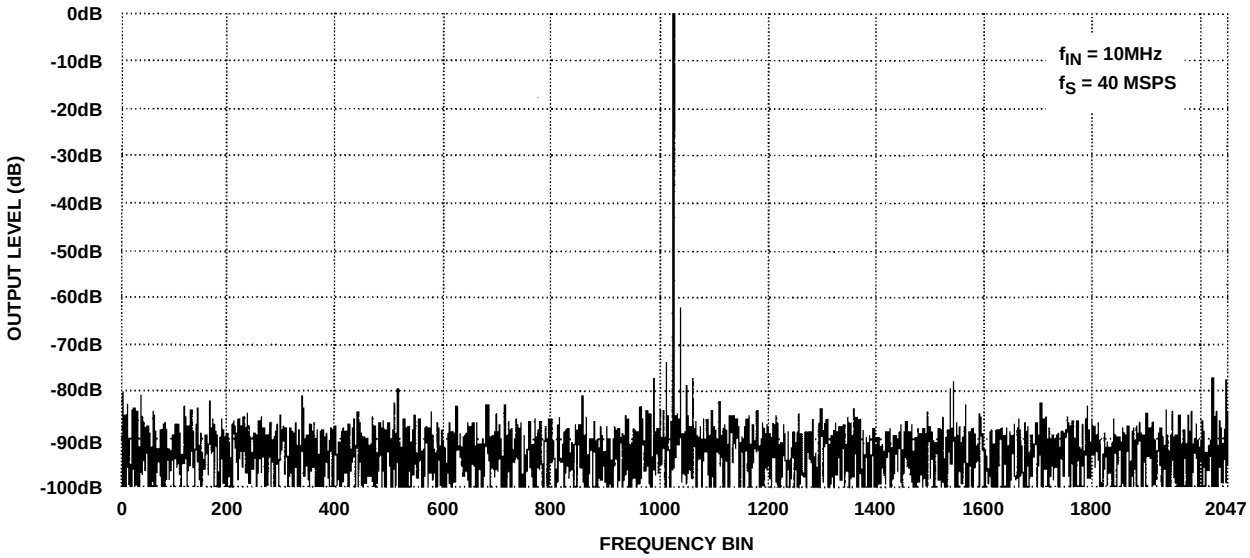


FIGURE 13. 4096 POINT FFT SPECTRAL PLOT

Typical Performance Curves (Continued)

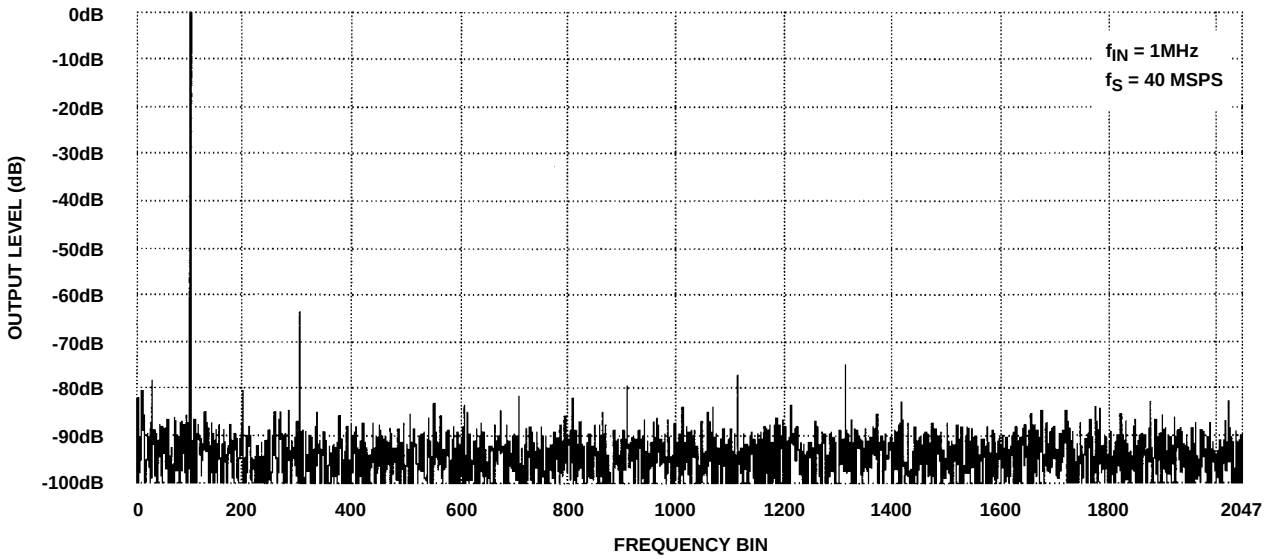


FIGURE 14. 4096 POINT FFT SPECTRAL PLOT

TABLE 1. PIN DESCRIPTION

PIN #	NAME	DESCRIPTION
1	DV_{CC1}	Digital Supply (+5.0V)
2	DGND	Digital Ground
3	DV_{CC1}	Digital Supply (+5.0V)
4	DGND	Digital Ground
5	AV_{CC}	Analog Supply (+5.0V)
6	AGND	Analog Ground
7	$V_{REF}+$	Positive Reference Voltage Input
8	$V_{REF}-$	Negative Reference Voltage Input
9	$V_{IN}+$	Positive Analog Input
10	$V_{IN}-$	Negative Analog Input
11	V_{DC}	DC Bias Voltage Output
12	AGND	Analog Ground
13	AV_{CC}	Analog Supply (+5.0V)
14	$\overline{OE}$	Digital Output Enable Control Input
15	DFS	Data Format Select Input
16	D9	Data Bit 9 Output (MSB)
17	D8	Data Bit 8 Output
18	D7	Data Bit 7 Output
19	D6	Data Bit 6 Output
20	D5	Data Bit 5 Output
21	DGND	Digital Ground
22	CLK	Sample Clock Input
23	DV_{CC2}	Digital Output Supply (+3.3V to +5V)
24	D4	Data Bit 4 Output
25	D3	Data Bit 3 Output
26	D2	Data Bit 2 Output
27	D1	Data Bit 1 Output
28	D0	Data Bit 0 Output (LSB)

Detailed Description

Theory of Operation

The HI5703 is a 10-bit fully differential sampling pipeline A/D converter with digital error correction. Figure 15 depicts the circuit for the front end differential-in-differential-out sample-and-hold (S/H). The switches are controlled by an internal clock which is a non-overlapping two phase signal, ϕ_1 and ϕ_2, derived from the master clock. During the sampling phase, ϕ_1, the input signal is applied to the sampling capacitors, C_S. At the same time the holding capacitors, C_H, are discharged to analog ground. At the falling edge of ϕ_1 the input signal is sampled on the bottom plates of the sampling capacitors. In the next clock phase, ϕ_2, the two bottom plates of the sampling capacitors are connected together and the holding capacitors are switched to the op-amp output nodes. The charge then redistributes between C_S and C_H completing one sample-and-hold cycle. The output is a fully-differential, sampled-data representation of the analog input. The circuit not only performs the sample-and-hold function but will also convert a single-ended input to a fully-differential output for the converter core. During the sampling phase, the V_{IN} pins see only the on-resistance of a switch and C_S. The relatively small values of these components result in a typical full power input bandwidth of 250MHz for the converter.

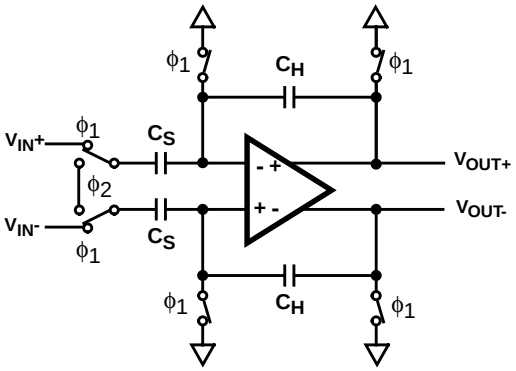


FIGURE 15. ANALOG INPUT SAMPLE-AND-HOLD

As illustrated in the functional block diagram and the timing diagram in Figure 1, nine identical pipeline subconverter stages, each containing a two-bit flash converter and a two-bit multiplying digital-to-analog converter, follow the S/H circuit with the tenth stage being a one bit flash converter. Each converter stage in the pipeline will be sampling in one phase and amplifying in the other clock phase. Each individual subconverter clock signal is offset by 180 degrees from the previous stage clock signal resulting in alternate stages in the pipeline performing the same operation.

The two-bit digital output of each stage is fed to a digital delay line controlled by the internal clock. The purpose of the delay line is to align the digital output data to the corresponding sampled analog input signal. This delayed data is fed to the digital error correction circuit which corrects the error in the output data with the information contained in the redundant bits to form the final ten bit output for the converter.

Because of the pipeline nature of this converter, the data on the bus is output at the 7th cycle of the clock after the analog sample is taken. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The output data is synchronized to the external clock by a double buffered latching technique.

The digital output bits are available in offset binary or two's complement format, the format being set by the Data Format Select (DFS) input.

Reference Voltage Inputs, V_{REF}- and V_{REF}+

The HI5703 requires two reference voltages connected to the V_{REF} pins. The HI5703 is tested with V_{REF}- equal to 2V and V_{REF}+ equal to 3.25V for a fully differential input voltage range of ±1.25V. V_{REF}+ and V_{REF}- can differ from the above voltages as long as the reference common mode voltage, ((V_{REF}+ + V_{REF}-)/2), does not exceed 2.625V ±50mV and the limits on V_{REF}+ and V_{REF}- are not exceeded.

In order to minimize overall converter noise it is recommended that adequate high frequency decoupling be provided at the reference voltage input pins, V_{REF}+ and V_{REF}-.

Analog Input, Differential Connection

The analog input to the HI5703 is a differential input that can be configured in various ways depending on the signal source and the required level of performance. A fully differential connection (Figure 16 and Figure 17) will give the best performance for the converter.

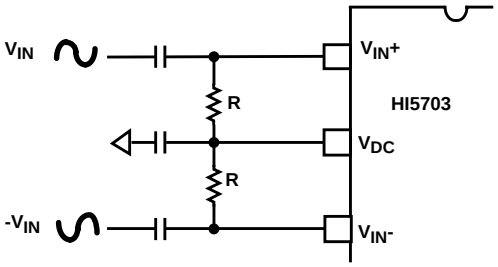


FIGURE 16. AC COUPLED DIFFERENTIAL INPUT

Since the HI5703 is powered by a single +5V analog supply, the analog input is limited to be between ground and +5V. For the differential input connection this implies the analog input common mode voltage can range from 0.625V to 4.375V. The performance of the ADC does not change significantly with the value of the analog input common mode voltage.

A DC voltage source, V_{DC}, equal to 2.8V (typical), is made available to the user to help simplify circuit design when using an AC coupled differential input. This low output impedance voltage source is not designed to be a reference but makes an excellent bias source and stays within the analog input common mode voltage range over temperature. It has a temperature coefficient of approximately +200ppm/^{O}C.

For the AC coupled differential input (Figure 16) assume the difference between V_{REF}+, typically 3.25V, and V_{REF}-, typically 2V, is 1.25V. Fullscale is achieved when the V_{IN}+ and V_{IN}- inputs are 1.25V_{P-P}, with V_{IN}- being 180 degrees out of phase with V_{IN}+. The converter will be at positive fullscale when the V_{IN}+ input is at V_{DC} + 0.625V and V_{IN}- is at V_{DC} - 0.625V (V_{IN}+ - V_{IN}- = 1.25V). Conversely, the converter will be at negative full scale when the V_{IN}+ input is equal to V_{DC} - 0.625V and V_{IN}- is at V_{DC} + 0.625V (V_{IN}+ - V_{IN}- = -1.25V).

The analog input can be DC coupled (Figure 17) as long as the inputs are within the analog input common mode voltage range (0.625V ≤ VDC ≤ 4.375V).

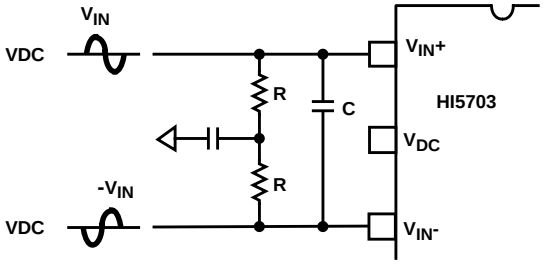


FIGURE 17. DC COUPLED DIFFERENTIAL INPUT

The resistors, R, in Figure 17 are not absolutely necessary but may be used as load setting resistors. A capacitor, C, connected from V_{IN}+ to V_{IN}- will help filter any high frequency noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well. Note, however, that the value of capacitor C chosen must take into account the highest frequency component of the analog input signal.

Analog Input, Single-Ended Connection

The configuration shown in Figure 18 may be used with a single ended AC coupled input.

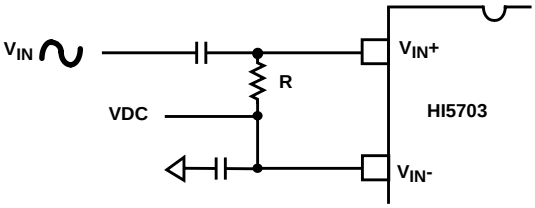


FIGURE 18. AC COUPLED SINGLE ENDED INPUT

Again, assume the difference between V_{REF}+, typically 3.25V, and V_{REF}-, typically 2V, is 1.25V. If V_{IN} is a 2.5V_{P-P} sinewave, then V_{IN}+ is a 2.5V_{P-P} sinewave riding on a positive voltage equal to VDC. The converter will be at positive fullscale when V_{IN}+ is at VDC + 1.25V and will be at negative fullscale when V_{IN}+ is equal to VDC - 1.25V. Sufficient headroom must be provided such that the input voltage never goes above +5V or below AGND. In this case, VDC could range between 1.25V and 3.75V without a significant change in ADC performance. The simplest way to produce VDC is to use the V_{DC} output of the HI5703.

The single ended analog input can be DC coupled (Figure 19) as long as the input is within the analog input common mode voltage range.

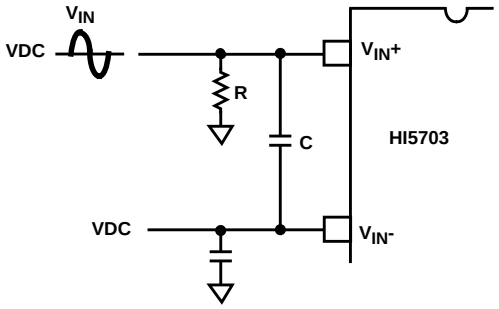


FIGURE 19. DC COUPLED SINGLE ENDED INPUT

The resistor, R, in Figure 19 is not absolutely necessary but may be used as a load setting resistor. A capacitor, C, connected from $V_{IN}+$ to $V_{IN}-$ will help filter any high frequency noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well. Note, however, that the value of capacitor C chosen must take into account the highest frequency component of the analog input signal.

A single ended source may give better overall system performance if it is first converted to differential before driving the HI5703. Refer to the application notes AN9534, “Using the HI5703 Evaluation Board”, and AN9413, “Driving the Analog Input of the HI5702”. Application note AN9413 applies to the HI5703 as well as the HI5702 and describes several different ways of driving the analog differential inputs.

Digital Output Control and Clock Requirements

The HI5703 provides a standard high-speed interface to external TTL logic families.

In order to ensure rated performance of the HI5703, the duty cycle of the clock should be held at 50% ±5%. It must also have low jitter and operate at standard TTL levels.

Performance of the HI5703 will only be guaranteed at conversion rates above 1 MSPS. This ensures proper performance of the internal dynamic circuits. Similarly, when power is first applied to the converter, a maximum of 20 cycles at a sample rate above 1 MSPS will have to be performed before valid data is available.

A Data Format Select (DFS) pin is provided which will determine the format of the digital data outputs. When at logic low, the data will be output in offset binary format. When at logic high, the data will be output in two’s complement format. Refer to Table 2 for further information.

The output enable pin, $\overline{OE}$, when pulled high will three-state the digital outputs to a high impedance state. Set the $\overline{OE}$ input to logic low for normal operation.

$\overline{OE}$ INPUT	DIGITAL DATA OUTPUTS
0	Active
1	High Impedance

Supply and Ground Considerations

The HI5703 has separate analog and digital supply and ground pins to keep digital noise out of the analog signal path. The digital data outputs also have a separate supply pin, DV_{CC2}, which can be powered from a 3.3V to 5.0V supply. This allows the outputs to interface with 3.3V logic if so desired.

The part should be mounted on a board that provides separate low impedance connections for the analog and digital supplies and grounds. For best performance, the supplies to the HI5703 should be driven by clean, linear regulated supplies. The board should also have good high frequency decoupling capacitors mounted as close as possible to the converter. If the part is powered off a single supply then the analog supply and ground pins should be isolated by ferrite beads from the digital supply and ground pins.

Refer to the application notes “Using Intersil High Speed A/D Converters” (AN9214) for additional considerations when using high speed converters.

Static Performance Definitions

Offset Error (V_{OS})

The midscale code transition should occur at a level $^1/_4$ LSB above half-scale. Offset is defined as the deviation of the actual code transition from this point.

Full-Scale Error (FSE)

The last code transition should occur for an analog input that is $^3/_4$ LSB below positive Fullscale (+FS) with the offset error removed. Full-scale error is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL)

DNL is the worst case deviation of a code width from the ideal value of 1 LSB.

Integral Linearity Error (INL)

INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Power Supply Sensitivity

Each of the power supplies are moved plus and minus 5% and the shift in the offset and full scale error (in LSBs) is noted.

TABLE 2. A/D CODE TABLE

CODE CENTER DESCRIPTION	DIFFERENTIAL INPUT VOLTAGE ($V_{IN}+ - V_{IN}-$)	OFFSET BINARY OUTPUT CODE (DFS LOW)										TWO'S COMPLEMENT OUTPUT CODE (DFS HIGH)									
		MSB									LSB	MSB									LSB
		D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
+Full Scale (+FS) - $^1/_4$ LSB	1.24939V	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
+FS - $1^1/_4$ LSB	1.24695V	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	0
+$^3/_4$ LSB	1.83mV	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-$^1/_4$ LSB	-0.610mV	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
-FS + $1^3/_4$ LSB	-1.24573V	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1
-Full Scale (-FS) + $^3/_4$ LSB	-1.24817V	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

NOTES:

8. The voltages listed above represent the ideal center of each output code shown as a function of the reference voltage.
9. $V_{REF}+ = 3.25V$ and $V_{REF}- = 2.0V$.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI5703. A low distortion sine wave is applied to the input, it is coherently sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with an FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from full scale for all these tests.

SNR and SINAD are quoted in dB. The distortion numbers are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

Effective Number Of Bits (ENOB)

The effective number of bits (ENOB) is calculated from the SINAD data by:

$$ENOB = (SINAD - 1.76 + V_{CORR}) / 6.02$$

where: $V_{CORR} = 0.5$ dB

V_{CORR} adjusts the ENOB for the amount the input is below fullscale.

Signal To Noise and Distortion Ratio (SINAD)

SINAD is the ratio of the measured RMS signal to RMS sum of all the other spectral components below the Nyquist frequency, $f_S/2$, excluding DC.

Signal To Noise Ratio (SNR)

SNR is the ratio of the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components below $f_S/2$ excluding the fundamental, the first five harmonics and DC.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the fundamental input signal.

2nd and 3rd Harmonic Distortion

This is the ratio of the RMS value of the applicable harmonic component to the RMS value of the fundamental input signal.

Spurious Free Dynamic Range (SFDR)

SFDR is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spectral component in the spectrum below $f_S/2$.

Intermodulation Distortion (IMD)

Nonlinearities in the signal path will tend to generate intermodulation products when two tones, f_1 and f_2, are present at the inputs. The ratio of the measured signal to the distortion terms is calculated. The terms included in the calculation are (f_1+f_2), (f_1-f_2), $(2f_1)$, $(2f_2)$, $(2f_1+f_2)$, $(2f_1-f_2)$, (f_1+2f_2), (f_1-2f_2). The ADC is tested with each tone 6dB below full scale.

Transient Response

Transient response is measured by providing a full scale transition to the analog input of the ADC and measuring the number of cycles it takes for the output code to settle within 10-bit accuracy.

Over-Voltage Recovery

Over-Voltage Recovery is measured by providing a full scale transition to the analog input of the ADC which overdrives the input by 200mV, and measuring the number of cycles it takes for the output code to settle within 10-bit accuracy.

Full Power Input Bandwidth (FPBW)

Full power input bandwidth is the analog input frequency at which the amplitude of the digitally reconstructed output has decreased 3dB below the amplitude of the input sine wave. The input sine wave has an amplitude which swings from -FS to +FS. The bandwidth given is measured at the specified sampling frequency.

Video Definitions

Differential Gain and Differential Phase are two commonly found video specifications for characterizing the distortion of a chrominance signal as it is offset through the input voltage range of an ADC.

Differential Gain (DG)

Differential Gain is the peak difference in chrominance amplitude (in percent) relative to the reference burst.

Differential Phase (DP)

Differential Phase is the peak difference in chrominance phase (in degrees) relative to the reference burst.

Timing Definitions

Refer to Figure 1 and Figure 2 for these definitions.

Aperture Delay (t_{AP})

Aperture delay is the time delay between the external sample command (the falling edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter (t_{AJ})

Aperture jitter is the RMS variation in the aperture delay due to variation of internal clock path delays.

Data Hold Time (t_H)

Data hold time is the time to where the previous data (N - 1) is no longer valid.

Data Output Delay Time (t_{OD})

Data output delay time is the time to where the new data (N) is valid.

Data Latency (t_{LAT})

After the analog sample is taken, the digital data is output on the bus at the 7th cycle of the clock. This is due to the pipeline nature of the converter where the data has to ripple through the stages. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The digital data lags the analog input sample by 7 cycles.

Power-Up initialization

This time is defined as the maximum number of clock cycles that are required to initialize the converter at power-up. The requirement arises from the need to initialize the dynamic circuits within the converter.

AMP	A/D	DSP/µP	D/A	AMP
HFA1100	HI5702	HSP9501	HI5780	HA5020
HFA1105	HI5703	HSP48410	HI1171	HA2842
HFA1106		HSP48908	CA3338	HFA1115
HFA1135		HSP48212		HFA1212
HFA1145		HSP43891		HFA1412
HFA1245		HSP43168		
		HSP43216		

HFA1100: 850MHz Video Op Amp
HFA1105: 300MHz Video Op Amp
HFA1106: 250MHz Video Op Amp with Bandwidth Limit Control
HFA1135: 350MHz Video Op Amp with Output Limiting
HFA1145: 300MHz Video Op Amp with Output Disable
HFA1245: Dual 350MHz Video Op Amp with Output Disable
HI5702: 10-Bit, 40 MSPS, A/D Converter
HI5703: 10-Bit, 40 MSPS, Low Power A/D Converter
HSP9501: Programmable Data Buffer
HSP48410: Histogrammer/Accumulating Buffer, 10-Bit Pixel Resolution
HSP48908: 2-D Convolver, 3 x 3 Kernal Convolution, 8-Bit
HSP48212: Digital Video Mixer
HSP43891: Digital Filter, 30MHz, 9-Bit
HSP43168: Dual FIR Filter, 10-Bit, 33MHz/45MHz
HSP43216: Digital Half Band Filter
HI5780: 10-Bit, 80 MSPS, Video D/A Converter
HI1171: 8-Bit, 40 MSPS, Video D/A Converter
CA3338: 8-Bit, 50 MSPS, Video D/A Converter
HA5020: 100MHz Video Op Amp
HA2842: High Output Current, Video Op Amp
HFA1115: 225MHz Programmable Gain Video Buffer with Output Limiting
HFA1212: 350MHz, Dual Programmable Gain Video Buffer
HFA1412: 350MHz, Quad Programmable Gain Video Buffer

In addition, CMOS Logic Families in HC/HCT, AC/ACT, FCT and CD4000 are available.

FIGURE 20. 10-BIT VIDEO IMAGING COMPONENTS

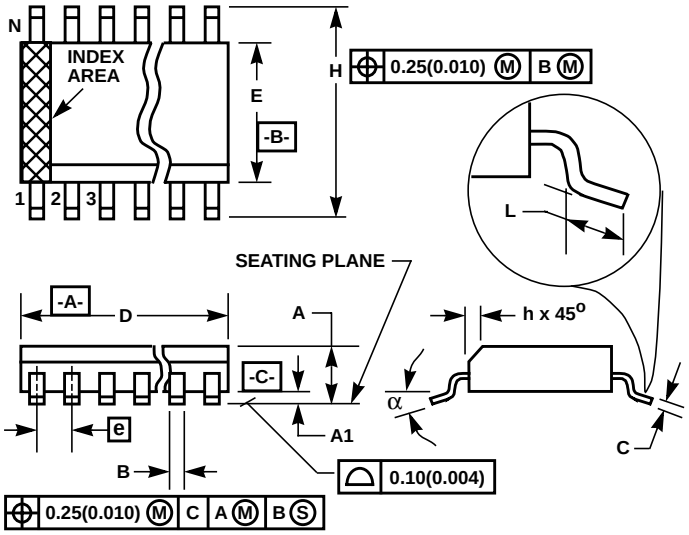
AMP	A/D	DSP/µP	D/A	AMP
HFA1100	HI5702	HSP43168	HI5721	HFA1112
HFA1110	HI5703	HSP43216	HI5780	HFA1113
HFA3101		HSP43220	HI20201	
HFA3102		HSP43891	HI20203	
HFA3600		HSP50016		
		HSP50110		
		HSP50210		

HFA1100: 850MHz Op Amp
HFA1110: 750MHz Unity Gain Video Buffer
HFA3101: Gilbert Cell Transistor Array
HFA3102: Dual Long-Tailed Pair Transistor Array
HFA3600: Low Noise Amplifier/Mixer
HI5702: 10-Bit, 40 MSPS, A/D Converter
HI5703: 10-Bit, 40 MSPS, Low Power A/D Converter
HSP43168: Dual FIR Filter, 10-Bit, 33MHz/45MHz
HSP43216: Digital Half Band Filter
HSP43220: Decimating Digital Filter
HSP43891: Digital Filter, 30MHz, 9-Bit
HSP50016: Digital Down Converter
HSP50110: Digital Quadrature Tuner
HSP50210: Digital Costas Loop
HI5721: 10-Bit, 100 MSPS, Communications D/A Converter
HI5780: 10-Bit, 80 MSPS, D/A Converter
HI20201: 10-Bit, 160 MSPS, High Speed D/A Converter
HI20203: 8-Bit, 160 MSPS, High Speed D/A Converter
HFA1112: 850MHz Programmable Gain Video Buffer
HFA1113: 850MHz Programmable Gain Video Buffer with Output Limiting

In addition, CMOS Logic Families in HC/HCT, AC/ACT, FCT and CD4000 are available.

FIGURE 21. 10-BIT COMMUNICATIONS COMPONENTS

Small Outline Plastic Packages (SOIC)



M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0^o	8^o	0^o	8^o	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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