EN29F040
4 Megabit (512K x 8-bit) Flash Memory

FEATURES

- 5.0V operation for read/write/erase operations
- Fast Read Access Time
  - 45ns, 55ns, 70ns, and 90ns
- Sector Architecture:
  - 8 uniform sectors of 64Kbytes each
  - Supports full chip erase
  - Individual sector erase supported
  - Sector protection: Hardware locking of sectors to prevent program or erase operations within individual sectors
- High performance program/erase speed
  - Byte program time: 10µs typical
  - Sector erase time: 500ms typical
  - Chip erase time: 3.5s typical
- Low Standby Current
  - 1µA CMOS standby current-typical
  - 1mA TTL standby current
- Low Power Active Current
  - 30mA active read current
  - 30mA program/erase current
- JEDEC Standard program and erase commands
- JEDEC standard $\overline{\text{DATA}}$ polling and toggle bits feature
- Single Sector and Chip Erase
- Sector Unprotect Mode
- Embedded Erase and Program Algorithms
- Erase Suspend / Resume modes: Read and program another Sector during Erase Suspend Mode
- 0.35 µm double-metal double-poly triple-well CMOS Flash Technology
- Low Vcc write inhibit ≤ 3.2V
- 100K endurance cycle
- Package Options
  - 32-pin PDIP
  - 32-pin PLCC
  - 32-pin TSOP (Type 1)
- Commercial and Industrial Temperature Ranges

GENERAL DESCRIPTION

The EN29F040 is a 4-Megabit, electrically erasable, read/write non-volatile flash memory. Organized into 512K words with 8 bits per word, the 4M of memory is arranged in eight uniform sectors of 64Kbytes each. Any byte can be programmed typically in 10µs. The EN29F040 features 5.0V voltage read and write operation, with access times as fast as 45ns to eliminate the need for WAIT states in high-performance microprocessor systems.

The EN29F040 has separate Output Enable ($\overline{\text{OE}}$), Chip Enable ($\overline{\text{CE}}$), and Write Enable ($\overline{\text{WE}}$) controls, which eliminate bus contention issues. This device is designed to allow either single (or multiple) Sector or full chip erase operation, where each Sector can be individually protected against program/erase operations or temporarily unprotected to erase or program. The device can sustain a minimum of 100K program/erase cycles on each Sector.

TABLE 1. PIN DESCRIPTION

Pin Name	Function
A0-A18	Addresses
DQ0-DQ7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
Vcc	Supply Voltage (5V ± 10%)
Vss	Ground

FIGURE 1. LOGIC DIAGRAM

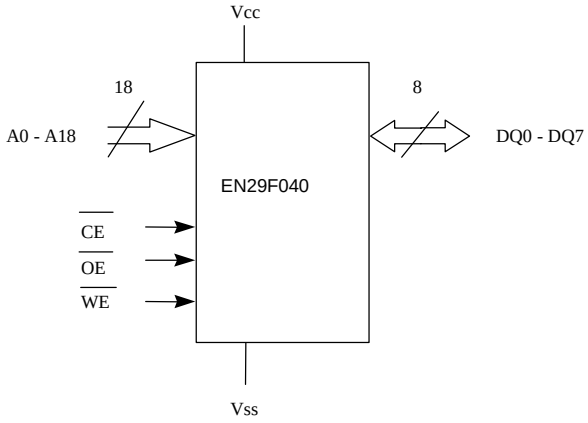


TABLE 2. SECTOR ARCHITECTURE

Sector	ADDRESSES	SIZE (Kbytes)	A18	A17	A16
7	70000h - 7FFFFh	64	1	1	1
6	60000h - 6FFFFh	64	1	1	0
5	50000h – 5FFFFh	64	1	0	1
4	40000h – 4FFFFh	64	1	0	0
3	30000h – 3FFFFh	64	0	1	1
2	20000h - 2FFFFh	64	0	1	0
1	10000h - 1FFFFh	64	0	0	1
0	00000h - 0FFFFh	64	0	0	0

BLOCK DIAGRAM

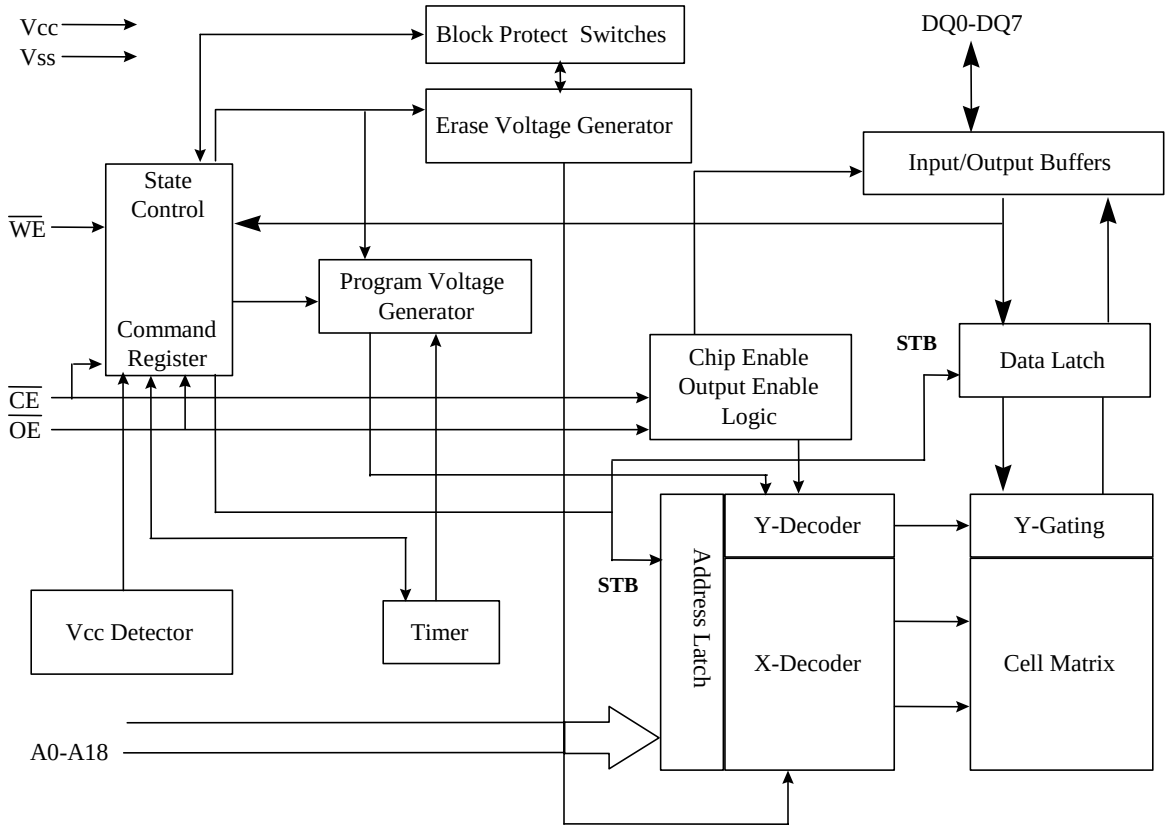


FIGURE 2. PDIP

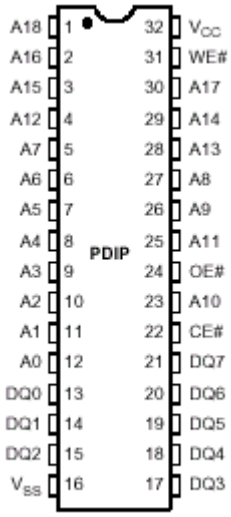


FIGURE 3. PLCC

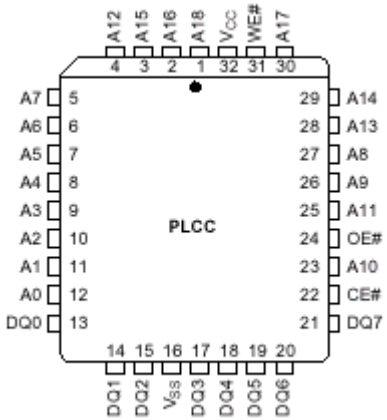


FIGURE 4. TSOP

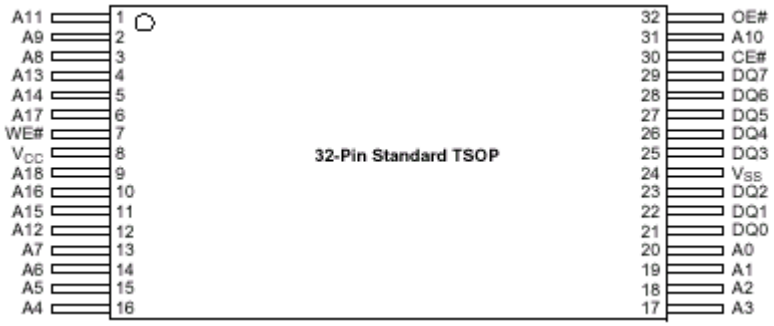


TABLE 3. OPERATING MODES

4M FLASH USER MODE TABLE

	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	A9	A8	A6	A5	A1	A0	Ax/y	DQ(0-7)
USER MODE											
STANDBY	H	X	X	X	X	X	X	X	X	X	HI-Z
READ	L	H	L	A9	A8	A6	A5	A1	A0	Ax/y	DQ (0-7)
OUTPUT DISABLE	L	H	H	X	X	X	X	X	X	X	HI-Z
READ MANUFACTURE ID	L	H	L	VID	L/H	L	X	L	L	X	MANUFACTURE ID
READ DEVICE ID	L	H	L	VID	L/H	L	X	L	H	X	DEVICE ID (T/B)
VERIFY SECTOR PROTECTION	L	H	L	VID	X	L	X	H	L	X	CODE
SECTOR PROTECTION	L	Pulse L	VID	VID	X	L	X	X	X	X	X
VERIFY SECTOR UNPROTECTION	L	H	L	VID	X	H	X	H	L	X	CODE
SECTOR UNPROTECTION	Pulse L	VID	VID	L	X	X	H	X	X	X	X
WRITE	L	L	H	A9	A8	A6	A5	A1	A0	Ax/y	DIN (0-7)

NOTES:

1) L = V_{IL}, H = V_{IH}, V_{ID} = 11.0V ± 0.5V
2) X = Don't care, either V_{IH} or V_{IL}
3) Ax/y: Ax = Addr(x), Ay = Addr(y)

TABLE 4. DEVICE IDENTIFICTION

4M FLASH MANUFACTURER/DEVICE ID TABLE

	A8	A6	A1	A0	DQ(7-0) HEX
READ MANUFACTURER ID	H(1)	L	L	L	MANUFACTURER ID 1C
READ DEVICE ID	H(2)	L	L	H	DEVICE ID 04

NOTES:

1) If a Manufacturing ID is read with A8 = L, the chip will output a configuration code 7Fh. A further Manufacturing ID must be read with A8 = H.
2) If a Device ID is read with A8 = L, the chip will output a configuration code 7Fh. A further Device ID must be read with A8 = H.

USER MODE DEFINITIONS

Standby Mode

The EN29F040 has a CMOS-compatible standby mode, which reduces the current to < 1µA (typical). It is placed in CMOS-compatible standby when the $\overline{CE}$ pin is at $V_{CC} \pm 0.5$. The device also has a TTL-compatible standby mode, which reduces the maximum V_{CC} current to < 1mA. It is placed in TTL-compatible standby when the $\overline{CE}$ pin is at V_{IH}. When in standby modes, the outputs are in a high-impedance state independent of the $\overline{OE}$ input.

Read Mode

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See “Erase Suspend/Erase Resume Commands” for more information on this mode.

The system must issue the reset command to re-enable the device for reading array data if DQ5 goes high, or while in the autoselect mode. See “Reset Command” section.

See also “Requirements for Reading Array Data” in the “Device Bus Operations” section for more information. The Read Operations table provides the read parameters, and Read Operation Timings diagram shows the timing diagram.

Output Disable Mode

When the $\overline{OE}$ pin is at a logic high level (V_{IH}), the output from the EN29F040 is disabled. The output pins are placed in a high impedance state.

Auto Select Identification Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (10.5 V to 11.5 V) on address pin A9. Address pins A6, A1, and A0 must be as shown in Autoselect Codes (High Voltage Method) table. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits. Refer to the corresponding Sector Address Tables. The Command Definitions table shows the remaining address bits that are don’t care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0.

To access the autoselect codes in-system; the host system can issue the autoselect command via the command register, as shown in the Command Definitions table. This method does not require V_{ID}. See “Command Definitions” for details on using the autoselect mode.

Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are don't care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete. The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to reading array data (also applies to autoselect during Erase Suspend).

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

Write Mode

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 5 (Command Definitions) shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using DQ7 or DQ6. See "Write Operation Status" for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from a "0" back to a "1".** Attempting to do so may halt the operation and set DQ5 to "1", or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still "0". Only erase operations can convert a "0" to a "1".

COMMAND DEFINITIONS

The operations of the EN29F040 are selected by one or more commands written into the command register to perform Read/Reset Memory, Read ID, Read Sector Protection, Program, Sector Erase, Chip Erase, Erase Suspend and Erase Resume. Commands are made up of data sequences written at specific addresses via the command register. The sequences for the specified operation are defined in the Command Table (Table 5). Incorrect addresses, incorrect data values or improper sequences will reset the device to the read mode.

Table 5. EN29F040 Command Definitions

Command Sequence Read/Reset	Write Cycles Req'd	1st Write Cycle		2nd Write Cycle		3rd Write Cycle		4th Write Cycle		5th Write Cycle		6th Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	RA	RD										
Reset	1	XXXh	F0h										
Read/Reset	4	555h	AAh	2AAh	55h	555h	F0h	RA	RD				
AutoSelect Manufacturer ID	4	555h	AAh	2AAh	55h	555h	90h	000h/ 100h	7Fh/ 1Ch				
AutoSelect Device ID	4	555h	AAh	2AAh	55h	555h	90h	001h/ 101h	7Fh/ 04h				
AutoSelect Sector Protect Verify	4	555h	AAh	2AAh	55h	555h	90h	BA & 02h	00h/ 01h				
Byte Program	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD				
Chip Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h
Sector Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	BA	30h
Sector Erase Suspend	1	xxxh	B0h										
Sector Erase Resume	1	xxxh	30h										

Notes:

RA = Read Address: address of the memory location to be read. This one is a read cycle.
RD = Read Data: data read from location RA during Read operation. This one is a read cycle.
PA = Program Address: address of the memory location to be programmed
PD = Program Data: data to be programmed at location PA
BA = Sector Address: address of the Sector to be erased. Address bits A17-A13 uniquely select any Sector.

Byte Programming Command

Programming the EN29F040 is performed on a byte-by-byte basis using a four bus-cycle operation (two unlock write cycles followed by the Program Setup command and Program Data Write cycle). When the program command is executed, no additional CPU controls or timings are necessary. An internal timer terminates the program operation automatically. Address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever is last; data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever is first. The program operation is completed when EN29F040 returns the equivalent data to the programmed location.

Programming status may be checked by sampling data on DQ7 ($\overline{DATA}$ polling) or on DQ6 (toggle bit). Changing data from 0 to 1 requires an erase operation. When programming time limit is exceeded, DQ5 will produce a logical "1" and a Reset command can return the device to Read mode.

Chip Erase Command

Chip erase is a six-bus-cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. The Command Definitions table shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Erase algorithm are ignored.

The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. See “Write Operation Status” for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Flowchart 4 illustrates the algorithm for the erase operation. See the Erase/Program Operations tables in “AC Characteristics” for parameters, and Chip/Sector Erase Operation Timings for timing waveforms.

Sector Erase Command

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two un-lock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. The Command Definitions table shows the address and data requirements for the sector erase command sequence.

The device does not require the system to preprogram the memory prior to erase. The Embedded Erase algorithm automatically programs and verifies the sector for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

This device does not support multiple sector erase commands. Sector Erase operation will commence immediately after the first 30h command is written. The first sector erase operation must finish before another sector erase command can be given.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. Refer to “Write Operation Status” for information on these status bits. Flowchart 4 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations tables in the “AC Characteristics” section for parameters, and to the Sector Erase Operations Timing diagram for timing waveforms.

Erase Suspend / Resume Command

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Addresses are “don’t-cares” when writing the Erase Suspend command.

When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation.

After the erase operation has been suspended, the system can read array data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See “Write Operation Status” for information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See “Write Operation Status” for more information.

The system must write the Erase Resume command (address bits are “don’t care”) to exit the erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.

Sector Protection/Unprotection

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors.

Sector protection/unprotection must be implemented using programming equipment. The procedure requires a high voltage (V_{ID}) on address pin A9 and the control pins. Contact Eon Silicon Devices, Inc. for an additional supplement on this feature.

WRITE OPERATION STATUS

DQ7
$\overline{\text{DATA}}$ Polling

The EN29F040 provides $\overline{\text{DATA}}$ Polling on DQ7 to indicate to the host system the status of the embedded operations. The $\overline{\text{DATA}}$ Polling feature is active during the Byte Programming, Sector Erase, Chip Erase, and Erase Suspend. (See Table 6)

When the Byte Programming is in progress, an attempt to read the device will produce the complement of the data last written to DQ7. Upon the completion of the Byte Programming, an attempt to read the device will produce the true data last written to DQ7. For the Byte Programming, $\overline{\text{DATA}}$ polling is valid after the rising edge of the fourth $\overline{\text{WE}}$ or $\overline{\text{CE}}$ pulse in the four-cycle sequence.

When the embedded Erase is in progress, an attempt to read the device will produce a "0" at the DQ7 output. Upon the completion of the embedded Erase, the device will produce the "1" at the DQ7 output during the read. For Chip Erase, the $\overline{\text{DATA}}$ polling is valid after the rising edge of the sixth $\overline{\text{WE}}$ or $\overline{\text{CE}}$ pulse in the six-cycle sequence. For Sector Erase, $\overline{\text{DATA}}$ polling is valid after the last rising edge of the sector erase $\overline{\text{WE}}$ or $\overline{\text{CE}}$ pulse.

$\overline{\text{DATA}}$ Polling must be performed at any address within a sector that is being programmed or erased and not a protected sector. Otherwise, $\overline{\text{DATA}}$ polling may give an inaccurate result if the address used is in a protected sector.

Just prior to the completion of the embedded operations, DQ7 may change asynchronously when the output enable ($\overline{\text{OE}}$) is low. This means that the device is driving status information on DQ7 at one instant of time and valid data at the next instant of time. Depending on when the system samples the DQ7 output, it may read the status of valid data. Even if the device has completed the embedded operations and DQ7 has a valid data, the data output on DQ0-DQ6 may be still invalid. The valid data on DQ0-DQ7 will be read on the subsequent read attempts.

The flowchart for $\overline{\text{DATA}}$ Polling (DQ7) is shown on Flowchart 5. The $\overline{\text{DATA}}$ Polling (DQ7) timing diagram is shown in Figure 8.

DQ6
Toggle Bit I

The EN29F040 provides a "Toggle Bit" on DQ6 to indicate to the host system the status of the embedded programming and erase operations. (See Table 6)

During an embedded Program or Erase operation, successive attempts to read data from the device at any address (by toggling $\overline{\text{OE}}$ or $\overline{\text{CE}}$) will result in DQ6 toggling between "zero" and "one". Once the embedded Program or Erase operation is complete, DQ6 will stop toggling and valid data will be read on the next successive attempts. During Byte Programming, the Toggle Bit is valid after the rising edge of the fourth $\overline{\text{WE}}$ pulse in the four-cycle sequence. For Chip Erase, the Toggle Bit is valid after the rising edge of the sixth-cycle sequence. For Sector Erase, the Toggle Bit is valid after the last rising edge of the Sector Erase $\overline{\text{WE}}$ pulse. The Toggle Bit is also active during the sector erase time-out window.

In Byte Programming, if the sector being written to is protected, DQ6 will toggles for about 2 µs, then stop toggling without the data in the sector having changed. In Sector Erase or Chip Erase, if all selected sectors are protected, DQ6 will toggle for about 100 µs. The chip will then return to the read mode without changing data in all protected sectors.

Toggling either $\overline{CE}$ or $\overline{OE}$ will cause DQ6 to toggle.

The flowchart for the Toggle Bit (DQ6) is shown in Flowchart 6. The Toggle Bit timing diagram is shown in Figure 9.

DQ5 Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1." (The Toggle Bit (DQ6) should also be checked at this time to make sure that the DQ5 is not a "1" due to the device having returned to read mode.) This is a failure condition that indicates the program or erase cycle was not successfully completed. . $\overline{DATA}$ Polling (DQ7), Toggle Bit (DQ6) and Erase Toggle Bit (DQ2) still function under this condition. Setting the $\overline{CE}$ to V_{IH} will partially power down the device under those conditions.

The DQ5 failure condition may appear if the system tries to program a "1" to a location that is previously programmed to "0." **Only an erase operation can change a "0" back to a "1."** Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, DQ5 produces a "1." Under both these conditions, the system must issue the reset command to return the device to reading array data.

DQ2 Erase Toggle Bit II

The "Toggle Bit" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence. DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 6 to compare outputs for DQ2 and DQ6.

Flowchart 6 shows the toggle bit algorithm, and the section "DQ2: Toggle Bit" explains the algorithm. See also the "DQ6: Toggle Bit I" subsection. Refer to the Toggle Bit Timings figure for the toggle bit timing diagram. The DQ2 vs. DQ6 figure shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Flowchart 6 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, a system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped

toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Flowchart 6).

Table 6. Status Register Bits

DQ	Name	Logic Level	Definition
7	$\overline{\text{DATA}}$ POLLING	'1'	Erase Complete or erase Sector in Erase suspend
		'0'	Erase On-Going
		DQ7	Program Complete or data of non-erase Sector during Erase Suspend
		DQ7	Program On-Going
6	TOGGLE BIT	'-1-0-1-0-1-0-1-'	Erase or Program On-going
		DQ6	Read during Erase Suspend
		'-1-1-1-1-1-1-1-'	Erase Complete
5	ERROR BIT	'1'	Program or Erase Error
		'0'	Program or Erase On-going
2	TOGGLE BIT	'-1-0-1-0-1-0-1-'	Chip Erase, Erase or Erase suspend on currently addressed Sector. (When DQ5=1, Erase Error due to currently addressed Sector. Program during Erase Suspend on-going at current address
		DQ2	Erase Suspend read on non Erase Suspend Sector

Notes:

DQ7 $\overline{\text{DATA}}$ Polling: indicates the P/E C status check during Program or Erase, and on completion before checking bits DQ5 for Program or Erase Success.

DQ6 Toggle Bit: remains at constant level when P/E operations are complete or erase suspend is acknowledged. Successive reads output complementary data on DQ6 while programming or Erase operation are on-going.

DQ5 Error Bit: set to "1" if failure in programming or erase

DQ2 Toggle Bit: indicates the Erase status and allows identification of the erased Sector.

DATA PROTECTION

Power-up Write Inhibit

During power-up, the device automatically resets to READ mode and locks out write cycles. Even with $\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IL} and $\overline{OE}$ = V_{IH}, the device will not accept commands on the rising edge of $\overline{WE}$.

Low V_{CC} Write Inhibit

During V_{CC} power-up or power-down, the EN20F040 locks out write cycles to protect against any unintentional writes. If V_{CC} < V_{LOK}, the command register is disabled and all internal program or erase circuits are disabled. Under this condition, the device will reset to the READ mode. Subsequent writes will be ignored until V_{CC} > $V_{LKO.}$

Write “Noise” Pulse Protection

Noise pulses less than 5ns on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ will neither initiate a write cycle nor change the command register.

Logical Inhibit

If $\overline{CE}$=V_{IH} or $\overline{WE}$=V_{IH}, writing is inhibited. To initiate a write cycle, $\overline{CE}$ and $\overline{WE}$ must be a logical “zero”. If $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$ are all logical zero (not recommended usage), it will be considered a write.

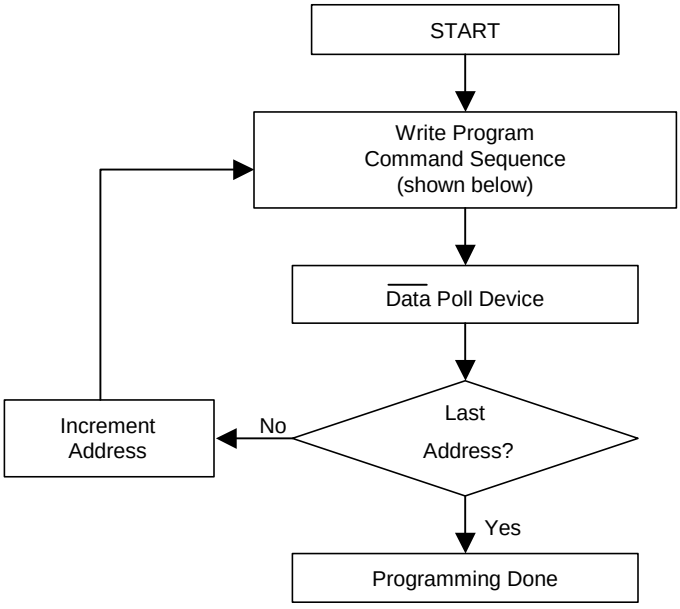
Sector Protect and Unprotect

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operation in previously protected sectors.

Sector protection/unprotection must be implemented using programming equipment. The procedure requires a high voltage (V_{ID}) on address pin A9 and the control pins. Contact Eon Silicon Devices, Inc. for an additional supplement on this feature.

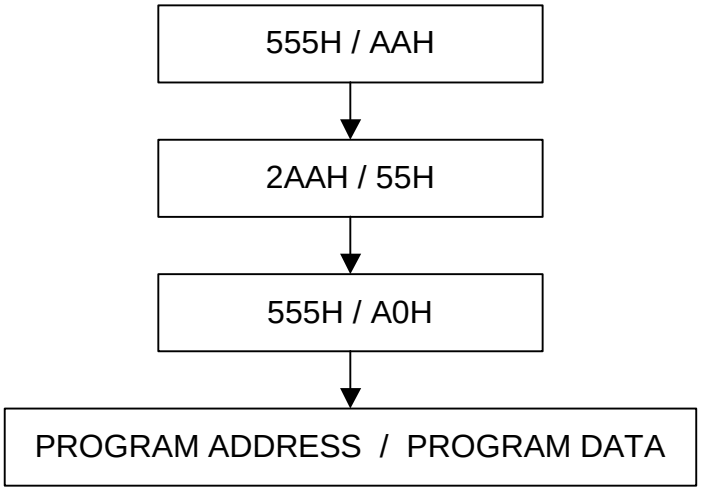
EMBEDDED ALGORITHMS

Flowchart 1. Embedded Program

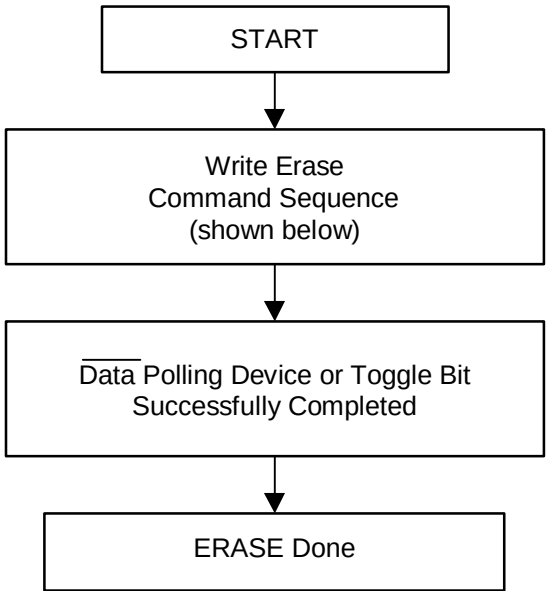


Flowchart 2. Embedded Program Command Sequence

See the Command Definitions section for more information.

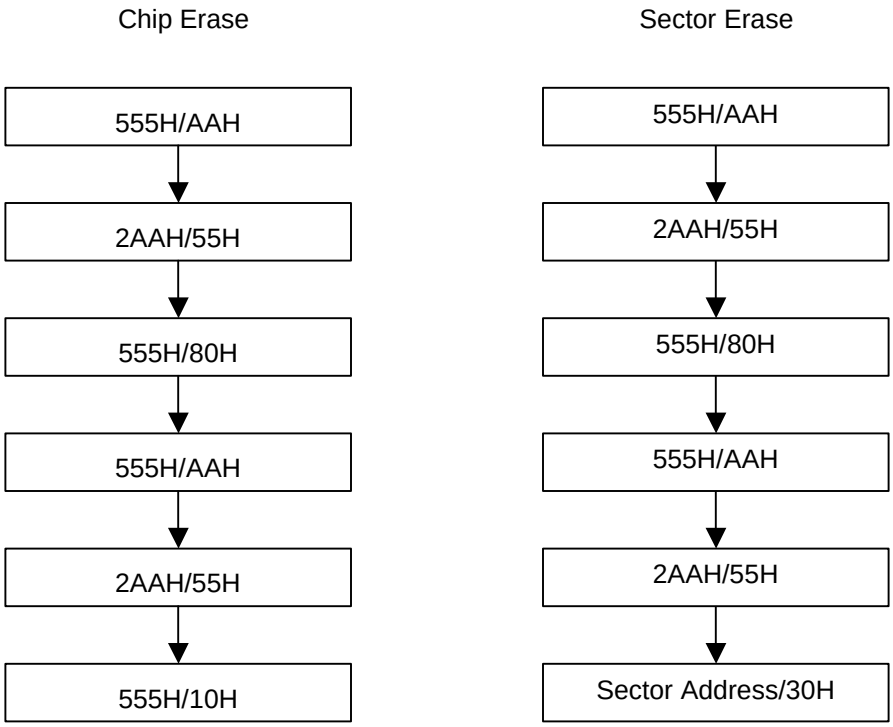


Flowchart 3. Embedded Erase

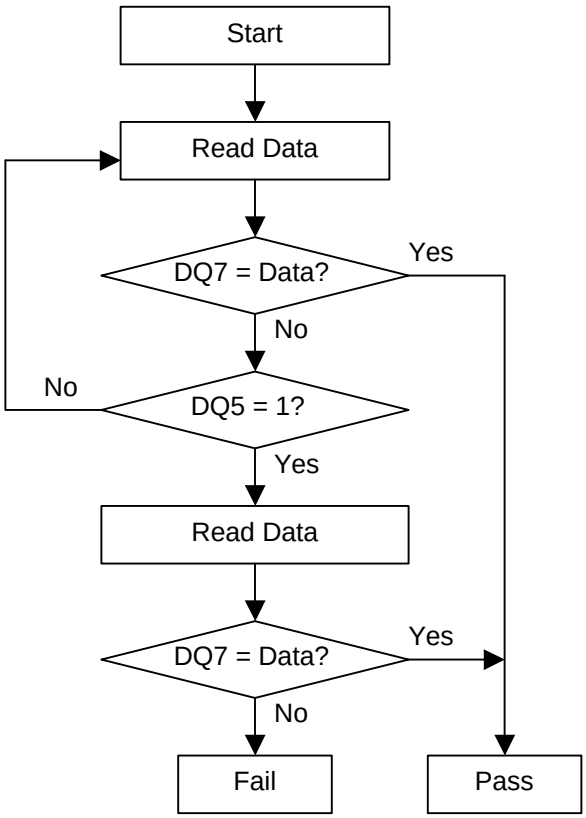


Flowchart 4. Embedded Erase Command Sequence

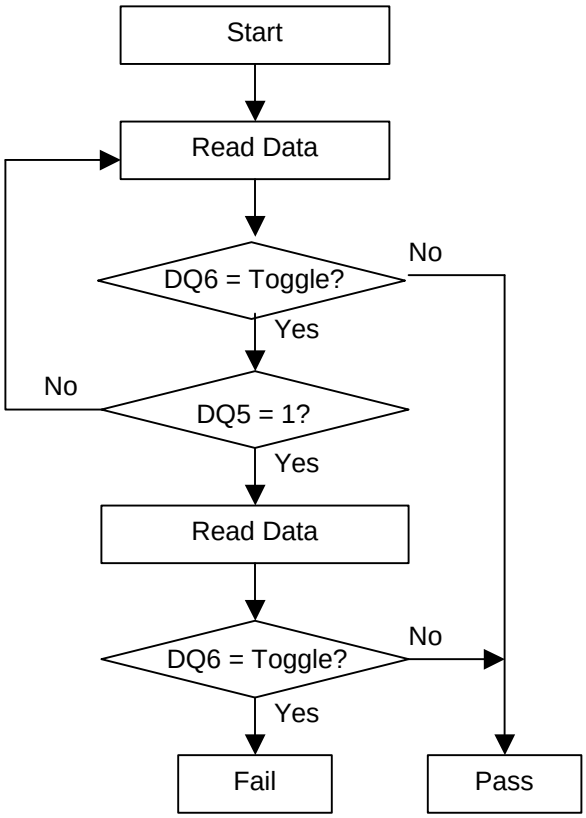
See the Command Definitions section for more information.



Flowchart 5. $\overline{\text{DATA}}$ Polling Algorithm



Flowchart 6. Toggle Bit Algorithm



ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . . –65°C to +125°C
Ambient Temperature
with Power Applied. . . . . –55°C to +125°C
Voltage with Respect to Ground
V_{CC} (Note 1) . . . . . –0.5 V to 7.0 V
A9, OE# (Note 2) . . . . . –0.5 V to 11.5 V
All other pins (Note 1) . . . . . –0.5 V to Vcc+0.5V
Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

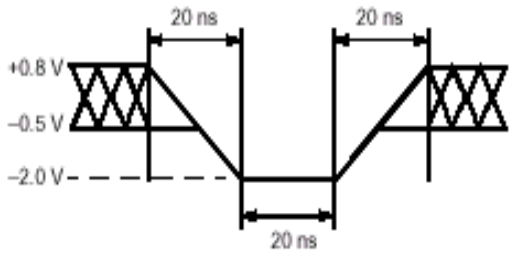
1. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may undershoot V_{SS} to –1.0V for periods of up to 50 ns and to –2.0 V for periods of up to 20 ns. See Left Figure below. Maximum DC voltage on input and I/O pins is V_{CC} + 0.5 V. During voltage transitions, input and I/O pins may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See Right Figure below.
2. Minimum DC input voltage on A9 pin is –0.5 V. During voltage transitions, A9 and OE# may undershoot V_{SS} to –1.0V for periods of up to 50 ns and to –2.0 V for periods of up to 20 ns. See Left Figure. Maximum DC input voltage on A9 and OE# is 11.5 V which may overshoot to 12.5 V for periods up to 20 ns.
3. No more than one output shorted to ground at a time. Duration of the short circuit should not be greater than one second. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

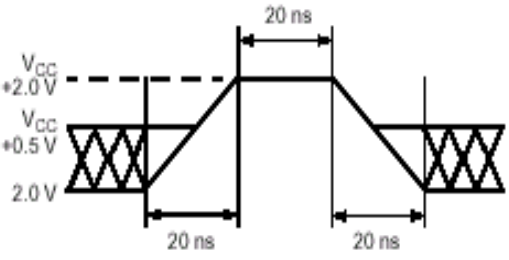
Commercial (C) Devices
Ambient Temperature (T A) . . . . . 0°C to +70°C

Industrial (I) Devices
Ambient Temperature (T A). . . . . -40°C to +85°C

V_{CC} Supply Voltages
V_{CC} for ± 5% devices . . . . . +4.75 V to +5.25 V
V_{CC} for ± 10% devices . . . . . +4.50 V to +5.50 V
Operating ranges define those limits between which the functionality of the device is guaranteed.



Maximum Negative Overshoot Waveform



Maximum Positive Overshoot Waveform

Table 7. DC Characteristics

(T_a = 0°C to 70°C or - 40°C to 85°C; V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Min	Max	Unit
I_{LI}	Input Leakage Current	0V≤ V_{IN} ≤ Vcc		±5	µA
I_{LO}	Output Leakage Current	0V≤ V_{OUT} ≤ Vcc		±5	µA
I_{CC1}	Supply Current (read) TTL Byte	$\overline{CE}$ = V_{IL}; $\overline{OE}$ = V_{IH}; f = 6MHz		30	mA
I_{CC2}	Supply Current (Standby) TTL	$\overline{CE}$ = V_{IH}		1.0	MA
I_{CC3}	Supply Current (Standby) CMOS	$\overline{CE}$ = Vcc ± 0.3V		5.0	µA
I_{CC4}	Supply Current (Program or Erase)	Byte program, Sector or Chip Erase in progress		30	mA
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High Voltage		2	Vcc + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA		0.45	V
V_{OH}	Output High Voltage TTL	I_{OH} = -2.5 mA	2.4		V
	Output High Voltage CMOS	I_{OH} = -100 µA	Vcc - 0.4V		V
V_{ID}	A9 Voltage (Electronic Signature)		10.5	11.5	V
I_{LIT}	A9 Current (Electronic Signature)	A9 = V_{ID}		100	µA
V_{LKO}	Supply voltage (Erase and Program lock-out)		3.2	4.2	V

Table 8. AC CHARACTERISTICS
Read-only Operations Characteristics

Parameter Symbols			Test Setup		Speed Options				
JEDEC	Standard	Description			-45	-55	-70	-90	Unit
t_{AVAV}	t_{RC}	Read Cycle Time		Min	45	55	70	90	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	Max	45	55	70	90	ns
t_{ELQV}	t_{CE}	Chip Enable To Output Delay	$\overline{OE} = V_{IL}$	Max	45	55	70	90	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay		Max	25	30	30	35	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z		Max	10	15	20	20	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z		Max	10	15	20	20	ns
t_{AXQX}	t_{OH}	Output Hold Time from Addresses, $\overline{CE}$ or $\overline{OE}$, whichever occurs first		Min	0	0	0	0	ns

Notes:

For -45, -55
Vcc = 5.0V ± 5%
Output Load : 1 TTL gate and 30pF
Input Rise and Fall Times: 5ns
Input Rise Levels: 0.0 V to 3.0 V
Timing Measurement Reference Level, Input and Output: 1.5 V

For all others:
Vcc = 5.0V ± 10%
Output Load: 1 TTL gate and 100 pF
Input Rise and Fall Times: 20 ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level, Input and Output: 0.8 V and 2.0 V

Table 9. AC CHARACTERISTICS
Write (Erase/Program) Operations

Parameter Symbols		Description			Speed Options				
JEDEC	Standard				-45	-55	-70	-90	Unit
t_{AVAV}	t_{WC}	Write Cycle Time		Min	45	55	70	90	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	35	45	45	45	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	20	25	30	45	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0	0	0	0	ns
	t_{OES}	Output Enable Setup Time		Min	0	0	0	0	ns
	t_{OEH}	Output Enable Hold Time	Read	MIn	0	0	0	0	ns
			Toggle and $\overline{DATA}$ Polling	Min	10	10	10	10	ns
t_{GHWL}	t_{GHWL}	Read Recovery Time before Write ($\overline{OE}$ High to $\overline{WE}$ Low)		Min	0	0	0	0	ns
t_{ELWL}	t_{CS}	$\overline{CE}$ SetupTime		Min	0	0	0	0	ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold Time		Min	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	25	30	35	45	ns
t_{WHDL}	t_{WPH}	Write Pulse Width High		Min	20	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation		Typ	7	7	7	7	µs
				Max	200	200	200	200	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation		Typ	0.3	0.3	0.3	0.3	s
				Max	5	5	5	5	s
t_{WHWH3}	t_{WHWH3}	Chip Erase Operation		Typ	3	3	3	3	s
				Max	35	35	35	35	s
	t_{VCS}	Vcc Setup Time		Min	50	50	50	50	µs
	t_{VIDR}	Rise Time to V_{ID}		Min	500	500	500	500	ns

Table 10. AC CHARACTERISTICS
Write (Erase/Program) Operations

Alternate $\overline{CE}$ Controlled Writes

Parameter Symbols		Description			Speed Options				
JEDEC	Standard				-45	-55	-70	-90	Unit
t_{AVAV}	t_{WC}	Write Cycle Time		Min	45	55	70	90	ns
t_{AVEL}	t_{AS}	Address Setup Time		Min	0	0	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	35	45	45	45	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	20	25	30	45	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0	0	0	0	ns
	t_{OES}	Output Enable Setup Time		Min	0	0	0	0	ns
	t_{OEH}	Output Enable Hold Time	Read	0	0	0	0	0	ns
			Toggle and Data Polling	10	10	10	10	10	ns
t_{GHEL}	t_{GHEL}	Read Recovery Time before Write ($\overline{OE}$ High to $\overline{CE}$ Low)		Min	0	0	0	0	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ SetupTime		Min	0	0	0	0	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time		Min	0	0	0	0	ns
t_{ELEH}	t_{CP}	Write Pulse Width		Min	25	30	35	45	ns
t_{EHEL}	t_{CPH}	Write Pulse Width High		Min	20	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation		Typ	7	7	7	7	µs
				Max	200	200	200	200	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation		Typ	0.3	0.3	0.3	0.3	s
				Max	5	5	5	5	s
t_{WHWH3}	t_{WHWH3}	Chip Erase Operation		Typ	3	3	3	3	s
				Max	35	35	35	35	s
	t_{VCS}	Vcc Setup Time		Min	50	50	50	50	µs
	t_{VIDR}	Rise Time to V_{ID}		Min	500	500	500	500	ns

Table 11. ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Comments
	Typ	Max	Unit	
Sector Erase Time	0.3	5	sec	Excludes 00H programming prior to erasure
Chip Erase Time	3	35	sec	
Byte Programming Time	7	200	µs	Excludes system level overhead
Chip Programming Time	2	5	sec	
Erase/Program Endurance	100K		cycles	Minimum 100K cycles guaranteed

Table 12. LATCH UP CHARACTERISTICS

Parameter Description	Min	Max
Input voltage with respect to Vss on all pins except I/O pins (including A9 and $\overline{OE}$)	-1.0 V	12.0 V
Input voltage with respect to Vss on all I/O Pins	-1.0 V	Vcc + 1.0 V
Vcc Current	-100 mA	100 mA

Note : These are latch up characteristics and the device should never be put under these conditions. Refer to Absolute Maximum ratings for the actual operating limits.

Table 13. 32-PIN PLCC PIN CAPACITANCE @ 25°C, 1.0MHz

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	8	12	pF

Table 14. 32-PIN TSOP PIN CAPACITANCE @ 25°C, 1.0MHz

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Table 15. DATA RETENTION

Parameter Description	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

SWITCHING WAVEFORMS

Figure 5. AC Waveforms for READ Operations

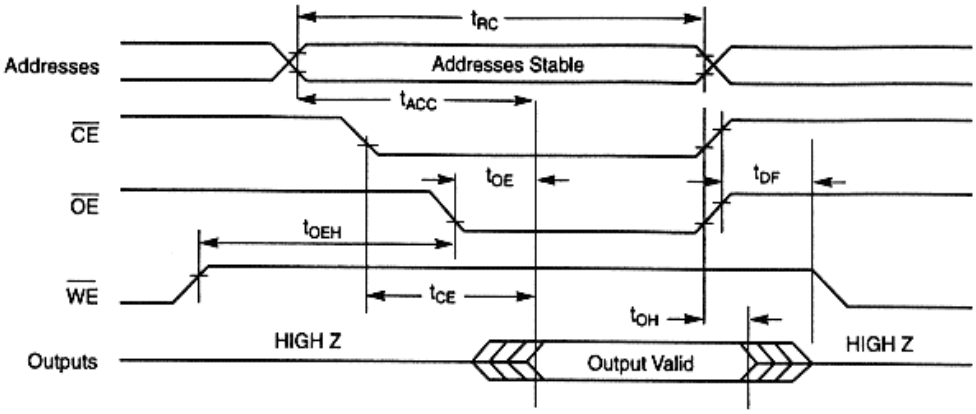
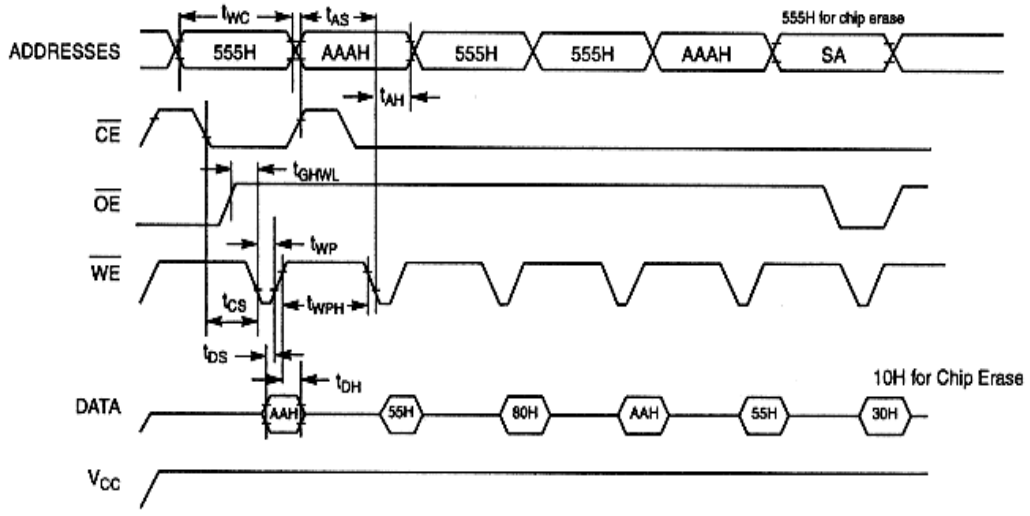


Figure 6. AC Waveforms for Chip/Sector Erase Operations

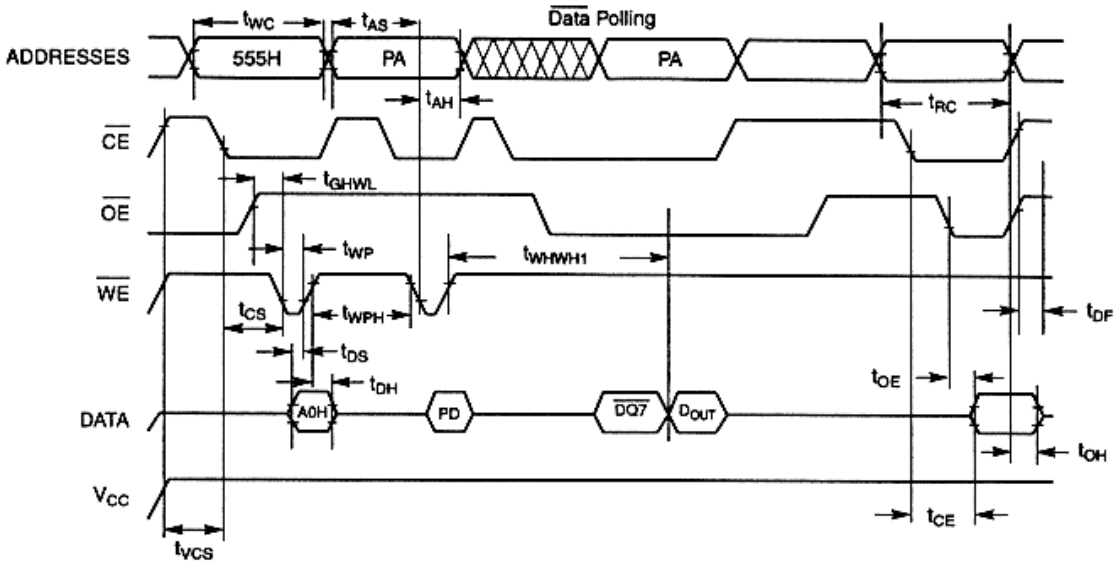


Notes:

1. SA is the Sector address for Sector erase.

SWITCHING WAVEFORMS (continued)

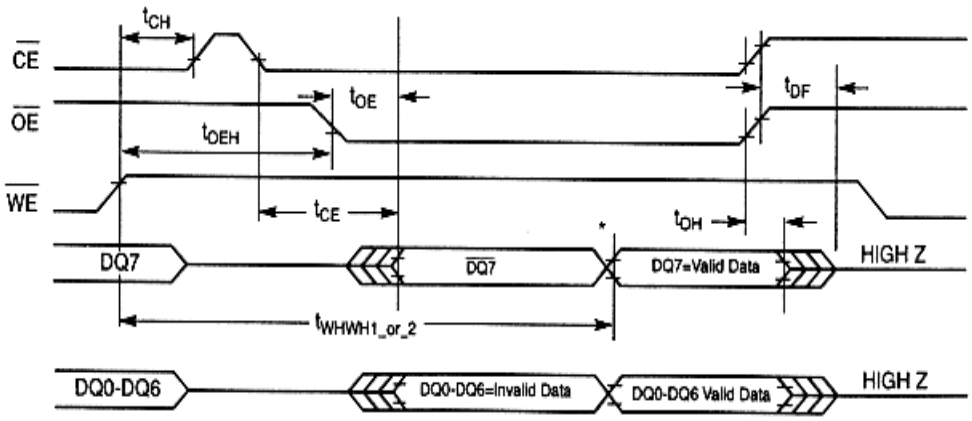
Figure 7. Program Operation Timings



Notes:

1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. /DQ7 is the output of the complement of the data written to the device.
4. D_{OUT} is the output of data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

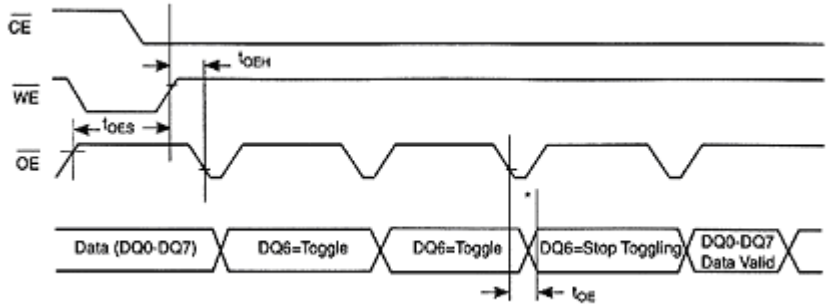
Figure 8. AC Waveforms for /DATA Polling During Embedded Algorithm Operations



Notes:

***** DQ_7 = Valid Data (The device has completed the embedded operation).

Figure 9. AC Waveforms for Toggle Bit During Embedded Algorithm Operations

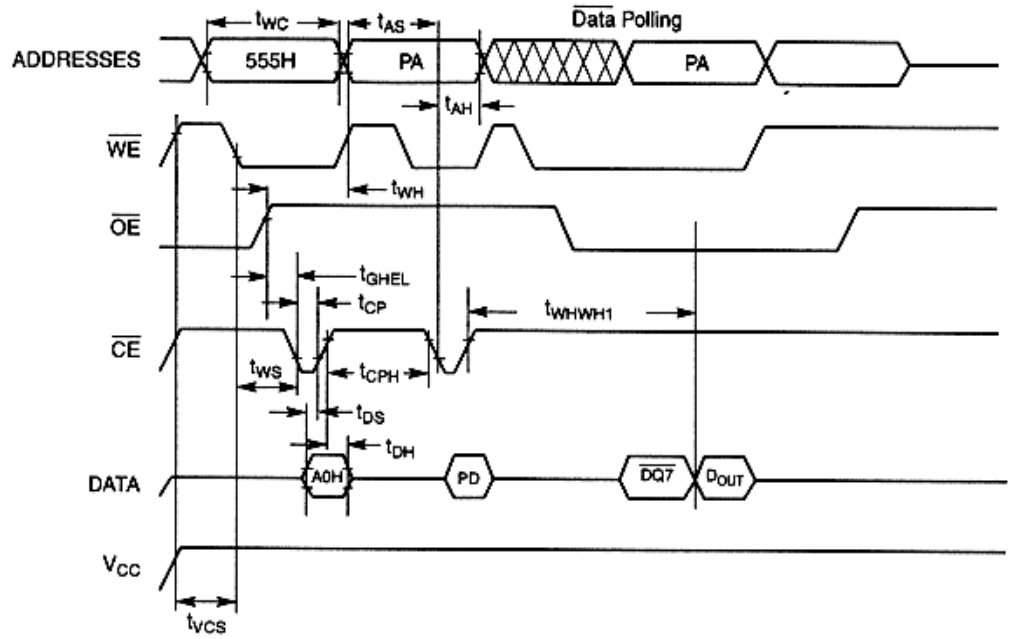


Notes:

***** DQ_6 stops toggling (The device has completed the embedded operation).

SWITCHING WAVEFORMS (continued)

Figure 10. Alternate /CE Controlled Write Operation Timings



Notes:

1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. /DQ7 is the output of the complement of the data written to the device.
4. D_{OUT} is the output of data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

ORDERING INFORMATION

EN29F040 - 45 P I

TEMPERATURE RANGE
(Blank) = Commercial (0°C to +70°C)
I = Industrial (-40°C to +85°C)

PACKAGE
P = 32 Plastic DIP
J = 32 Plastic PLCC
T = 32 Plastic TSOP

SPEED
45 = 45ns
55 = 55ns
70 = 70ns
90 = 90ns

BASE PART NUMBER
EN = EON Silicon Devices
29F = FLASH, 5V
040 = 512K x 8

Revisions List

A,B:

Preliminary

C (2001.07.03):

Pg. 13 Logical Inhibit section now says that if $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$ are all logical zero (not recommended usage), it will be considered a write.

VID is everywhere changed to be V_{ID} =11.5 ± 0.5V

D (2001.07.05):

“block” changed to “sector”

Deleted Sector Un/Protect flow charts (we have a supplement for that)

VID is everywhere changed to be V_{ID} =11.0 ± 0.5V

LACTHUP >= 200mA line removed from first page

Chip erase and Sector Erase command descriptions modified.

DQ7,DQ5,DQ3 status polling descriptions modified.

Table 12 Latchup characteristics modified