Ordering number : EN6142

CMOS IC

LC75742E, 75742W

1/2 Duty VFD Driver with Key Input Function

Overview

The LC75742E and LC75742W are 1/2 duty VFD drivers that can be used for electronic tuning frequency display and other applications under the control of a micro-controller. These products can directly drive VFDs with up to 82 segments. It also includes a key scan circuit and can support input from up to 30 keys and can thus reduce the number of lines to the front panel in application systems.

Features

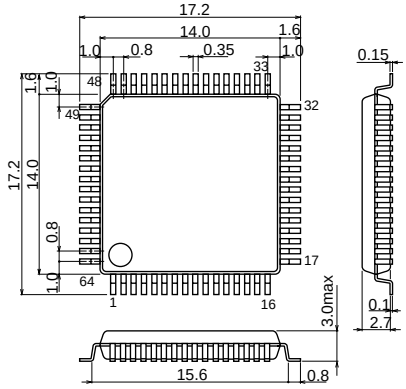
- Key input from up to 30 keys
  (Key scans are only performed when keys are pressed.)
- 82 segment outputs.
- Noise reduction circuits are built into the output drivers.
- Serial data I/O supports CCB format communication with the system controller.
- Dimmer and sleep mode can be controlled by serial data input.
- High generality since display data is displayed without the intervention of a decoder.
- All segments can be turned off with the $\overline{\text{BLK}}$ pin.

Package Dimensions

unit: mm

3151-QFP64E

[LC75742E]

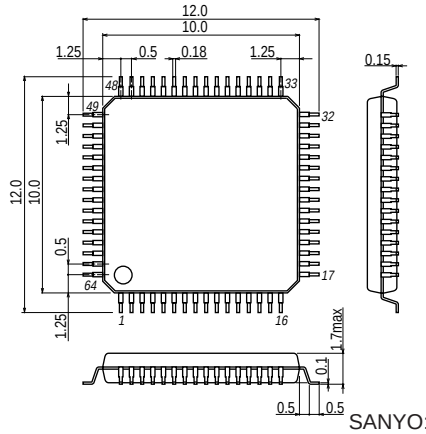


SANYO: QFP64E (QIP64E)

unit: mm

3190-SQFP64

[LC75742W]



SANYO: SQFP64

- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum Supply voltage	V_{DD} max	V_{DD}	–0.3 to +6.5	V
	V_{FL} max	V_{FL}	–0.3 to +21.0	V
Input voltage	$V_{IN}1$	DI, CL, CE, $\overline{BLK}$	–0.3 to +6.5	V
	$V_{IN}2$	OSCI, KI1 to KI5	–0.3 to V_{DD} +0.3	V
Output voltage	$V_{OUT}1$	S1 to S41, G1, G2	–0.3 to V_{FL} +0.3	V
	$V_{OUT}2$	OSCO, KS1 to KS6	–0.3 to V_{DD} +0.3	V
	$V_{OUT}3$	DO	–0.3 to +6.5	V
Output current	$I_{OUT}1$	S1 to S41	6	mA
	$I_{OUT}2$	G1, G2	60	mA
	$I_{OUT}3$	KS1 to KS6	1	mA
Allowable power dissipation	Pd max	Ta = 85°C (LC75742E)	400	mW
		Ta = 85°C (LC75742W)	300	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–50 to +150	°C

Allowable Operating Ranges at Ta = –40 to +85°C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V

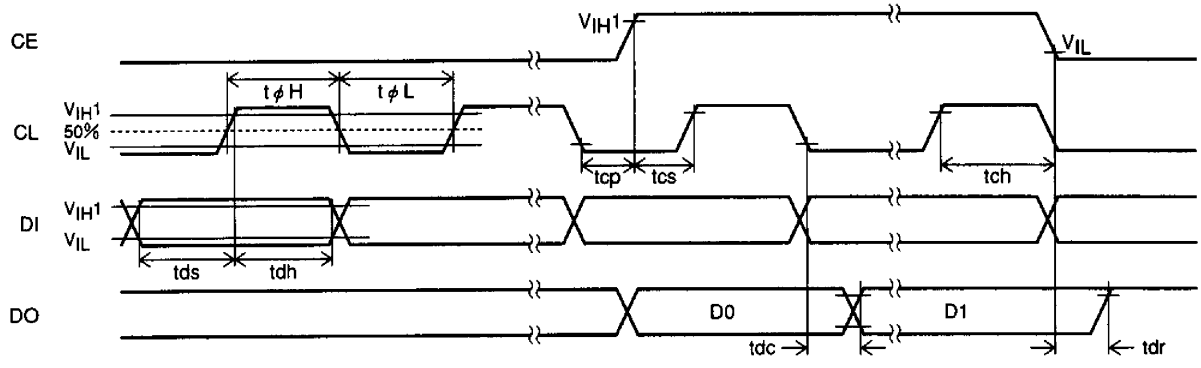
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	4.5	5.0	5.5	V
	V_{FL}	V_{FL}	8	12	18	V
High-level input voltage	$V_{IH}1$	DI, CL, CE, $\overline{BLK}$	0.8 V_{DD}		5.5	V
	$V_{IH}2$	OSCI	0.8 V_{DD}		V_{DD}	V
	$V_{IH}3$	KI1 to KI5	0.6 V_{DD}		V_{DD}	V
Low-level input voltage	V_{IL}	DI, CL, CE, $\overline{BLK}$, OSCI, KI1 to KI5	0		0.2 V_{DD}	V
Guaranteed oscillator frequency range	f_{OSC}	OSCI, OSCO	0.4	1.6	3.0	MHz
Recommended external resistor value	R_{OSC}	OSCI, OSCO	4.7	20	100	kΩ
Recommended external capacitor value	C_{OSC}	OSCI, OSCO	22	47	100	pF
Clock low-level pulse width	$t_{øL}$	CL : See figure 1.	160			ns
Clock high-level pulse width	$t_{øH}$	CL : See figure 1.	160			ns
Data setup time	t_{ds}	DI, CL : See figure 1.	160			ns
Data hold time	t_{dh}	DI, CL : See figure 1.	160			ns
CE wait time	t_{cp}	CE, CL : See figure 1.	160			ns
CE setup time	t_{cs}	CE, CL : See figure 1.	160			ns
CE hold time	t_{ch}	CE, CL : See figure 1.	160			ns
DO output delay time	t_{dc}	DO: R_{PU} = 4.7 kΩ, C_L = 10 pF*: See figure 1.			1.5	µs
DO rise time	t_{dr}	DO: R_{PU} = 4.7 kΩ, C_L = 10 pF*: See figure 1.			1.5	µs
$\overline{BLK}$ switching time	t_c	$\overline{BLK}$, CE : See figure 4.	10			µs

Note: Since DO is an open-drain output, these values will vary with the pull-up resistance R_{PU} and the load capacitance C_L.

Electrical Characteristics in the Allowable Operating Ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
High-level input current	$I_{IH}1$	DI, CL, CE, $\overline{BLK}$: V_{IN} = 5.5 V			5	µA
	$I_{IH}2$	OSCI: $V_{IN} = V_{DD}$			5	µA
Low-level input current	I_{IL}	DI, CL, CE, $\overline{BLK}$, OSCI: V_{IN} = 0 V	–5			µA
Input floating voltage	V_{IF}	KI1 to KI5			0.05 V_{DD}	V
Pull-down resistance	R_{PD}	KI1 to KI5: V_{DD} = 5.0 V	50	100	250	kΩ
Output off leakage current	I_{OFFH}	DO: V_O = 5.5 V			5	µA
High-level output voltage	$V_{OH}1$	S1 to S41: I_O = –2 mA	V_{FL} – 0.6			V
	$V_{OH}2$	G1, G2: I_O = –50 mA	V_{FL} – 1.3			V
	$V_{OH}3$	OSCO: I_O = –0.5 mA	V_{DD} – 2.0			V
	$V_{OH}4$	KS1 to KS6: I_O = –500 µA	V_{DD} – 1.2	V_{DD} – 0.5	V_{DD} – 0.2	V
Low-level output voltage	$V_{OL}1$	S1 to S41, G1, G2: I_O = 50 µA			0.5	V
	$V_{OL}2$	OSCO: I_O = 0.5 mA			2.0	V
	$V_{OL}3$	KS1 to KS6: I_O = 25 µA	0.2	0.5	1.5	V
	$V_{OL}4$	DO: I_O = 1 mA		0.1	0.5	V
Oscillator frequency	f_{OSC}	R_{OSC} = 20 kΩ, C_{OSC} = 47 pF		1.6		MHz
Hysteresis voltage	V_H	DI, CL, CE, $\overline{BLK}$, KI1 to KI5		0.1 V_{DD}		V
Current drain	$I_{DD}1$	Sleep mode			5	µA
	$I_{DD}2$	Outputs open: f_{OSC} = 1.6 MHz			10	mA

• When stopped with CL at the low level



• When stopped with CL at the high level

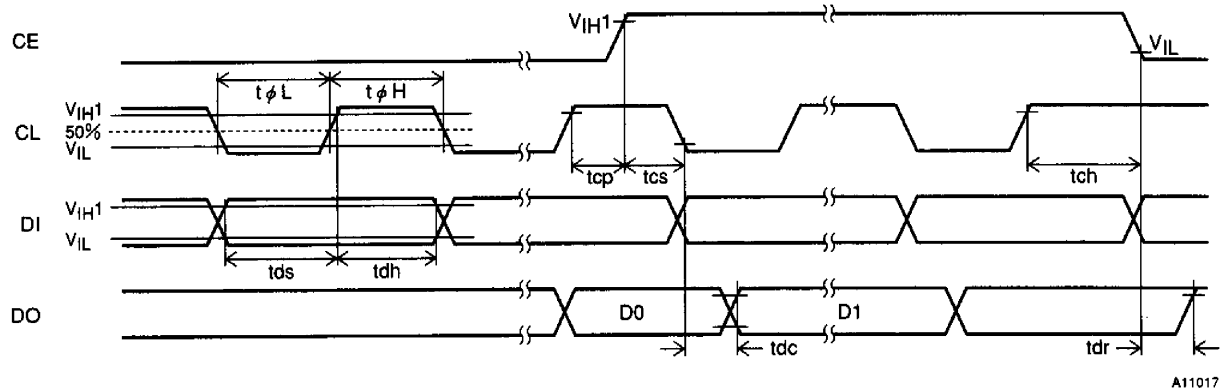
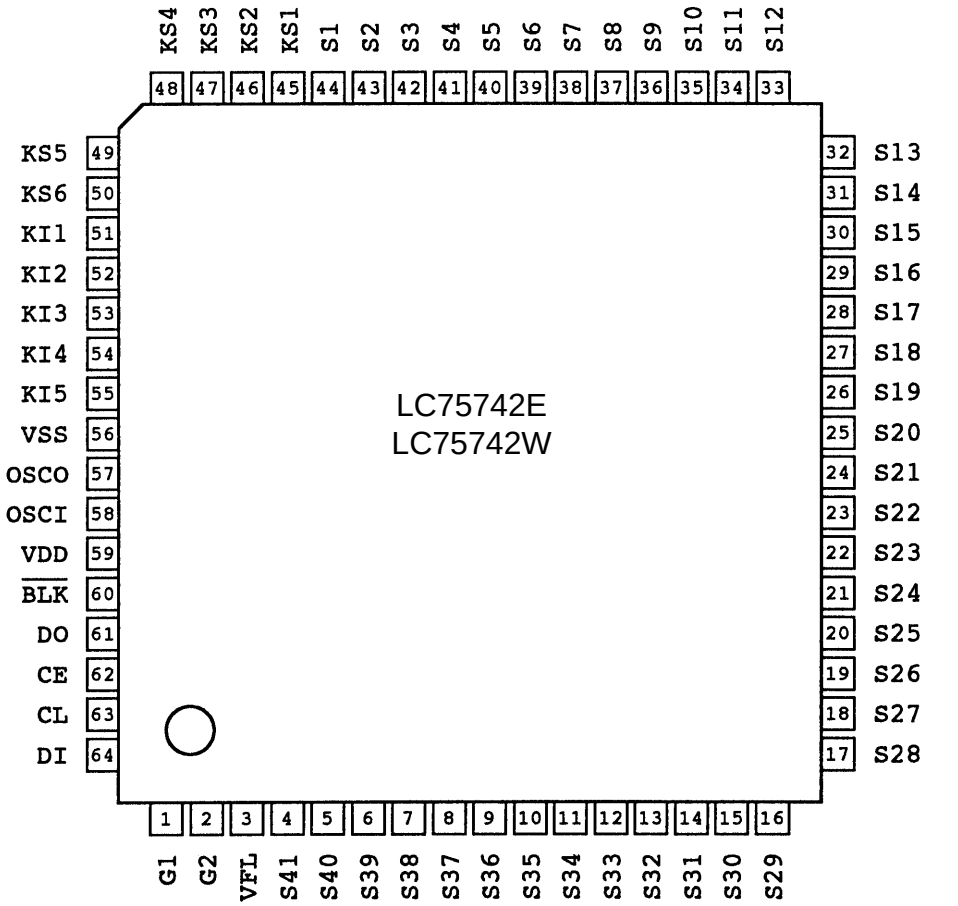


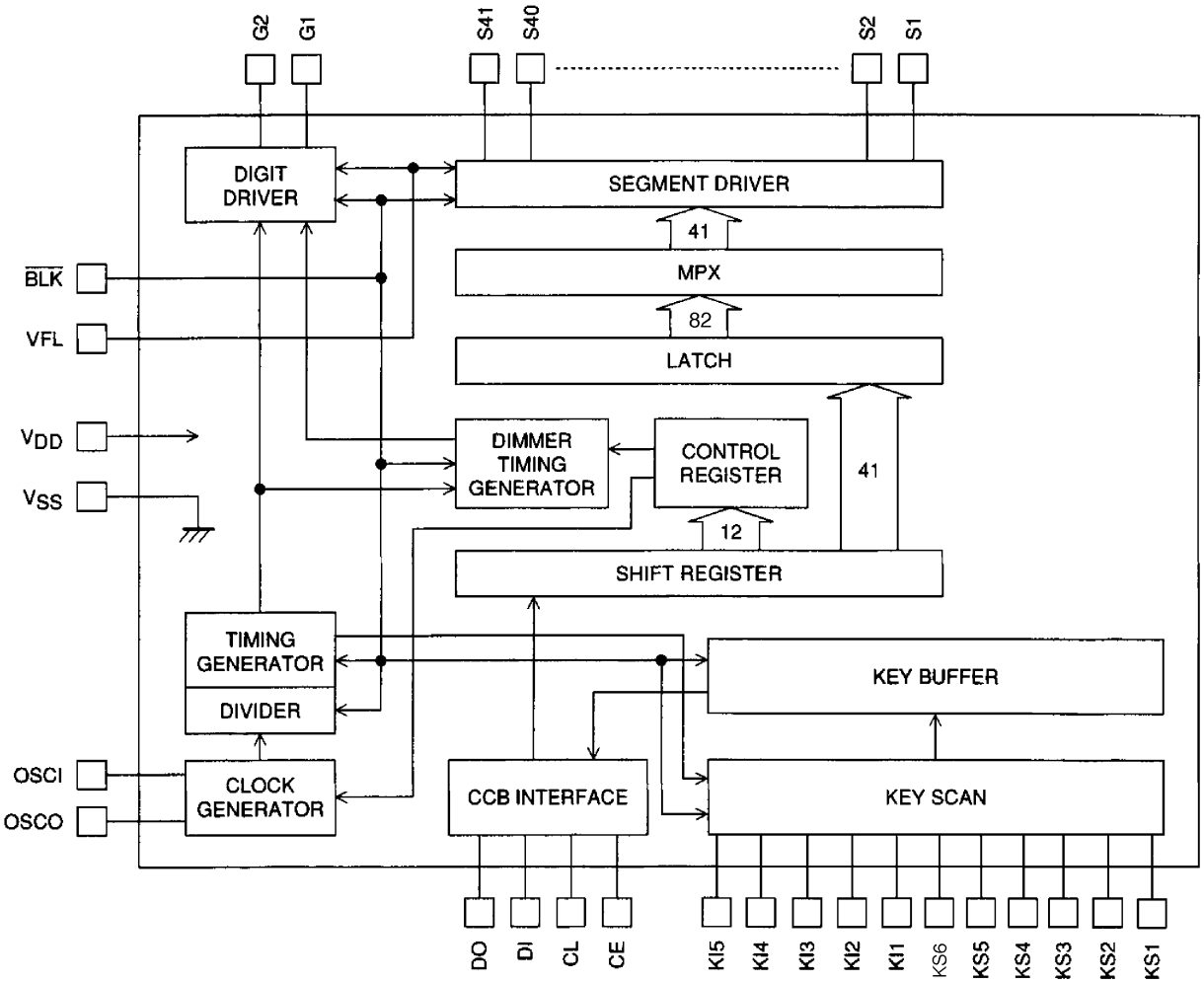
Figure 1

Pin Assignment



Top view

Block Diagram

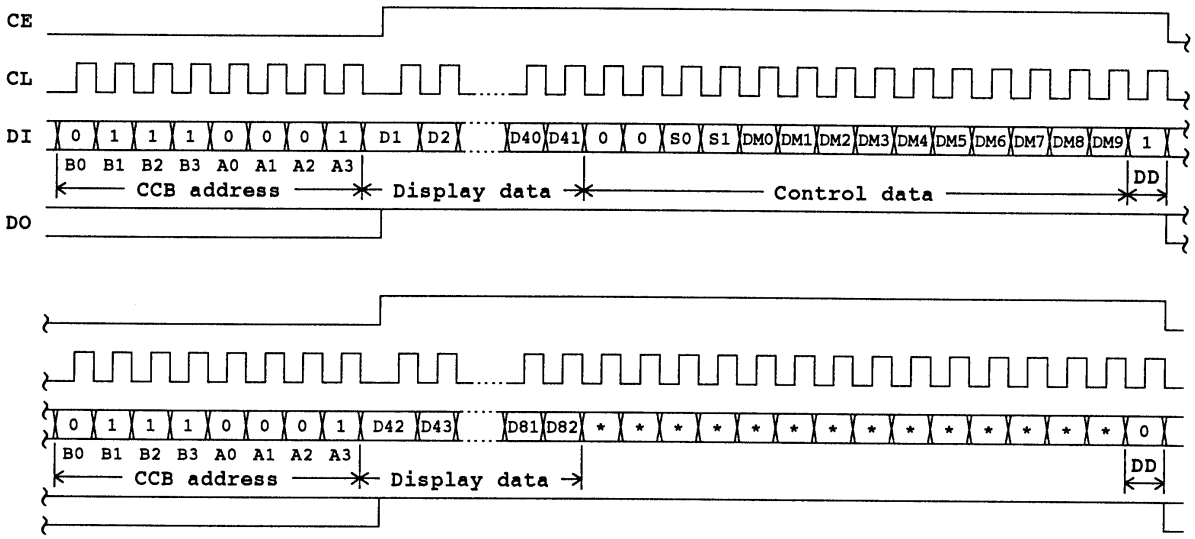


Pin Descriptions

Pin No.	Pin	Function	I/O	Handling when unused
3	V_{FL}	Driver block power supply. Applications must provide a voltage in the range 8.0 to 18.0 V.	—	—
59	V_{DD}	Logic block power supply. Applications must provide a voltage in the range 4.5 to 5.5 V.	—	—
56	V_{SS}	Power supply ground. This pin must be connected to the system ground.	—	—
58	OSCI	Oscillator circuit connections. An oscillator circuit is formed by connecting a resistor and a capacitor externally to these pins.	I	GND
57	OSCO		O	OPEN
60	$\overline{BLK}$	Reset signal input used to initialize the IC internal state. During a reset, the display is turned off forcibly regardless of the internal display data. Also note that the internal key data is all reset to 0 and key scan operations are disabled. However, serial data input is possible in this state.	I	GND
63	CL	Serial data interface. These pins must be connected to the system microcontroller. Note that since DO is an open-drain output, a pull-up resistor is required. CL: Synchronization clock DI: Transfer data CE: Chip enable DO: Output data	I	GND
64	DI			
62	CE			
61	DO		O	OPEN
1, 2	G1, G2	Digit outputs. The frame frequency f_O is (f_{OSC}/4096) Hz.	O	OPEN
44 to 4	S1 to S41	Segment outputs that display the display data transferred over the serial interface.	O	OPEN
45 to 50	KS1 to KS6	Key scan outputs. Normally, when a key matrix is formed, diodes are inserted in the key scan timing lines to prevent shorts. However, since this IC uses unbalanced CMOS outputs in the output transistor circuit, the IC will not be damaged if these outputs are shorted.	O	OPEN
51 to 55	KI1 to KI5	Key scan inputs. Pull-down resistors are built into the IC internal pin circuits.	I	GND

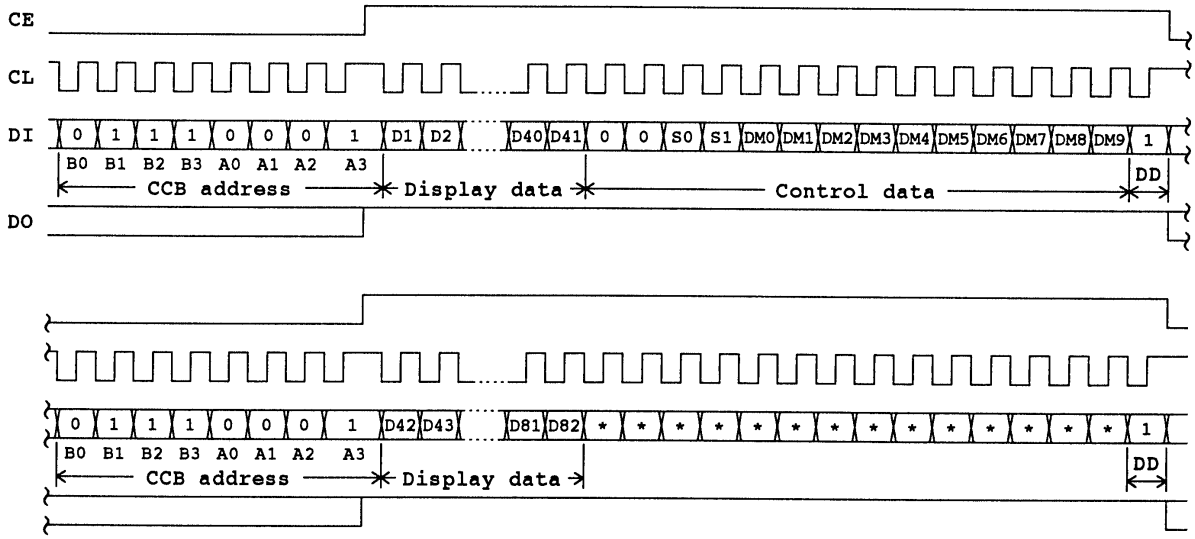
Serial Data Input

• When stopped with CL at the low level



Note: don't care
DD: Direction data

• When stopped with CL at the high level



Note: don't care
DD: Direction data

Figure 2

• CCB address: Applications must send the value 01110001_B ($8E_H$) as shown in figure 2.
• D1 to D41: Segment display data for the G1 digit output pin
Dn (n = 1 to 41) = 1: Segment on
Dn (n = 1 to 41) = 0: Segment off
• D42 to D82: Segment display data for the G2 digit output pin
Dn (n = 42 to 82) = 1: Segment on
Dn (n = 42 to 82) = 0: Segment off
• S0, S1: Sleep control data
• DM0 to DM9: Dimmer data

Control Data

• S0, S1: Sleep control data

This control data controls switching between sleep mode and normal mode, and also sets the states of the KS1 to KS6 key scan output pins in key scan standby mode.

Control data		Mode	Clock generator (oscillator circuit)	Segment outputs Digit output	Output pin states during key scan standby					
S0	S1				KS1	KS2	KS3	KS4	KS5	KS6
0	0	Normal	Oscillator operating	Operating	H	H	H	H	H	H
0	1	Sleep	Stopped	L	L	L	L	L	L	H
1	0	Sleep	Stopped	L	L	L	L	L	H	H
1	1	Sleep	Stopped	L	H	H	H	H	H	H

• DM0 to DM9: Dimmer data

This data controls the duty of the G1, G2 digit output pins. This data forms a 10-bit binary value in which D0 is the LSB. The brightness of the display can be controlled by adjusting the duty of the G1, G2 digit output pins. The table lists the relationship between the dimmer data and the dimmer value.

DM9	DM8	DM7	DM6	DM5	DM4	DM3	DM2	DM1	DM0	Dimmer value (t4/t3)
0	0	0	0	0	0	0	0	0	0	0/1024
0	0	0	0	0	0	0	0	0	1	1/1024
0	0	0	0	0	0	0	0	1	0	2/1024
					to					to
1	1	1	1	1	1	1	1	0	0	1020/1024
1	1	1	1	1	1	1	1	0	1	1021/1024
1	1	1	1	1	1	1	1	1	0	1022/1024
1	1	1	1	1	1	1	1	1	1	Illegal setting

t3 and t4: See figure 5.

Relationship between the Display Data (D1 to D82) and the Segment Output Pins

Segment output pin	G1	G2
S1	D1	D42
S2	D2	D43
S3	D3	D44
S4	D4	D45
S5	D5	D46
S6	D6	D47
S7	D7	D48
S8	D8	D49
S9	D9	D50
S10	D10	D51
S11	D11	D52
S12	D12	D53
S13	D13	D54
S14	D14	D55

Segment output pin	G1	G2
S15	D15	D56
S16	D16	D57
S17	D17	D58
S18	D18	D59
S19	D19	D60
S20	D20	D61
S21	D21	D62
S22	D22	D63
S23	D23	D64
S24	D24	D65
S25	D25	D66
S26	D26	D67
S27	D27	D68
S28	D28	D69

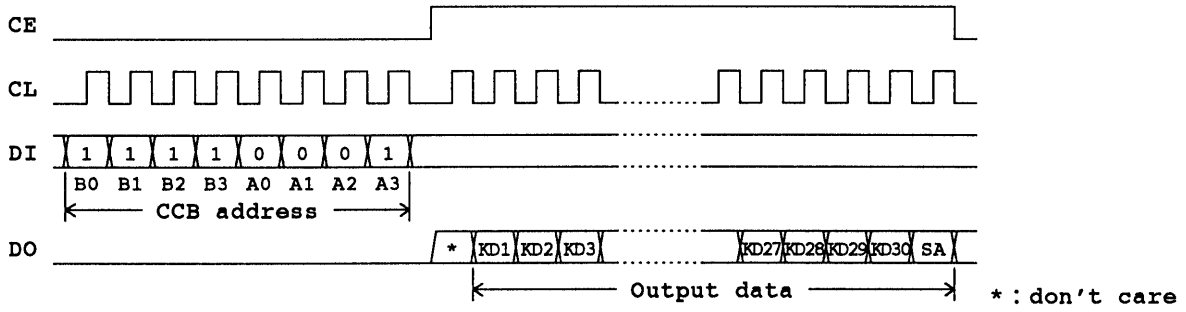
Segment output pin	G1	G2
S29	D29	D70
S30	D30	D71
S31	D31	D72
S32	D32	D73
S33	D33	D74
S34	D34	D75
S35	D35	D76
S36	D36	D77
S37	D37	D78
S38	D38	D79
S39	D39	D80
S40	D40	D81
S41	D41	D82

As an example, the table below lists the operation of the S11 segment output pin.

Display data		Segment output pin (S11) state
D11	D52	
0	0	The segments corresponding to the G1 and G2 digit output pins are off
0	1	The segment corresponding to the G2 digit output pin is turned on
1	0	The segment corresponding to the G1 digit output pin is on
1	1	The segments corresponding to the G1 and G2 digit output pins are on

Serial Data Output

• When stopped with CL at the low level



• When stopped with CL at the high level

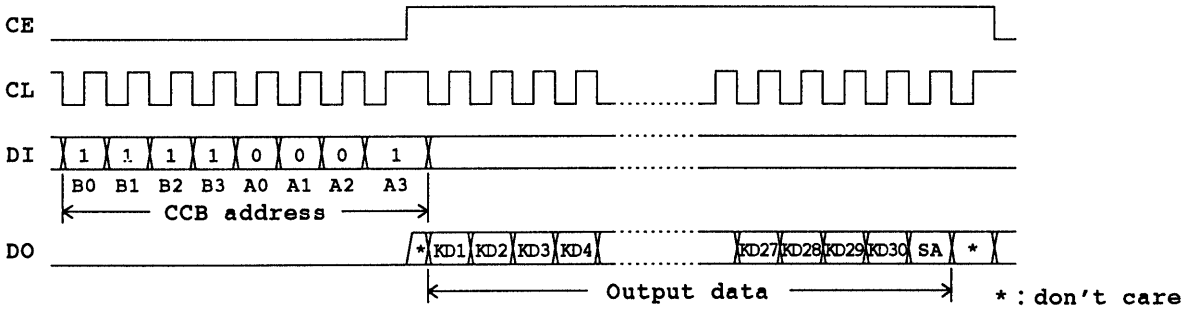


Figure 3

• CCB address: Applications must send the value 11110001_B ($8F_H$) as shown in figure 3.
• KD1 to KD30: Key data
• SA: Sleep acknowledge data

Note: The key data (KD1 to KD30) and the sleep acknowledge data (SA) will be invalid if the key data is read when DO is high.

Output Data

• KD1 to KD30: Key data

These bits represent the key output states when a key matrix with up to 30 keys is formed using the KS1 to KS6 key scan output pins and the KI1 to KI5 key scan input pins. When a key is pressed, the bit corresponding to that key will be set to 1. The correspondence is listed in the following table.

Item	KI1	KI2	KI3	KI4	KI5
KS1	KD1	KD2	KD3	KD4	KD5
KS2	KD6	KD7	KD8	KD9	KD10
KS3	KD11	KD12	KD13	KD14	KD15
KS4	KD16	KD17	KD18	KD19	KD20
KS5	KD21	KD22	KD23	KD24	KD25
KS6	KD26	KD27	KD28	KD29	KD30

• SA: Sleep acknowledge data

This output data is set to the state when the key was pressed. In that case DO will go to the low level. If serial data is input during this period and the mode is set (normal mode or sleep mode), the IC will be set to that mode. SA is set to 1 in the sleep mode and to 0 in the normal mode.

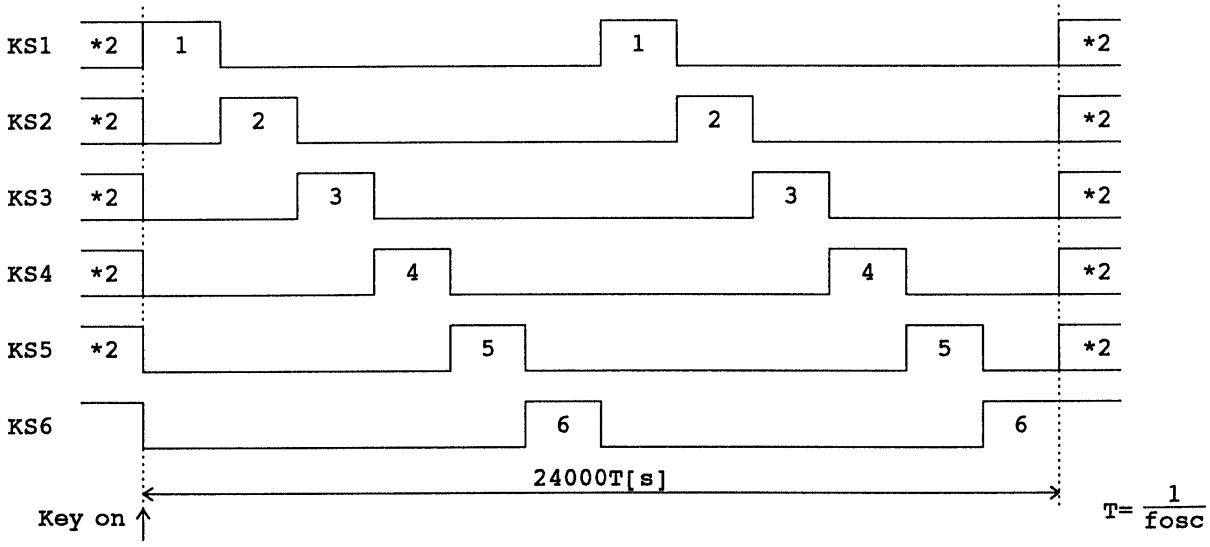
Sleep Mode

The IC is set to sleep mode by setting either S0 or S1 in the control data to 1. The segment outputs and the digit outputs are all set low, and the clock generator (oscillator circuit) is stopped (although it is restarted when a key is pressed), and thus power dissipation is reduced. This mode is cleared by setting S0 and S1 in the control data to 0.

Key Scan Operation

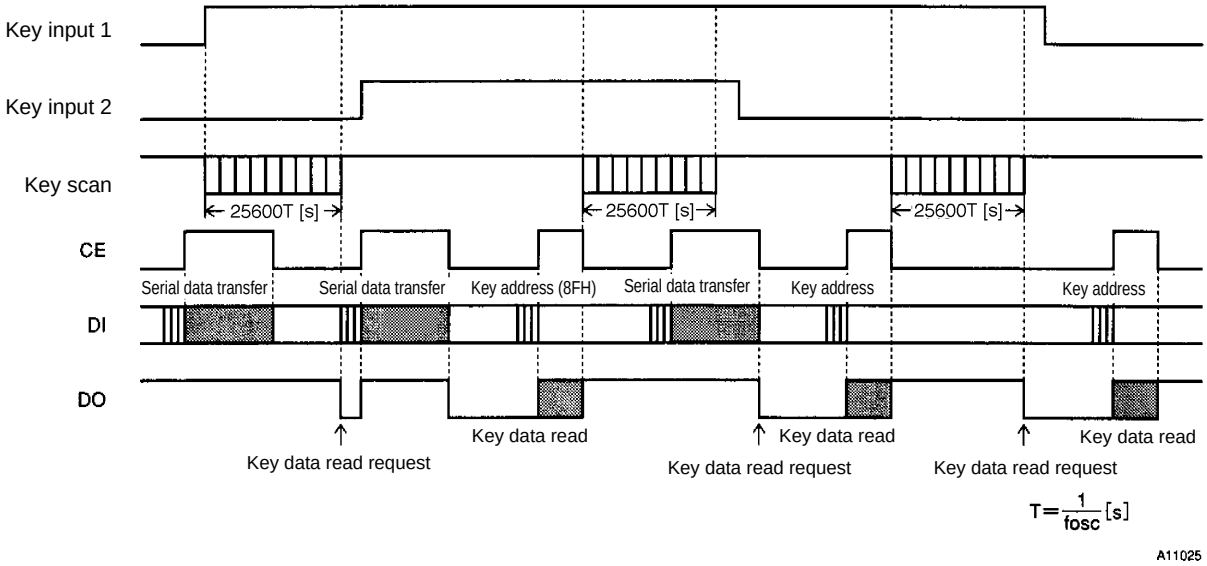
• Key scan timing

The scan period is 12000T [s]. A key scan is performed twice to reliably recognize the key on/off states by verifying that the key data for the two scans agrees. If the data agrees, the IC recognizes a key press and 25600T [s] after the start of key scan execution issues a key scan data read request by outputting a low level from DO. If the key data does not agree and a key was pressed at the later scan, the IC executes another key scan operation. Note that this means that this IC cannot recognize a key press shorter than 25600T [s].



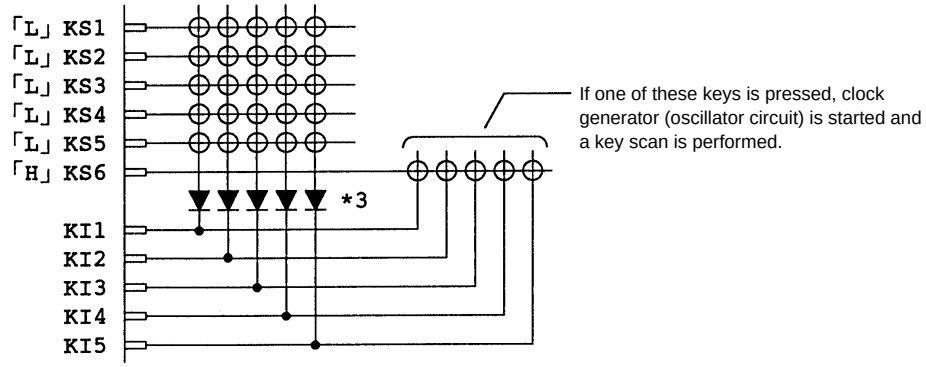
Note *: The high-level and low-level states in sleep mode are set according to the control data S0 and S1. Key scan output signals are not output from pins set to the “L” state.

- In normal mode
  - — The pins KS1 to KS6 are set high.
  - — A key scan is started when any of the keys is pressed, and the keys are kept scanning until all keys are released. The controller can recognize simultaneous multiple key presses by checking the key data for multiple bits being set.
  - — If a key is pressed for over 25600T [s] (where T = $1/f_{OSC}$), the IC outputs a key data read request to the controller by setting DO low. The controller acknowledges this state and reads the key data. However, note that DO will go high when CE is set high during the serial data transfer.
  - — After the controller key data readout completes, the key data read request will be cleared (DO will be set high), and the IC performs another key scan. Note that since DO is an open-drain output, a pull-up resistor (between 1 and 10 kΩ) is required.

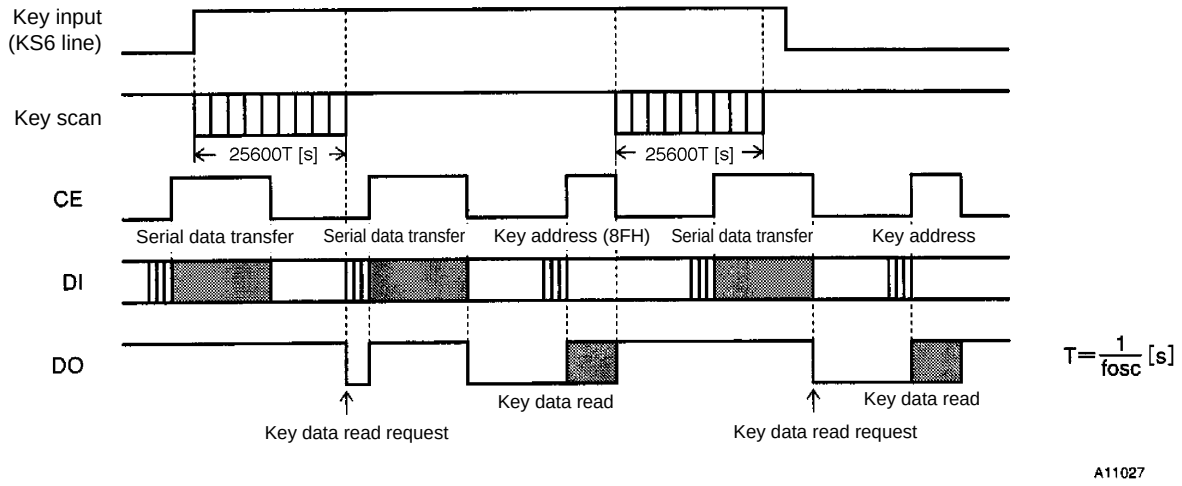


- In sleep mode
  - — The pins KS1 to KS6 are set to high or low according to the values of S0 and S1 in the control data. (See the description of the control data elsewhere in this document.)
  - — If a key connected to one of the KS1 to KS6 lines that was set high is pressed, the clock generator (oscillator circuit) is started and a key scan is performed, and the keys are kept scanning until all keys are released. The controller can recognize simultaneous multiple key presses by checking the key data for multiple bits being set.
  - — If a key is pressed for over 25600T [s] (where T = $1/f_{OSC}$), the IC outputs a key data read request to the controller by setting DO low. The controller acknowledges this state and reads the key data. However, note that DO will go high when CE is set high during the serial data transfer.
  - — After the controller key data readout completes, the key data read request will be cleared (DO will be set high), and the IC performs another key scan. However, sleep mode will not be cleared. Note that since DO is an open-drain output, a pull-up resistor (between 1 and 10 kΩ) is required.
  - — Example of a key scan operation in sleep mode

Example: Sleep mode with S0 = 0, S1 = 1 (Only KS6 is set high)



Note *: These diodes are required to reliably recognize multiple key presses on the KS6 line when the IC is set to sleep mode with only KS6 set to high as in the example above. That is, they prevent incorrect recognition of key presses due to sneak currents arising from simultaneous presses of keys on the KS1 through KS5 lines.



Multiple Key Presses

The LC75742E/W, even without diodes in the key scan lines, can scan for any combination of dual key presses, any combination of triple key presses on any of the KI1 to KI5 key scan input pin lines, or any combination of multiple key presses on any of the KS1 to KS6 key scan output lines. However, keys that are not pressed may be seen as having been pressed for any other multiple key press combination. Accordingly, applications must insert diodes at each key. Also, to reject any triple and higher multiple key presses, if three or more data readout are 1 ignore the data by the software or in other ways.

Notes on the $\overline{\text{BLK}}$ Pin and Display Control

Since the states of the IC internal data (D1 to D82, and the control data) are undefined when power is first applied, applications should turn off the display (i.e. set S1 to S41, and G1 and G2 low) by setting the $\overline{\text{BLK}}$ pin low at the same time as power is applied. Applications should transfer all 128 bits of the serial data while $\overline{\text{BLK}}$ is held low, and only then set $\overline{\text{BLK}}$ high. This will prevent random meaningless display at power on. (See figure 4.)

Note on the Power on Sequence

Applications must observe the following sequences when turning the power on or off.

- At power on: First turn on the logic system power (V_{DD}), and then turn on the driver power (V_{FL})
- At power off: First turn off the driver power (V_{FL}), and then turn off the logic system power (V_{DD}).

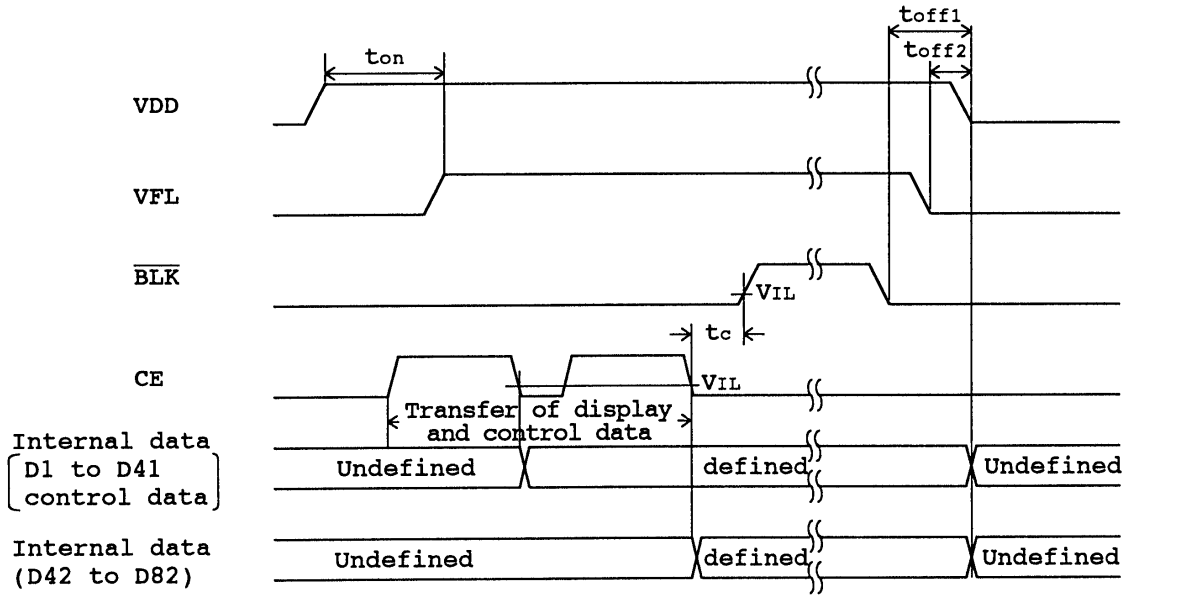


Figure 4

Output Waveforms (S1 to S41)

G1

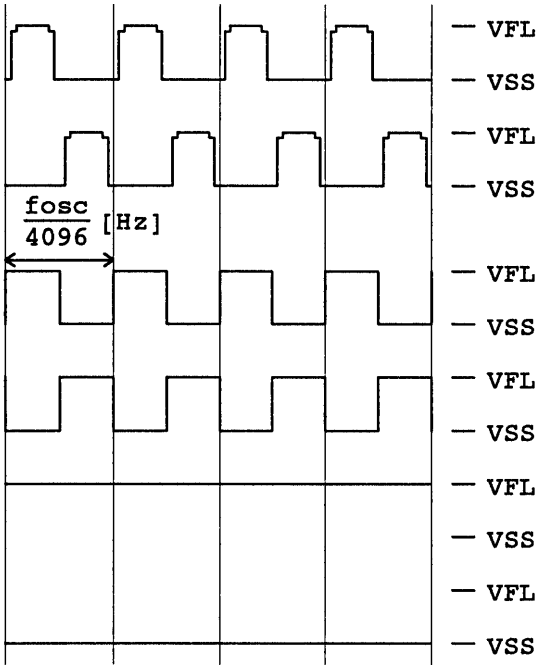
G2

S1 to S41 waveform when the segment corresponding to G1 is on.

S1 to S41 waveform when the segment corresponding to G2 is on.

S1 to S41 waveform when the seguments corresponding to G1 and G2 are on.

S1 to S41 waveform when the seguments corresponding to G1 and G2 are off.



Relationship between the Segment and Digit Outputs

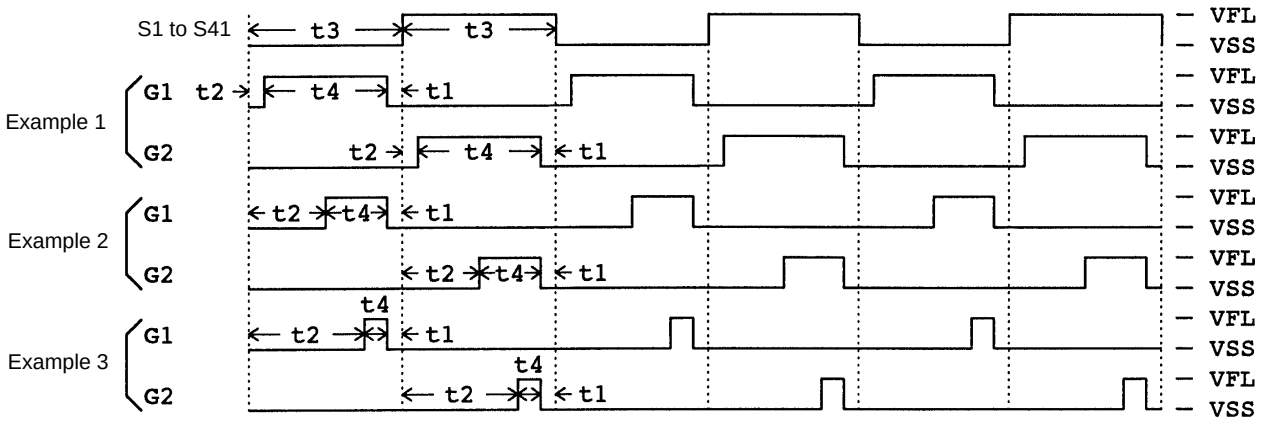


Figure 5

- Figure 5 shows the case where the display data is set up so that the segment outputs S1 to S41 output the V_{SS} level with the same timing as the G1 and G2 digit outputs, and output the V_{FL} level with the same timing as the G2 digit output. Here, the segments corresponding to G2 will be turned on. The relationship between t3 and the oscillator frequency f_{OSC} in this case is $t3 = 2048/f_{OSC}$.
- The G1 and G2 digit output waveforms in example 1 correspond to a dimmer data (DM0 to DM9) set to $3FE_H$. The relationship between t1 and the oscillator frequency f_{OSC} is $t1 = 2/f_{OSC}$. Note that t1 and t2 in example 1 are identical times.
- The G1 and G2 digit output waveforms in example 2 correspond to a dimmer data (DM0 to DM9) set to a smaller value. Although t1 does not change, t2 becomes longer. Here, if the dimmer data (DM0 to DM9) is set to $1FF_H$ and the oscillator frequency f_{OSC} is 1.6 MHz, then t2 can be calculated as follows.

$$t2 = t3 - t1 \times (1FF_H + 1)$$

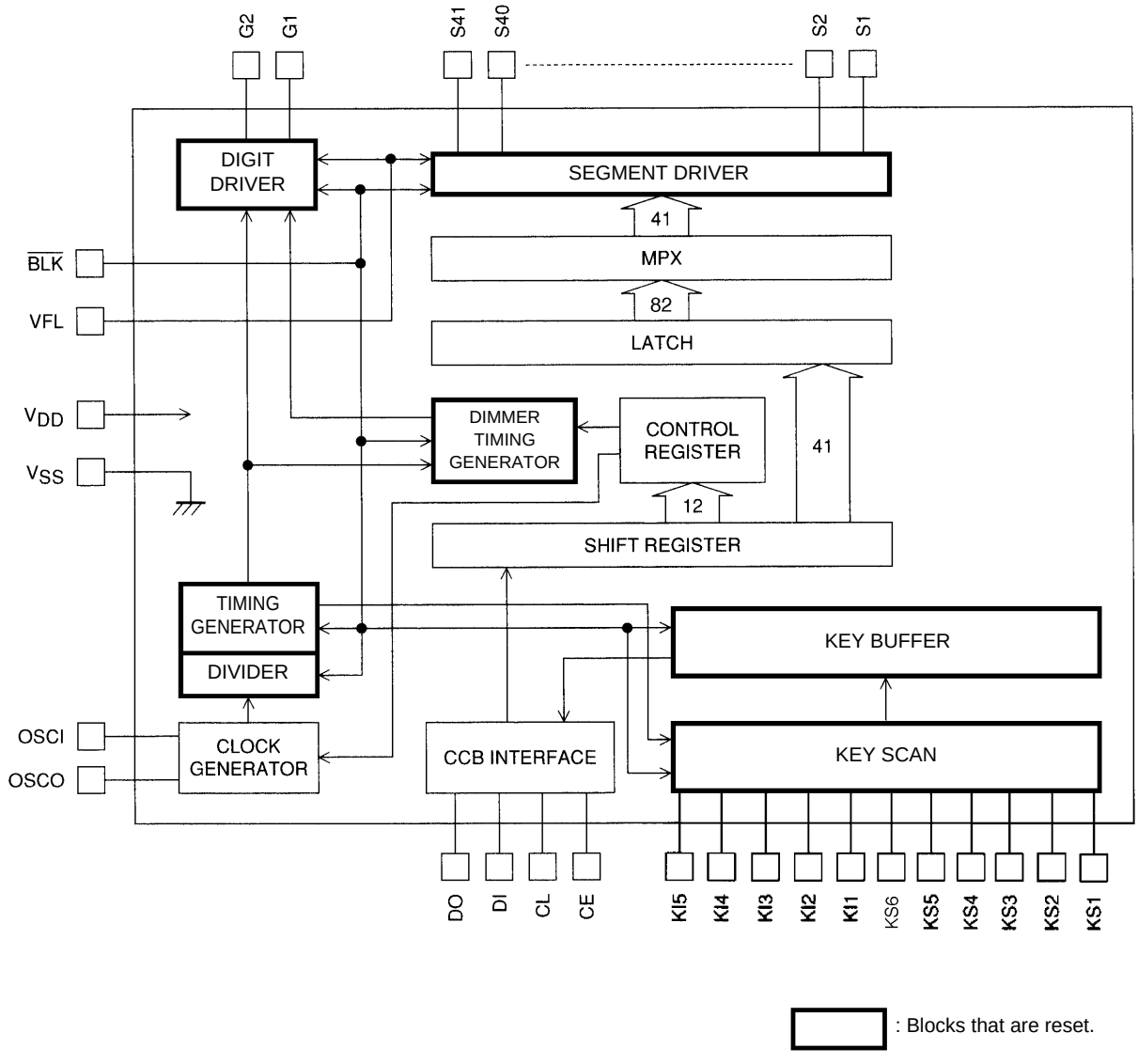
$$= \frac{1024}{f_{OSC}}$$

$$= 0.64 \text{ [ms]}$$

- If the dimmer data (DM0 to DM9) is set to an even smaller value, t2 will become even longer as shown in example 3. Note that t1 does not change in this case as well.

Block States during the Reset Period (when $\overline{\text{BLK}}$ is low)

- Divider and timing generator
  These circuits are reset and their base clock is stopped.
- Dimmer timing generator
  The circuit is reset and its operation is stopped.
- Digit and segment drivers
  These circuits are reset and the display is turned off (S1 to S41 and G1 and G2 are set low.)
- Key scan
  The circuit is reset, its internal circuits are set to the initial state, and key scanning is disabled.
- Key buffer
  The circuit is reset and all data is set to 0.
- Clock generator
  The state (normal or sleep mode) of this block (the clock oscillator circuit) is determined after the sleep control data (S0 and S1) is transferred.
- CCB interface, shift register, control register, latch, and multiplexer
  These circuits are not reset so that serial data can be input during the reset period.

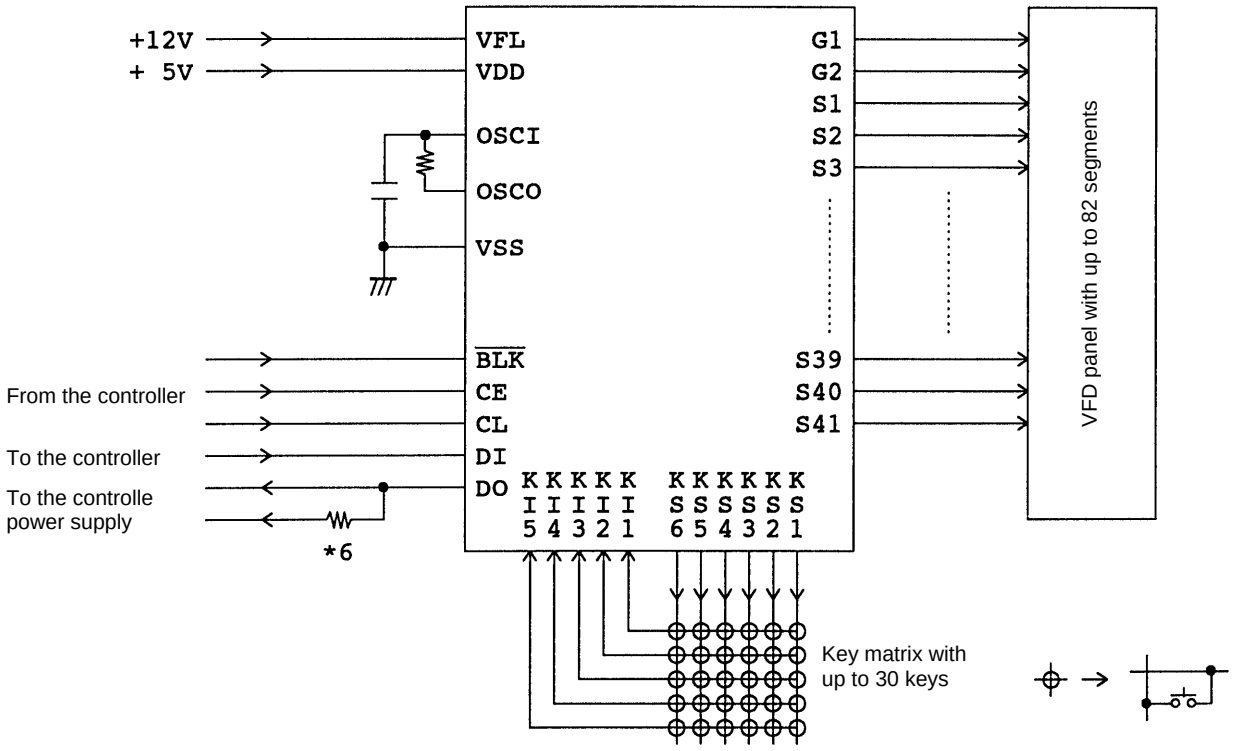


Output Pin States during the Reset Period (when $\overline{BLK}$ is low)

Output pin	State during reset
S1 to S41	L
G1, G2	L
KS1 to KS5	X *1
KS6	H
DO	H *2

Notes: 1. The state of this pin is undefined after power has been applied until the sleep control data (S0 and S1) are transferred.
2. Since this pin is an open-drain output, a pull-up resistor (between 1 and 10 kΩ) is required. It remains high during the reset period even if the controller attempts to read the key data.

Sample Application Circuit



Note *: Since DO is an open-drain output, a pull-up resistor is required. Select a value in the range 1 to 10 kΩ that is most appropriate for the capacitance of the external lines so that the waveform is not distorted.

Notes on the Segment and Digit Waveforms

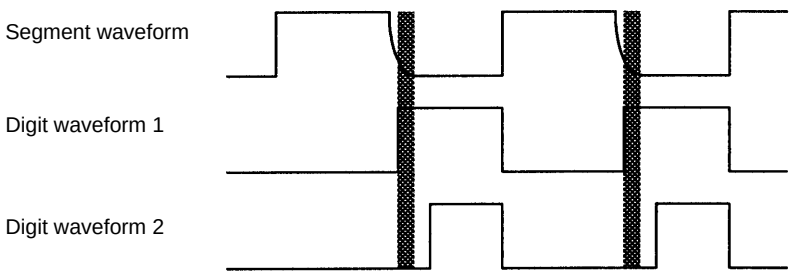


Figure 6

The segment waveform is somewhat deformed due to the VFD panel itself and the circuit wiring. Furthermore, if a digit waveform such as digit waveform 1 in which no dimming is applied is used, the display will glow dimly. Therefore, applications must take this waveform deformation into account and apply adequate dimming such as that shown in digit waveform 2 so that this phenomenon does not occur.

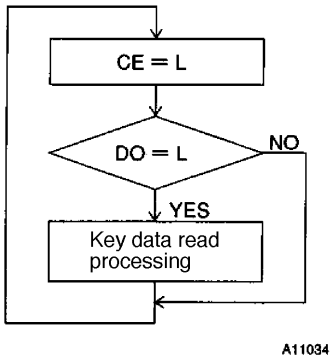
Notes on Controller Transfer of Display Data

Since the display data (D1 to D82) is transferred in two operations as shown in figure 2, we strongly recommend that applications transfer all the data within a 30 ms period to assure display quality.

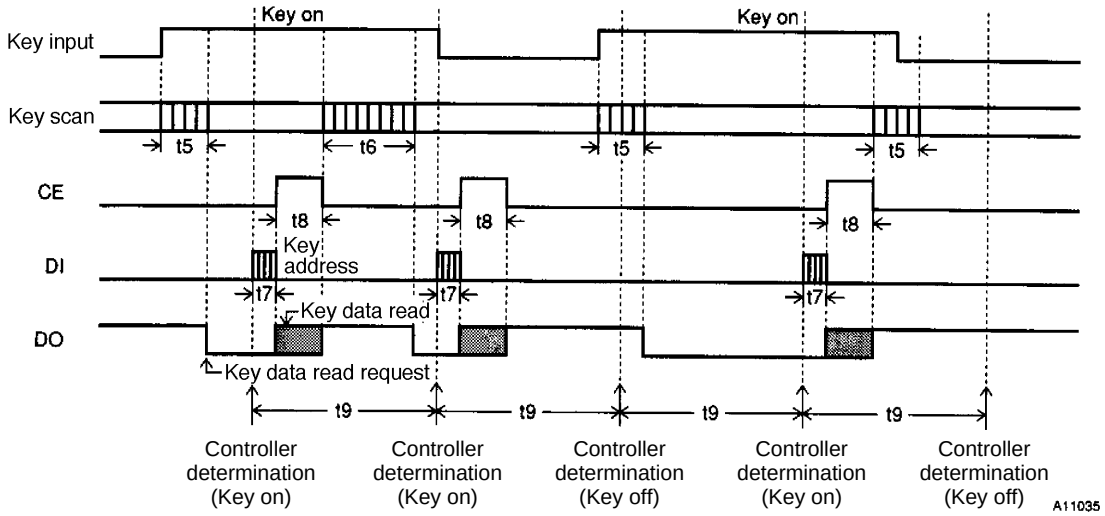
Controller Key Data Readout Procedure

When the controller uses a timer to read out the key data

• Flowchart



• Timing chart



t5·····Key scan execution time (25600T [s]) when the key data for two key scan operations matches.

t6 ·····Key scan execution time (51200T [s]) when the key data for the first two key scan operations does not match.

t7·····Key address ($8F_H$) transfer time

t8·····Key data readout time

$$T = \frac{1}{f_{OSC}} \text{ [s]}$$

• Operation

When the controller use timer processing for key on/off determination and key data readout, it must set CE low and check the state of DO at least once every t9 period. If DO is low, the controller must recognize that a key has been pressed and read out the key data.

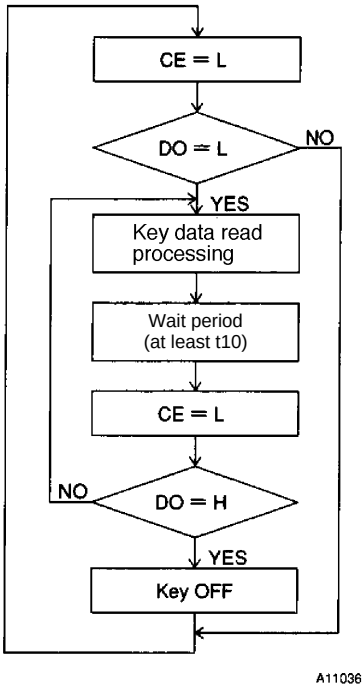
The period t9 must obey the following inequality:

$t9 > t7 + t8 + t6$

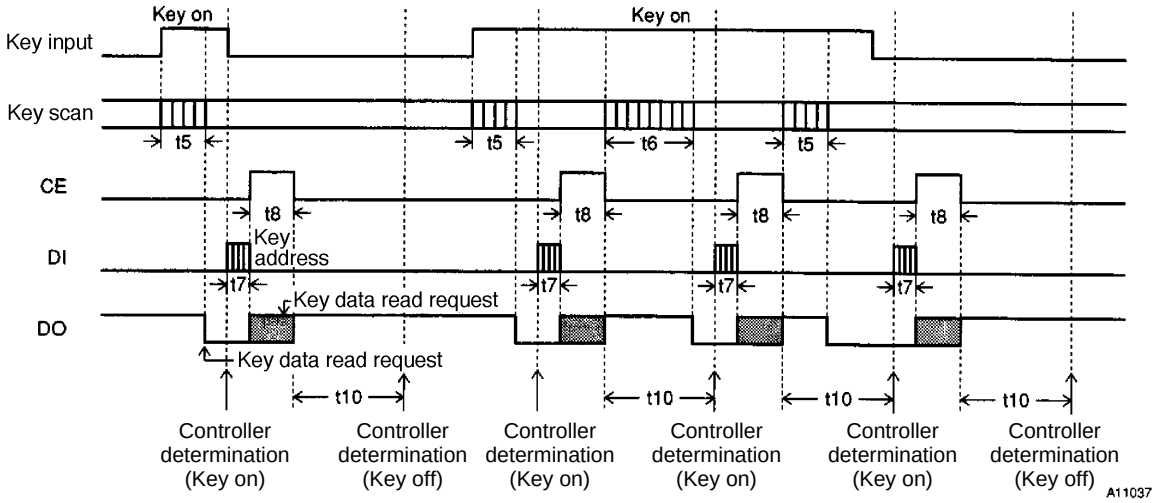
Note that if the controller reads out key data when DO is high, both the key data (KD1 to KD30) and the sleep acknowledge data will be invalid data.

When the controller uses interrupt processing to read out the key data

• Flowchart



• Timing chart



t5.....Key scan execution time (25600T [s]) when the key data for two key scan operations matches.

t6.....Key scan execution time (51200T [s]) when the key data for the first two key scan operations does not match.

t7..... Key address ($8F_H$) transfer time $T = \frac{1}{f_{OSC}}$ [s]

t8.....Key data readout time

• Operation

When the controller uses interrupt processing for key on/off determination and key data readout, it must check the state of DO when CE is low, and perform a key data readout if DO is low. The next time the controller checks the on/off states of the keys, it must make that determination at a time t10 after the last readout based on the state of DO when CE is low, and then read out the key data. The time t10 must obey the following inequality:

$t10 > t6$

Note that if the controller reads out key data when DO is high, both the key data (KD1 to KD30) and the sleep acknowledge data will be invalid data.