MH1M144CXTJ-6

FAST PAGE MODE 150994944-BIT (1048576-WORD BY 144-BIT)DYNAMIC RAM

DESCRIPTION

The MH1M144CXTJ is 1048576-word by 144-bit dynamic RAM module. This consists of nine industry standard 1Mx16 dynamic RAMs in TSOP and one industry standard input buffer in T-SSOP.

The mounting of TSOP on a card edge Dual Read Out package provides any application where high densities and large quantities of memory are required.

This is a socket type - memory modules, suitable for easy interchange or addition of modules.

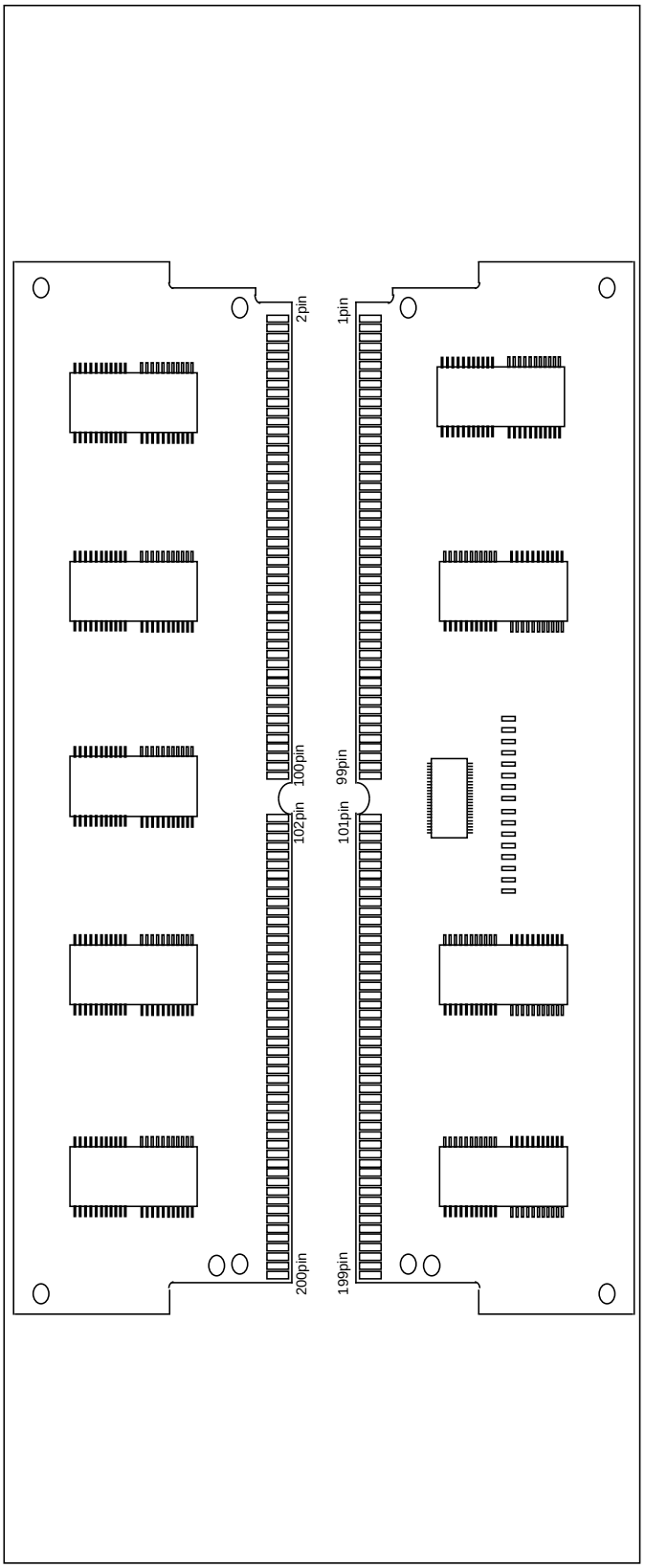
FEATURES

	RAS access time (max.ns)	CAS access time (max.ns)	Address access time (max.ns)	Cycle time (min.ns)
-6	65	20	35	110

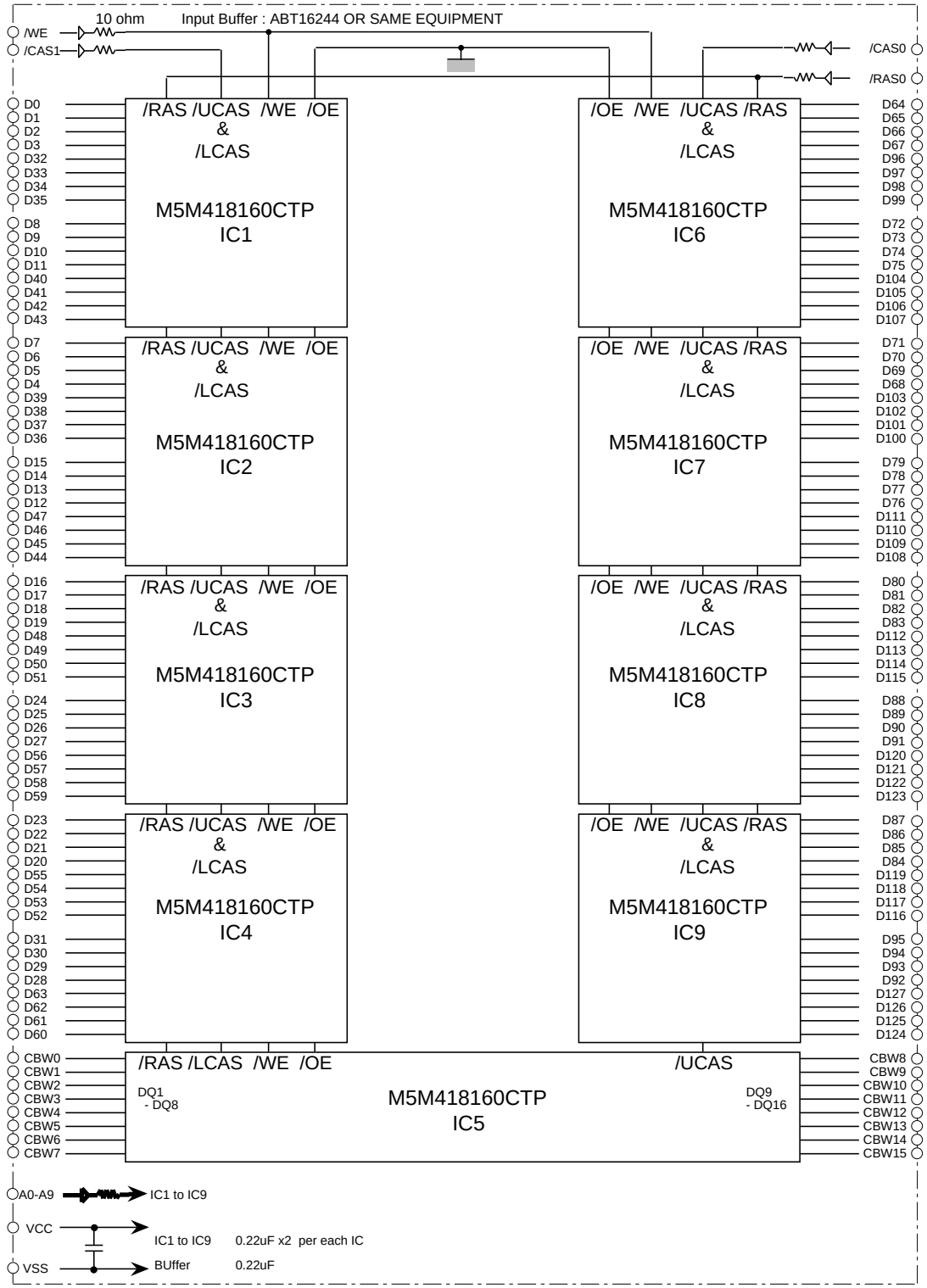
- single 5V±5% supply
- All input, output TTL compatible and low capacitance
- 1024 refresh cycle every 16.4ms(A0~A9)
- Includes decoupling capacitor(0.22µFx19)

APPLICATION

Main memory unit for computer,Microcomputer memory



BLOCK DIAGRAM



PIN CONFIGURATION

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	VSS	51	D49	101	VSS	151	VCC
2	VSS	52	D54	102	VSS	152	VCC
3	D0	53	D50	103	A6	153	D75
4	D7	54	D53	104	A7	154	D76
5	D1	55	D51	105	A8	155	D104
6	D6	56	D52	106	A9	156	D111
7	D2	57	D24	107	NC	157	D105
8	D5	58	D31	108	NC	158	D110
9	D3	59	D25	109	NC	159	D106
10	D4	60	D30	110	WE	160	D109
11	D32	61	D26	111	NC	161	D107
12	D39	62	D29	112	NC	162	D108
13	D33	63	D27	113	VSS	163	D80
14	D38	64	D28	114	VSS	164	D87
15	D34	65	VSS	115	VSS	165	D81
16	D37	66	VSS	116	VSS	166	D86
17	VCC	67	D56	117	CBW8	167	VSS
18	VCC	68	D63	118	CBW15	168	VSS
19	D35	69	D57	119	VCC	169	D82
20	D36	70	D62	120	VCC	170	D85
21	D8	71	D58	121	CBW9	171	D83
22	D15	72	D61	122	CBW14	172	D84
23	D9	73	D59	123	CBW10	173	D112
24	D14	74	D60	124	CBW13	174	D119
25	D10	75	CBW0	125	CBW11	175	D113
26	D13	76	CBW7	126	CBW12	176	D118
27	D11	77	CBW1	127	D64	177	D114
28	D12	78	CBW6	128	D71	178	D117
29	D40	79	CBW2	129	D65	179	D115
30	D47	80	CBW5	130	D70	180	D116
31	D41	81	VCC	131	D66	181	D88
32	D46	82	VCC	132	D69	182	D95
33	VSS	83	CBW3	133	D67	183	VCC
34	VSS	84	CBW4	134	D68	184	VCC
35	D42	85	CAS0	135	VSS	185	D89
36	D45	86	CAS1	136	VSS	186	D94
37	D43	87	RAS0	137	D96	187	D90
38	D44	88	NC	138	D103	188	D93
39	D16	89	NC	139	D97	189	D91
40	D23	90	NC	140	D102	190	D92
41	D17	91	NC	141	D98	191	D120
42	D22	92	NC	142	D101	192	D127
43	D18	93	A0	143	D99	193	D121
44	D21	94	A1	144	D100	194	D126
45	D19	95	A2	145	D72	195	D122
46	D20	96	A3	146	D79	196	D125
47	D48	97	A4	147	D73	197	D123
48	D55	98	A5	148	D78	198	D124
49	VCC	99	VSS	149	D74	199	VSS
50	VCC	100	VSS	150	D77	200	VSS

FUNCTION

The MH1M144CXTJ provide, in addition to normal read, write operation, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh.The input conditions for each are shown in Table 1.

Table 1. Input conditions for each mode

Operation	Inputs					Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	APD	APD	APD	OPN	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	NAC	DNC	DNC	OPN	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : Invalid,APD : applied, OPN : open

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	-1 ~ 7	V
VI	Input voltage		-1 ~ 7	V
V0	Output voltage		-1 ~ 7	V
I0	Output current		50	mA
Pd	Power dissipation	Ta=25°C	21.6	W
Topr	Operating temperature		0 ~ 70	°C
Tstg	Storage temperature		-40 ~ 100	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0 ~ 70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	4.75	5	5.25	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, I/O pins	2.4		5.5	V
V_{IH}	High-level input voltage, non I/O pins	2.0		5.5	V
V_{IL}	Low-level input voltage, I/O pins	-1.0		0.8	V
V_{IL}	Low-level input voltage, non I/O pins	-0.5		0.8	V

Note 1 : All voltage values are with respect to Vss

ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70°C , Vcc=5.0V ± 5%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	High-level output voltage	I_{OH}=-5.0mA	2.4		Vcc	V
V_{OL}	Low-level output voltage	I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current	Q floating 0V ≤ V_{OUT} ≤ 5.5V	-10		10	µA
I_I	Input current	0V ≤ VIN ≤ 6.5V, Other inputs pins=0V	-10		10	µA
Icc(note 3)	Operating Current Average	13%Fase Page mode and 87% CBR Refresh mode			3.3	A

Note 2: Current flowing into an IC is positive, out is negative.
3: tRC = tRC(min.) Icc is depend on cycle rate.

CAPACITANCE (Ta=0 ~ 70 °C, Vcc=5.0V ± 5%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
CI1	Input capacitance, address inputs	V_I=Vss			17	pF
CI2	Input capacitance, clocks inputs	f=1MHz			15	pF
CI3	Input/Output capacitance	Vi=25mVrms			17	pF

AC CHARACTERISTICS

(Ta=0 ~70 °C, Vcc=5.0V ± 5%, Vss=0V, unless otherwise noted , see notes 4,5,6)

Symbol	Parameter	Min	Max	Unit	Notes
t_{RC}	Random Read or Write Cycle Time	110		ns	
t_{PC}	Fast Page Mode Cycle Time	40		ns	
t_{RAC}	Access time from /RAS		65	ns	7
t_{CAC}	Access time from /CAS		20	ns	7
t_{AA}	Access Time from Column Address		35	ns	7
t_{CPA}	Access time from /CAS precharge		40	ns	
t_{CLZ}	CAS to Output in Low Z	5		ns	
t_{OFF}	Output Buffer Turn-Off Delay time	1	20	ns	10
t_T	Transition Time(Rise And Fall)	3	12	ns	4
t_{RP}	/RAS Precharge Time	40		ns	
t_{RAS}	/RAS Pulse Width	60	10K	ns	
t_{RSH}	/RAS Hold Time	18		ns	
t_{CSH}	/CAS Hold Time	60		ns	
t_{CAS}	/CAS Pulse Width	20	10K	ns	
t_{RCD}	/RAS to /CAS Delay Time	20	43	ns	8
t_{RAD}	/RAS to Column Address Delay Time	15	30	ns	9
t_{CRP}	/CAS to /RAS Precharge Time	10		ns	11
t_{CP}	/CAS Precharge Time	10		ns	
t_{ASR}	Row Address Setup Time	0		ns	
t_{RAH}	Row Address Hold Time	10		ns	
t_{ASC}	Column Address Setup Time	0		ns	
t_{CAH}	Column Address Hold Time	15		ns	
t_{AR}	Column Address Hold Time Ref to /RAS	50		ns	
t_{RAL}	Column Address Lead Time Ref to /RAS	30		ns	
t_{CAL}	Column Address Lead Time Ref to /CAS	30		ns	
t_{RCS}	Read Command Setup Time	0		ns	
t_{RCH}	Read Command Hold Time Ref to /CAS	0		ns	12
t_{RRH}	Read Command Hold Time Ref to /RAS	10		ns	12
t_{WCS}	Write Command Setup Time	0		ns	14
t_{WCH}	Write Command Hold Time	15		ns	
t_{WCR}	Write Command Hold Time Ref to /RAS	45		ns	
t_{WP}	Write Commnad Pulse Width	15		ns	
t_{RWL}	Write Command to /RAS Lead Time	15		ns	
t_{CWL}	Write Command to /CAS Lead Time	15		ns	
t_{DS}	Data Setup Time	0		ns	13
t_{DH}	Data Hold Time	20		ns	13
t_{DHR}	Data Hold Time Ref to /RAS	45		ns	
t_{REF}	Refresh Period		16.4	ms	15
t_{CSR}	/CAS Setup Time(CBR)	10		ns	
t_{CHR}	/CAS Hold Time(CBR)	20		ns	
t_{RPC}	/RAS to /CAS Precharge Time	10		ns	
t_{CPN}	/CAS Precharge Time(Non Page Mode)	10		ns	
t_{WRP}	/WE Setup(CBR Refresh)	10		ns	
t_{WRH}	/WE Hold(CBR Refresh)	10		ns	
t_{RHP}	Write to RAS Hold Time	35		ns	

Note 4: VIH Min and VIL Max are reference levels for measuring timing of inputs signals.AIso,transition times are measured between VIH and VIL

5: An initial pause of 500us is required after power-up followed by 8 CBR cycles before proper device operation is achived.

6: AC measurements assume tT = 5ns.

7: Load = 2TTL loads and 100pF.

8: Operation within the tRCD Max limit insures that tRAC Max can be met.tRCD Max is specified as a reference point only.If tRCD is greater than the specified tRCD Max limit,then access time is controlled by tCAC.

9: Operation within the tRAD Max limit insures that tRAC Max can be met.tRAD Max is specified as a reference point only.If tRAD is greater than the specified tRAD Max limit,then access time is controlled by tAA.

10: tOFF Max defines the time at which the output achieves the open circuit conditon and is not referenced to VOH or VOL.

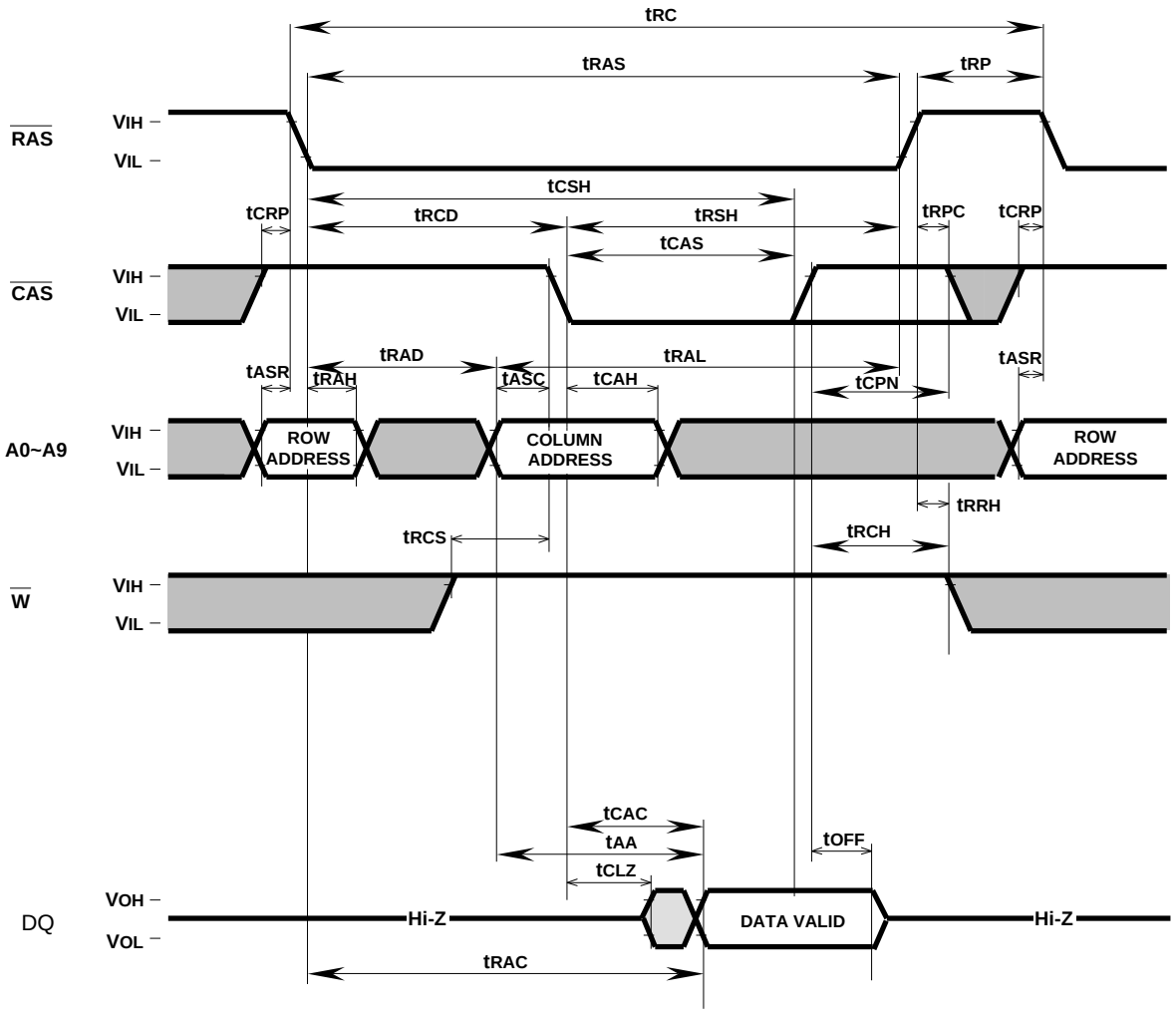
11: The tCRP requirement should be applicable for /RAS-/CAS cycles preceeded by any cycle.

12: Either tRRH or tRCH must be satisfied for a read cycle.

13: These parameters are referenced to the falling edge of /CAS for early write cycles.

Note 14 : If tWCS ≥ tWCS Min,the cycle is an early write cycle and dataout pin will remain open circuit(high impedance).
15 : 1024 refresh cycle for 16M.

Timing Diagrams (Note 16)
Read Cycle

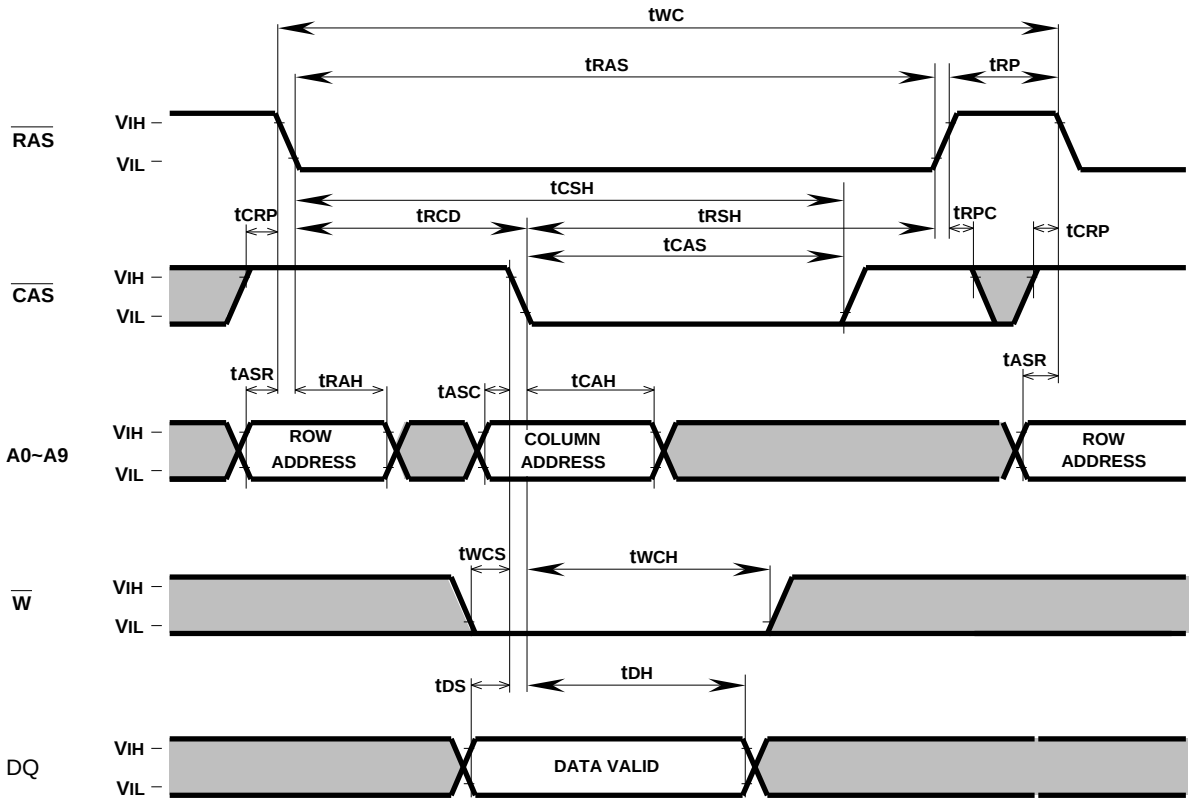


Note 16

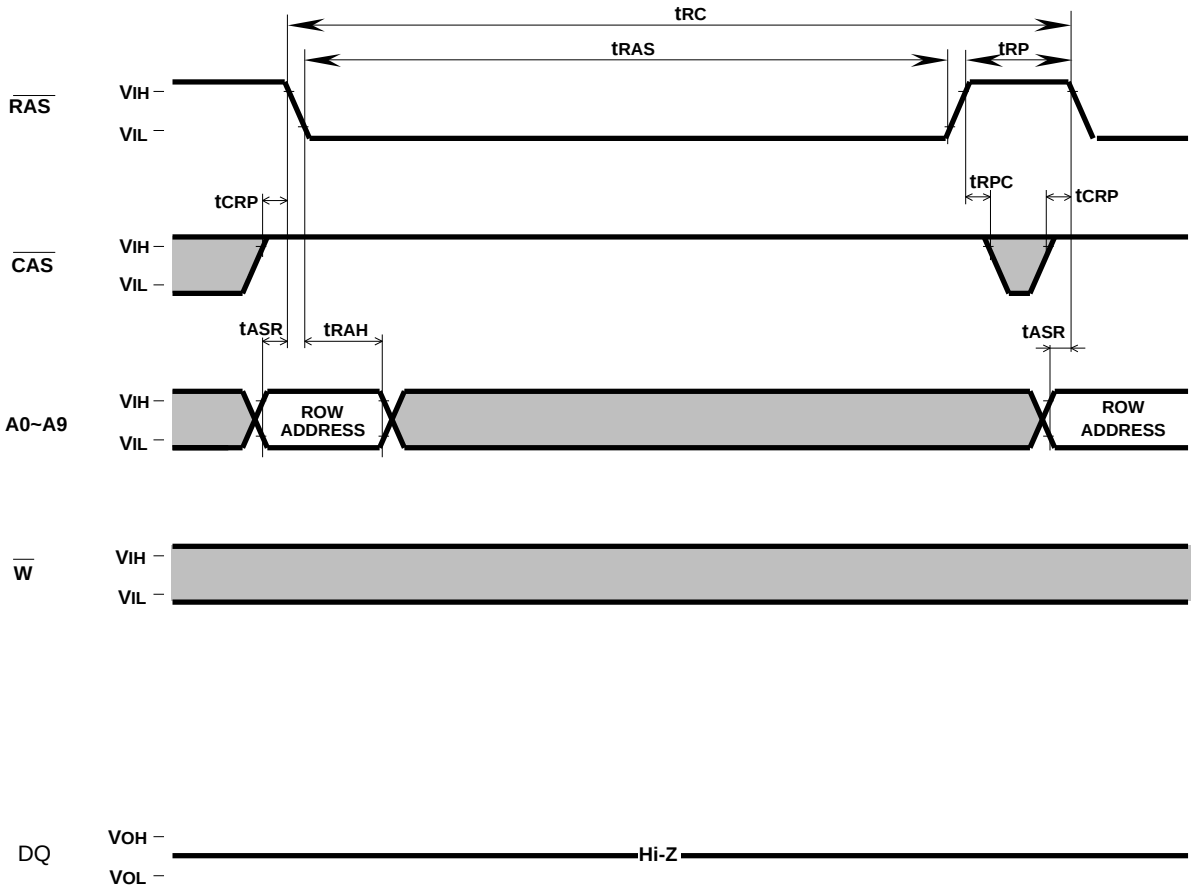
Indicates the don't care input.
VIH(min)≤VIN≤VIH(max) or VIL(min)≤VIN≤VIL(max)

Indicates the invalid output.

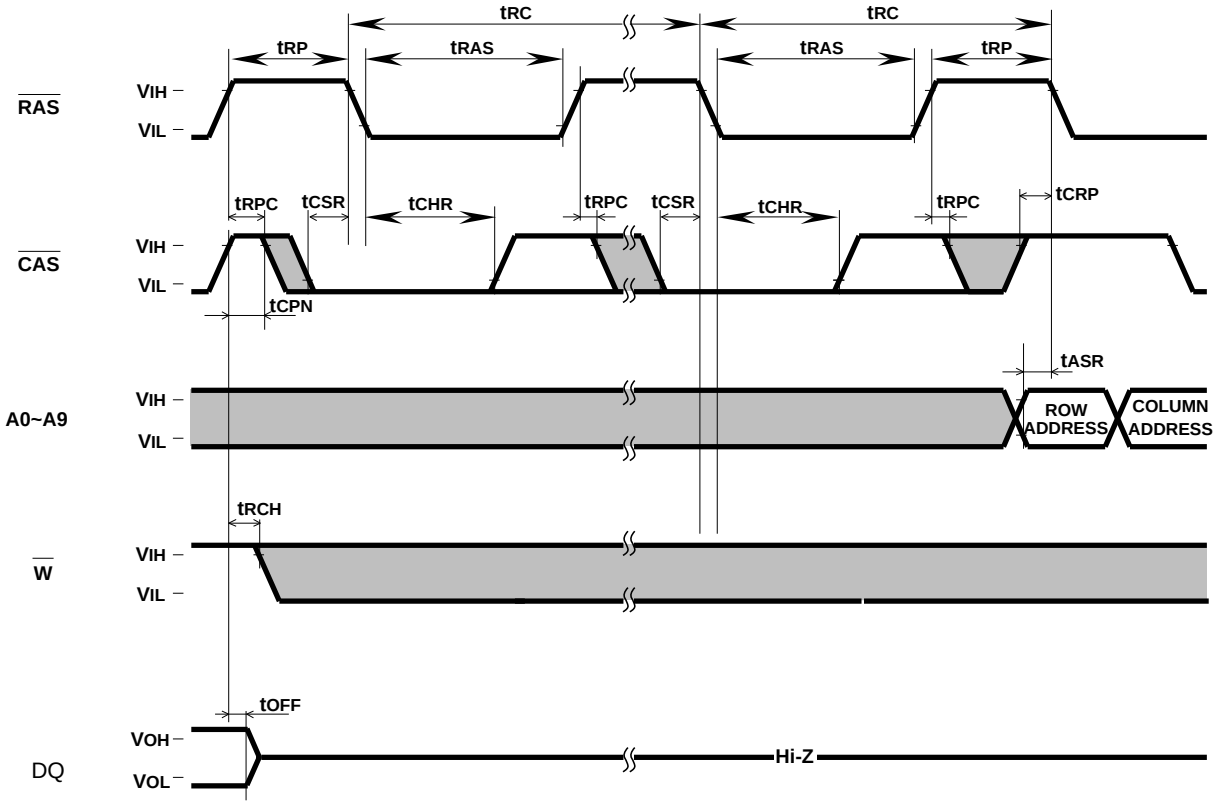
Write Cycle (Early write)



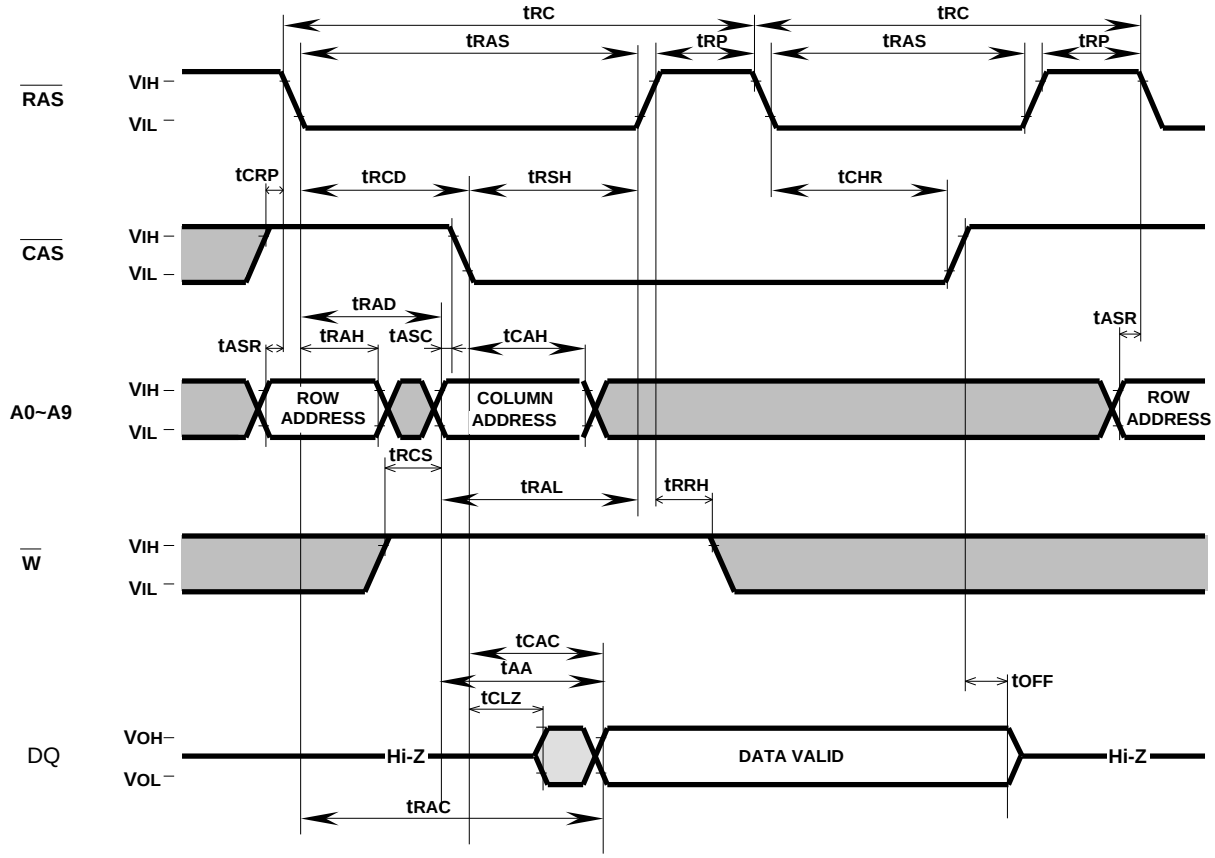
$\overline{\text{RAS}}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

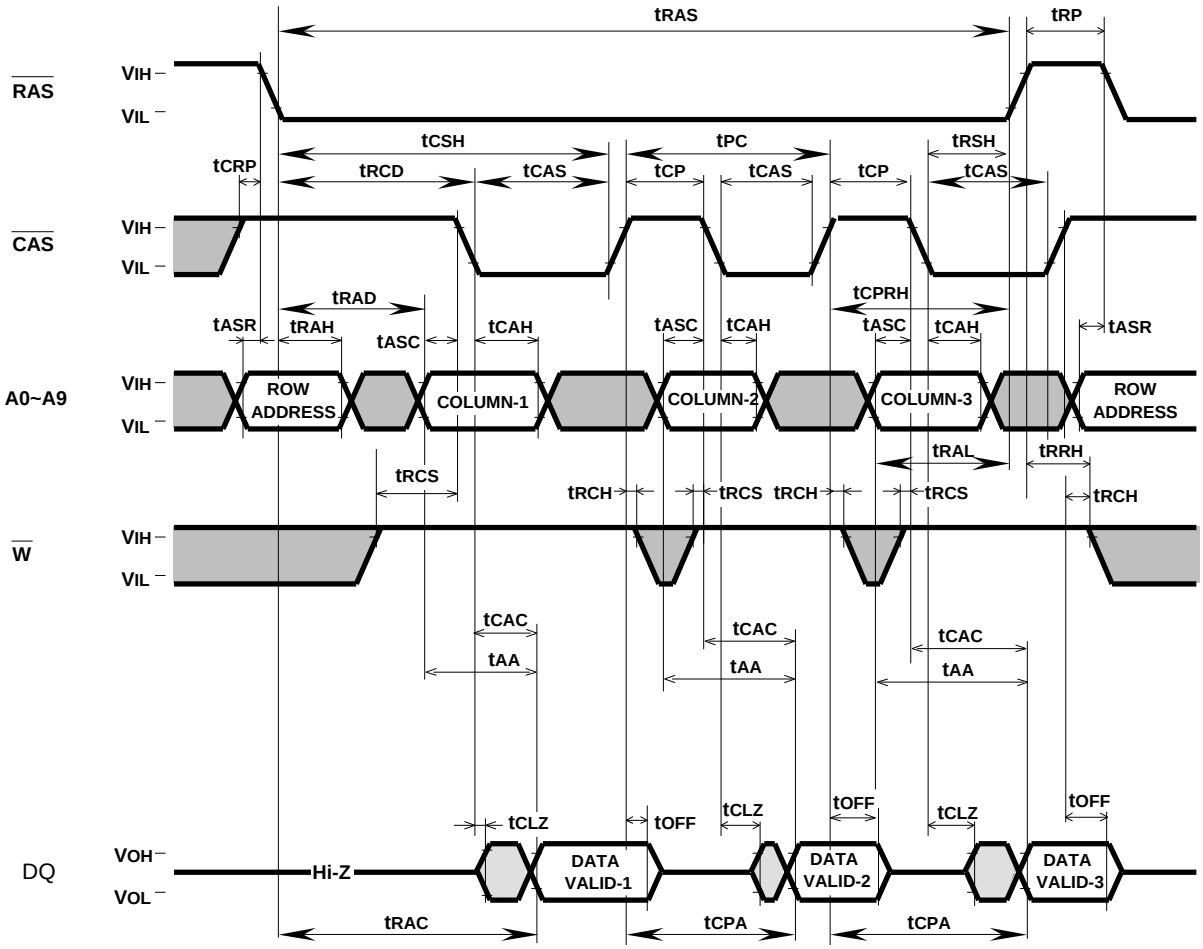


Hidden Refresh Cycle (Read) (Note 17)



Note 17: Early write is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

Fast Page Mode Read Cycle



Fast Page Mode Write Cycle (Early Write)