Preliminary

OKI Semiconductor

MSM7564-01

A Single Chip 14.4 kbps Data & Fax Modem

GENERAL DESCRIPTION

The MSM7564-01 is a highly integrated single-chip modem IC which provides the functions needed to construct 14.4 kbps full-duplex and half-duplex modems. This device is compliant with the following data communication formats : ITU-T Recommendation V.32bis, V.32, V.22bis, V.21 and Bell standard Bell 212A and Bell103 modes, and facsimile communication formats : ITU-T Recommendation V.17, V29, V.27ter, V.21 ch2.

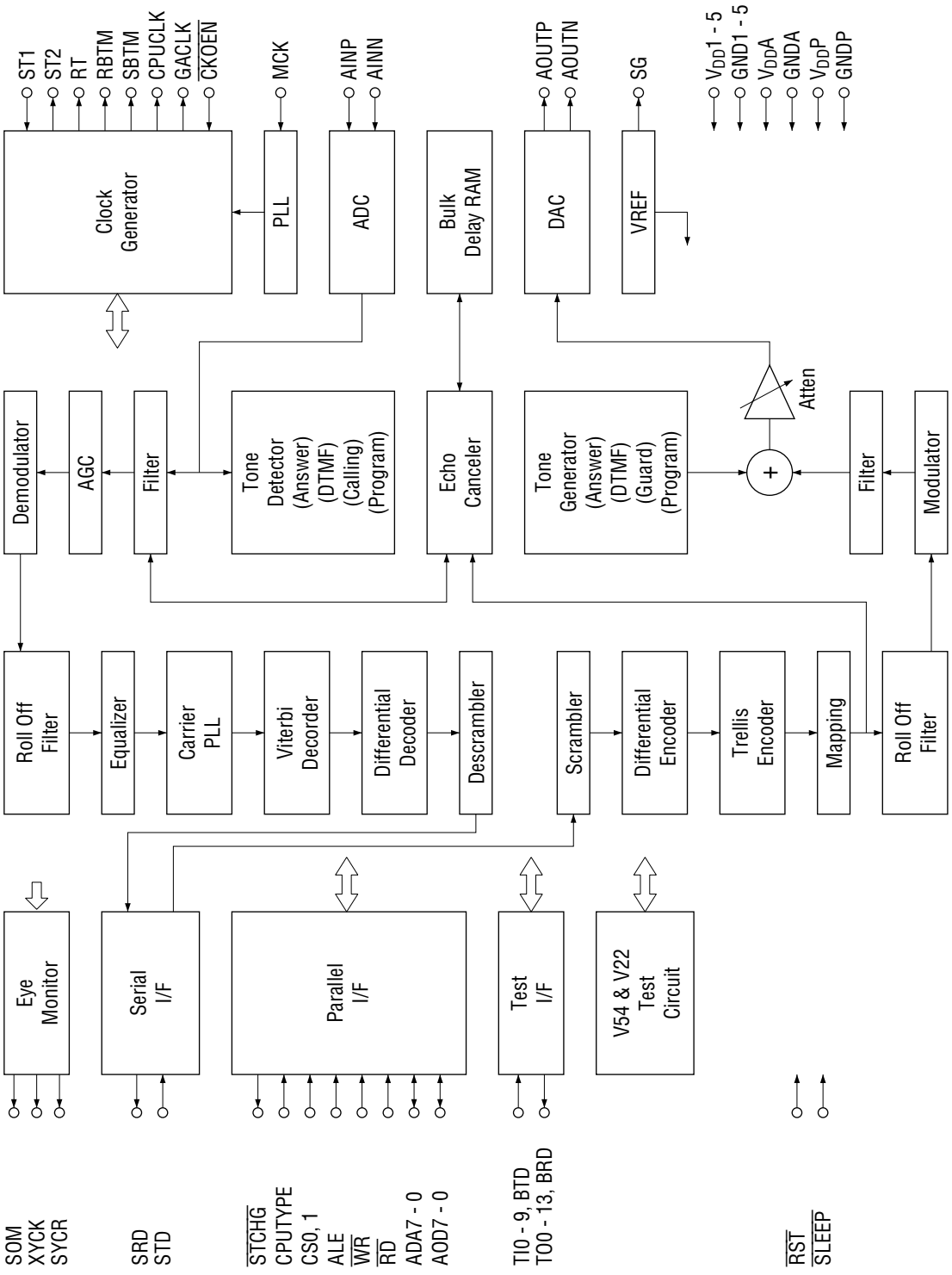
This device contains fundamental functions : high speed DSP, analog front end, and digital logic circuit. It also provides additional circuits such as test functions, synchronous-asynchronous conversion circuit, DTMF generator/detector, programmable tone generator/detector, voice output function and sleep mode. The MSM7564-01 is designed to provide a microprocessor peripheral to interface with popular single-chip microprocessors for the control of modem functions through its 8-bit multiplexed address/data bus.

FEATURES

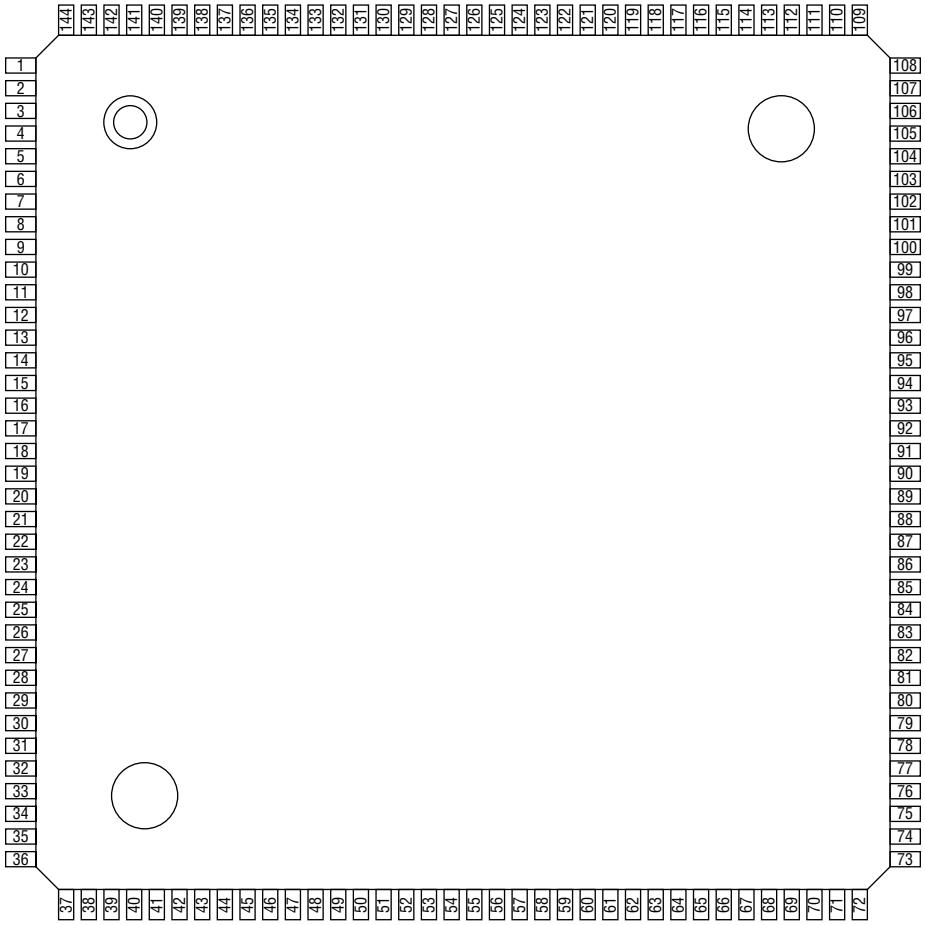
- Data mode : ITU-T Recommendation V.32bis, V.32, V.22bis, V.22, V.21
  Bell standard Bell 212A, Bell103
- Fax mode : ITU-T Recommendation V.17, V.29, V.27ter, V.21 ch2
- Synchronous/Asynchronous conversion
- Scrambler/Descrambler
- DTMF, answer tone, and guard tone generator
- Programmable transmit attenuation (15 dB, 1 dB steps)
- Call progress, answer tone, DTMF, and carrier detector
- Receiving signal quality monitor
- Independent adaptive line equalization for transmit and receive
- Carrier detection level selectable (4 steps)
- Echo canceler
- Jitter canceler
- Programmable tone generator/detector
- Voice output function
- Test mode : Local analog loop (internal/external)
  Remote digital loop
  511PN pattern generator for error test
  1:1 pattern generator for error test
  Error counter
- Sleep mode
- Single +5 V DC supply
- CMOS technology for low power consumption
  Operation mode : 500 mW Typ. @ +5 V
  Sleep mode : < 10 mW @ +5 V
- Package options:

144-pin plastic TQFP	(TQFP144-P-2020-K)	(Product name : MSM7564-01GS-K)
84-pin plastic QFJ	(QFJ84-P-S115)	(Product name : MSM7564-01JS)

BLOCK DIAGRAM



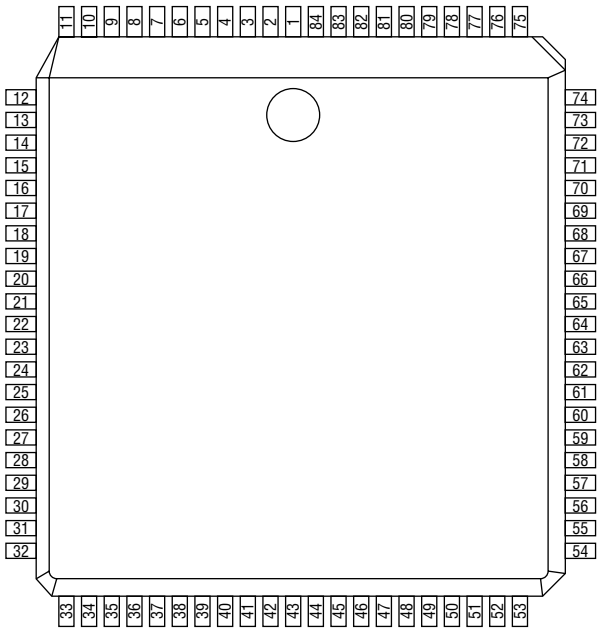
PIN CONFIGURATION (TOP VIEW)



144-Pin Plastic TQFP

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	AINN	37	NC	73	TO1	109	NC
2	NC	38	NC	74	ADA6	110	TO10
3	AINP	39	TI4	75	ADA4	111	TO6
4	AOUTN	40	TI3	76	ADA3	112	NC
5	NC	41	NC	77	$V_{DD}3$	113	TO13
6	NC	42	TI5	78	NC	114	TO12
7	AOUTP	43	NC	79	ADA2	115	NC
8	$V_{DD}A$	44	TO4	80	NC	116	TO11
9	GND1	45	NC	81	ADA0	117	TO7
10	NC	46	CPUTYPE	82	NC	118	NC
11	TI2	47	GND3	83	AOD7	119	TO9
12	NC	48	NC	84	NC	120	NC
13	STD	49	BRD	85	AOD6	121	TO8
14	NC	50	ALE	86	NC	122	NC
15	$V_{DD}1$	51	NC	87	NC	123	TI6
16	NC	52	SOM	88	AOD5	124	TI7
17	ST1	53	NC	89	NC	125	NC
18	NC	54	$V_{DD}2$	90	GND4	126	$V_{DD}5$
19	$\overline{WR}$	55	SYCR	91	NC	127	TI1
20	NC	56	NC	92	AOD4	128	NC
21	BTD	57	ST2	93	NC	129	TI0
22	NC	58	NC	94	AOD3	130	NC
23	$\overline{RD}$	59	XYCK	95	NC	131	TI9
24	NC	60	NC	96	AOD2	132	GND5
25	CS1	61	SRD	97	NC	133	$V_{DD}P$
26	GND2	62	$\overline{STCHG}$	98	NC	134	MCK
27	NC	63	NC	99	AOD1	135	NC
28	$\overline{RST}$	64	TO2	100	NC	136	NC
29	NC	65	NC	101	$V_{DD}4$	137	TO5
30	CS0	66	TO0	102	AOD0	138	GNDP
31	NC	67	TO3	103	ADA5	139	GNDA
32	$\overline{CKOEN}$	68	RT	104	NC	140	NC
33	NC	69	NC	105	NC	141	NC
34	SBTM	70	CPUCLK	106	ADA1	142	NC
35	$\overline{SLEEP}$	71	GACLK	107	ADA7	143	SG
36	RBTM	72	NC	108	TI8	144	NC

NC : No connect pin



84-Pin Plastic QFJ

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	GND4	22	$V_{DD}5$	43	$\overline{WR}$	64	SYCR
2	AOD4	23	TI1	44	BTD	65	ST2
3	AOD3	24	TI0	45	$\overline{RD}$	66	XYCK
4	AOD2	25	TI9	46	CS1	67	SRD
5	AOD1	26	GND5	47	GND2	68	$\overline{STCHG}$
6	$V_{DD}4$	27	$V_{DD}P$	48	$\overline{RST}$	69	TO2
7	AOD0	28	MCK	49	CS0	70	TO0
8	ADA5	29	TO5	50	$\overline{CKOEN}$	71	TO3
9	ADA1	30	GNDP	51	SBTM	72	RT
10	ADA7	31	GNDA	52	$\overline{SLEEP}$	73	CPUCLK
11	TI8	32	SG	53	RBTM	74	GACLK
12	TO10	33	AINN	54	TI4	75	TO1
13	TO6	34	AINP	55	TI3	76	ADA6
14	TO13	35	AOUTN	56	TI5	77	ADA4
15	TO12	36	AOUTP	57	TO4	78	ADA3
16	TO11	37	$V_{DD}A$	58	CPUTYPE	79	$V_{DD}3$
17	TO7	38	GND1	59	GND3	80	ADA2
18	TO9	39	TI2	60	BRD	81	ADA0
19	TO8	40	STD	61	ALE	82	AOD7
20	TI6	41	$V_{DD}1$	62	SOM	83	AOD6
21	TI7	42	ST1	63	$V_{DD}2$	84	AOD5

PIN DESCRIPTIONS

System and Clock

Symbol	Type	Description
MCK	I	Master Clock Input Frequency of 3.888 MHz ±100 ppm, with a duty ratio of between 45 and 55%.
$\overline{RST}$	I	Reset Input '0' : reset state, '1' : normal operation
$\overline{SLEEP}$	I	Sleep Input '0' : sleep state, '1' : normal operation
$\overline{CKOEN}$	I	Clock Output Enable '0' : CPUCLK and GACLK pins are enabled to output. (Internal PLL operates normally in sleep state.) '1' : CPUCLK and GACLK pins are disabled to output. (Internal PLL turns to be power down in sleep state.)
CPUCLK	O	CPU Clock Output CPUCLK outputs a 15.552 MHz clock for external CPU.
GACLK	O	Gate Array Clock Output GACLK outputs a 13.824 MHz clock for external gate array.

Modem Digital Interface

Symbol	Type	Description
ST1	I	External Transmit Clock Input An external transmit clock provided to input to ST1. The clock frequency of 300 to 14400 Hz is supplied by the local DTE.
ST2	O	Internal Transmit Clock Output ST2 outputs the transmitting data clock of between 300 and 14400 Hz selected by modem mode.
RT	O	Internal Receive Clock Output RT outputs the receiving data clock of between 300 and 14400 Hz selected by modem mode.
STD	I	Transmit Data Serial Input STD inputs the transmit serial data synchronized with either internal timing selected by modem mode or ST1 / ST2.
SRD	O	Received Data Serial Output SRD outputs the received serial data synchronized with either internal timing selected by modem mode or RT.

CPU Interfaces

Symbol	Type	Description
CPUTYPE	I	CPU Type Select CPUTYPE selects CPU bus type of ADA7 - 0 and AOD7 - 0. '1' : 80 mode (multiplexed address and data bus for Intel-compatible) '0' : 68 mode (separated address and data bus for Motorola-compatible)
$\overline{\text{STCHG}}$	O	Status Change Output When interface memory registers (0C, 0D, 1E, 1F) change, STCHG is set to "0". When the registers are read by external CPU, this pin is set to '1'.
CS0, 1	I	Chip Select Input 0 and 1 When CS0 and CS1 are set to '1', this chip is selected for microprocessor operation.
ALE	I	Address Latch Enable Input ALE allows the microprocessor to latch the address bus (ADA7 - 0) when CPUTYPE is 80 mode. Address bus is latched at the falling edge of ALE.
$\overline{\text{RD}}$	I	Read Enable $\overline{\text{RD}}$ is active LOW and is used to read from internal memory register via 8-bit address data input/output pins selected by CPUTYPE pin. CS0 and CS1 must be high.
$\overline{\text{WR}}$	I	Write Enable $\overline{\text{WR}}$ is active Low and is used to write the data at the rising edge via data input/output pins selected by CPUTYPE pin into internal memory registers. CS0 and CS1 must be high.
ADA7 - 0	I/O	8 bit Address and Data Bus 1 8 lines provide 2 modes of bus type which are selected by CPUTYPE pin. AD7 to 0 are controlled by ALE, $\overline{\text{RD}}$ and $\overline{\text{WR}}$. 80 mode : (I/O) address input and data input/output 68 mode : (I) address input
AOD7 - 0	I/O	8 bit Address and Data Bus 2 8 lines provide 2 modes of bus type which are selected by CPUTYPE pin. AD7 to 0 are controlled by ALE, $\overline{\text{RD}}$ and $\overline{\text{WR}}$. 80 mode : (O) address output (outputs latched address by ALE) 68 mode : (I/O) address input/output

Other Interfaces

Symbol	Type	Description
RBTM	O	Receive Baud Rate Timing Clock Output RBTM outputs receive baud rate timing clock of between 600 and 2400 Hz selected by modem mode.
SBTM	O	Transmit Baud Rate Timing Clock Output RBTM outputs transmit baud rate timing clock of between 600 and 2400 Hz selected by modem mode.
SOM	O	Serial Eye Pattern X/Y Output SOM outputs serial pattern containing two 16 bit words (X, Y references), synchronized with the falling edge of XYCK.
XYCK	O	Serial Eye Pattern Clock Output XYCK outputs a 1152 Hz clock for SOM timing.
SYCR	O	Serial Eye Pattern Timing Output SYCR outputs synchronous timing for SOM output. SYCR outputs two clocks of SOM clocks.

Test Interface

Symbol	Type	Description
TI0	I	TEST PIN. Connect to ground.
TI1	I	TEST PIN. Connect to ground.
TI2 - 4	I	TEST PIN. Connect to ground.
TI5, 6	I	TEST PIN. Connect to ground.
TI7	I	TEST PIN. Connect to ground.
TI8	I	TEST PIN. Connect to ground.
TI9	I	TEST PIN. Connect to V_{DD}.
BTD	I	TEST PIN. Connect to V_{DD}.
TO0	I/O	TEST PIN. Leave "OPEN".
TO1	I/O	TEST PIN. Leave "OPEN".
TO2	I/O	TEST PIN. Leave "OPEN".
TO3	I/O	TEST PIN. Connect to ground.
TO4	I/O	TEST PIN. Leave "OPEN".
TO5	O	TEST PIN. Leave "OPEN".
TO6 - 13	I/O	TEST PIN. Leave "OPEN".
BRD	O	TEST PIN. Leave "OPEN".

Analog Interface

Symbol	Type	Description
AINP	I	Analog Input (positive)
AINN	I	Analog Input (negative)
AOUTP	O	Analog Output (positive) AOUTP is in high impedance state when $\overline{\text{CKOEN}}$ is '1' state and in sleep mode.
AOUTN	O	Analog Output (negative) AOUTN is in high impedance state when $\overline{\text{CKOEN}}$ is in '1' state and in sleep mode.
SG	O	Signal Ground for Analog The SG level is about +2.4 V. Connect bypass capacitor between SG and GNDA when $\overline{\text{CKOEN}}$ is in '1' state and in sleep mode.

Power Supply

Symbol	Type	Description
V_{DD}1 - 5	I	Digital V_{DD}.
GND1 - 5	I	Digital Ground.
V_{DD}P	I	PLL V_{DD}.
GNDP	I	PLL Ground.
V_{DD}A	I	Analog V_{DD}.
GNDA	I	Analog Ground.

FUNCTIONAL DESCRIPTION

Modem Mode

MSM7564 conforms to ITU-T Recommendation and Bell standard as follows.

Modem Mode	Data Rate (bps)	Modulation	Carrier Frequency (Hz)	Baud Rate	Synchronous/ Asynchronous	Note
V.17	14400	TCM	1800	2400	sync	
V.17	12000	TCM	1800	2400	sync	
V.17	9600	TCM	1800	2400	sync	
V.17	7200	TCM	1800	2400	sync	
V.32bis	14400	TCM	1800	2400	sync/async	
V.32bis	12000	TCM	1800	2400	sync/async	
V.32bis	9600	TCM	1800	2400	sync/async	
V.32bis	7200	TCM	1800	2400	sync/async	
V.32	9600	QAM	1800	2400	sync/async	
V.32	4800	QAM	1800	2400	sync/async	
V.29	9600	QAM	1700	2400	sync	
V.29	7200	QAM	1700	2400	sync	
V.29	4800	PSK	1700	2400	sync	
V.27ter	4800	PSK	1800	1600	sync	Backward Channel ON/OFF
V.27ter	2400	PSK	1800	1200	sync	Backward Channel ON/OFF
V.22bis	2400	QAM	1200/2400	600	sync/async	
V.22	1200	PSK	1200/2400	600	sync/async	
Bell212A	1200	PSK	1200/2400	600	sync/async	
V.21	300	FSK	1080/1750	300	async	
V.21ch2	300	FSK	1080/1750	300	sync	
Bell103	300	FSK	1170/2125	300	async	

Serial Interface

MSM7564 provides a one channel serial interface, including synchronous-asynchronous and asynchronous-synchronous converters. Select synchronous or asynchronous. In synchronous mode, the transmit data is synchronized with the clock provided from this chip or DTE. Serial transmit data to STD pin is latched with the rising edge of ST1 or ST2, and receive data on SRD is output synchronously with the falling edge of RT. This chip also includes a scrambler and descrambler.

Parallel Interface

MSM7564 contains twenty 8-bit registers (location from addresses 00H through 0FH and 1C through 1F), which are used to control this chip and to detect various signals. Connect this chip to either multiplexed address and data bus such as Intel-compatible (80 mode) or separate address and data bus such as Motorola-compatible (68 mode).

Transmit and Receive Level

Analog input and output are differential amplifiers, and are $\pm 1.2\ V_{O\text{-}P}$ peak signals. The level of the transmit line signal is –10 dBm. The modem can provide 15 dB programmable transmit attenuation with 1 dB steps controlled by the TXLEV bit in located 0BH register. Receive signal level is from –10 dBm to –43 dBm. Carrier detection level can be selected from 4 levels (–43, –33, –26, –16 dBm) by the CDLEV bit located in register 0BH. An amplitude equalizer in transmitter and receiver can be individually controlled by RAEQL and SAEQL bits in register 07H.

DTMF Tone, Answer Tone, and Guard Tone Generators

The modem can generate 16 types of DTMF tones using the PBANSEL bit located in register 05H. It also generates answer tone and guard tone.

Various Detection Circuits

The internal detection circuit monitors carrier, call progress tone, answer tone, DTMF tone, and other receive signals needed for each modem mode, and stores them in the corresponding bits of each of the following registers : 0C, 0D, 1C, and 1D. Classification of detected tones is controlled by DETMODE bit in register 08H. If the contents of registers 0C, 0D, 1C, and 1D change, the interruption signal (STCHG) for controlling microprocessor is generated.

Programmable Tone Generator and Detector

The transmission of programmable tone 1 and tone 2 is available and is controlled by PTONE1 and PTONE2 bits in 05H register. To use this function, the initial download of frequency and gain is needed. This modem can output 16 kinds of frequency selected by PBANSEL bit of register 05H (composition of two tones is also available.). PTONE1 and PTONE2 are the same frequency and only the gain is variable. Each bit of D7, D6, D3, D2, D1, and D0 in register 0C can be used for programmable tone detecting by rewriting a coefficient of internal filter at the initial download.

Received Signal Quality Monitor

The modem indicates a state of received signal quality using the SQD bit of register 0D. If this bit changes, an interrupt signal (STCHG) for controlling the microprocessor is generated. Furthermore, it can read the bit error rate and receive level (stored in internal RAM) required for MNP class 10.

Echo Canceler

The modem has internal RAM for bulk delay and can cope with delays of up to 1.2 s for far-end echo.

Voice Output Function

The voice output is enabled by setting MODEMSET bit of register 06 to voice mode. In this case, voice data of 7.2 kHz sampling of 8 bits must be written in 00, 01, and 02 registers with the rising edge of RBTM (2.4 kHz).

Test Mode

The modem performs the internal local analog loop testing by the LALTST bit of register 07H. It also performs external local analog loop testing by the LALTST bit of register 07H and by connecting transmit analog output and receive analog input. Remote digital loop is available by the LOOP2 bit of register 1EH.
It can output a 511PN pattern and 1 to 1 pattern for error test controlling PN511 and ERR11 bits of register 1EH.
Error counts can be read controlling ERRCNT bit of register 1DH.

Sleep Mode

The modem supports a sleep function by controlling $\overline{\text{SLEEP}}$ bit of register 04H and $\overline{\text{SLEEP}}$ pin. It provides two modes of sleep1 (clock generator is inactive at $\overline{\text{CKOEN}}$ = '1') and sleep2 (clock generator is active at $\overline{\text{CKOEN}}$ = '0') controlled by $\overline{\text{CKOEN}}$ pin. Cancellation of sleep mode is controlled by SOFTRST bit of register 04H and $\overline{\text{RST}}$ pin.

Control register

The modem contains twenty 8-bit registers for control and signal detection monitoring. These registers are assigned by the address (ADA7-0 or AOD7-0) as shown in the following table.

• Table of control register

REG (H)	D7	D6	D5	D4	D3	D2	D1	D0
1F W	SB1DEN	RDZ	SDZ	SDA	WSIZE		EXTEND	ASYN
1E W	TXCLK		ERR11	PN511	SB11	PN1	PN0	LOOP2
1D R	DON'T CARE	BRKDET	ERRCNT			SB11DET	PN1DET	PN0DET
1C R	DON'T CARE	DON'T CARE	DON'T CARE	DON'T CARE	USB124D	USB112D	SB124D	SB112D
0F W	write "0"							
0E R	DON'T CARE						DCD	CTS
VOICE	PBTONE NO							
0D R	DON'T CARE	DSPRST	PBDET	TRN	FCD	SQD	EED	RATED
0C R V32	1650	1300	CPGDET	ANSDET	2250USB1	3000 AC	1800 AA	600 AC
V22ORG	2225	1100			2250USB1	2700 S1	2400 S1	2100 S1
V22ANS	980	1100			1270USB1	1500 S1	1200 S1	900 S1
V21ORG	1650	1300			2250USB1	3000 AC	1800 AA	600 AC
V21ANS	980	1300			2250USB1	3000 AC	1800 AA	600 AC
Bell103ORG	2225	1300			2250USB1	3000 AC	1800 AA	600 AC
Bell103ANS	1270	1300			2250USB1	3000 AC	1800 AA	600 AC
V17, V21ch2	1650	1300			1750	3000 AC	1800 AA	600 AC
V29	1650	1300			1750	2900	1700	500
V27	1650	1300			1750	2600	1800	1000
VOICE	1100	1300			2250USB1	3000 AC	1800 AA	600 AC
0B W	AGCRST	AGCH	TXLEV				CDLEV	
0A W	ILDCNT	DSPST	write "0"	write "0"	STRN	BRTS	EPT	RTS
09 W V32	EB1	RATES	TRN	ECTRN	SS	XCHG	AACC	ACCA
V22	write "0"	write "0"	write "0"	SB124	SB112	USB124	USB112	S1
VOICE	write "0"	VSMODE			write "0"			
08 W	DETMODE		AQID	TIMC	TANI	JHOLD	EHOLD	TAPH
07 W	LALTST		GTS	GTE	RAEQL	SAEQL	ORGANS	V32DATA
VOICE	write "0"			VEN	RAEQL	SAEQL	ORGANS	write "0"
06 W	MODEMSET							
05 W	PBANSEL				SFIL	PBANS	PTONE2	PTONE1
04 W	write "0"	NEGO	STUP	AUTO	EQLST	SLEEP	SOFTRST	RAMRDWR

• Table of control register (Continued)

REG (H)	D7	D6	D5	D4	D3	D2	D1	D0
03 R/W	DRAMDH (F-8)							
VOICE	write "0"			VSEN	write "0"	write "0"	VIOF	write "0"
02 R/W	DRAMDL (7-0)							
VOICE	VDATA3RD							
01 R/W	DRAMAH (F-8)							
VOICE	VDATA2ND							
00 R/W	DRAMAL(7-0)							
VOICE	VDATA1ST							

Notes: 1. W:Write Only, R: Read Only, R/W: Read/Write.
2. Deal with the following modes due to MODEMSET bit of 06H register and ORGANS bit of 07H register.
V32: V.32bis & V.32, V22: V.22bis & V.22, V21: V.21, V17: V.17, V21ch2: V.21ch2, V29: V.29, V23: V.23, V27: V.27ter, VOICE: Voice mode, ORG: Originate, ANS: Answer

Control register functional summary

REG (H)	BIT	SYMBOL	FUNCTION
00 R/W	7-0	DRAMAL (7-0)	Specify low-order 8-bit (bit7 - 0) of the address to access an internal RAM.
01 R/W	7-0	DRAMAH (F-8)	Specify high-order 8 bits (bit15 - 8) of the address to access an internal RAM.
02 R/W	7-0	DRAMDL (7-0)	Store low-order 8 bits of the data to access an internal RAM.
03 R/W	7-0	DRAMDH (F-8)	Store high-order 8 bits of the data to access an internal RAM.
00 R/W (VOICE)	7-0	VDATA1ST	Voice output 1st data
01R/W (VOICE)	7-0	VDATA2ND	Voice output 2nd data
02 R/W (VOICE)	7-0	VDATA3RD	Voice output 3rd data
03 R/W	1	VIOF	Input/output flag of voice data output
(VOICE)	4	VSEN	Enables voice data output.
04 W	0	RAMRDWR	When internal RAM is accessed, selects read or write.
	1	SOFTRST	Soft reset
	2	SLEEP	Sleep
	3	EQLST	Controls adaptive equalizer.
	4	AUTO	Specifies control method of adaptive equalizer.
	5	STUP	Start-up control
	6	NEGO	Auto negotiation control
05 W	0	PTONE1	Programmable tone control 1
	1	PTONE2	Programmable tone control 2
	2	PBANS	PB tone and answer tone control
	3	SFIL	Transmission filter control
	7-4	PBANSEL	Selects PB tone and answer tone.
06 W	7-0	MODEMSET	Modem mode setting.
07 W	0	V32DATA	Selects V.32bis and V.32 operating mode.
	1	ORGANS	Sets originate mode and answer mode.
	2	SAEQL	Sets adaptive equalization for transmit.
	3	RAEQL	Sets adaptive equalization for receive.
	4	GTE	Sets guard tone generator.
	5	GTS	Sets guard tone frequency.
	7-6	LALTST	Local analog loop back test control
07 W	1	ORGANS	Sets originate mode and answer mode.
(VOICE)	2	SAEQL	Sets transmit amplitude equalizer.
	3	RAEQL	Sets receive amplitude equalizer.
	4	VEN	Enables voice output.

Control register functional summary (Continued)

REG (H)	BIT	SYMBOL	FUNCTION
08 W	0	TAPH	Holds automatic equalizer, jitter canceler, and carrier PLL.
	1	EHOLD	Holds automatic equalizer and jitter canceler.
	2	JHOLD	Holds jitter canceler.
	3	TANI	Uses automatic equalizer of unit taps.
	4	TIMC	A pass through timing PLL
	5	AQID	Clears automatic equalizer, jitter canceler, and carrier PLL.
	7-6	DETMODE	Sets tone detection mode.
09 W (V22)	0	S1	Transmits S1 signal.
	1	USB112	Transmits unscrambled binary 1 at 1200 bps.
	2	USB124	Transmits unscrambled binary 1 at 2400 bps.
	3	SB112	Transmits scrambled binary 1 at 1200 bps.
	4	SB124	Transmits scrambled binary 1 at 2400 bps.
09 W (V32)	0	ACCA	Transmits signals AC and CA.
	1	AACC	Transmits signals AA and CC.
	2	XCHG	Selects signals AA and CC. Exchage command of AA/CC
	3	SS	Transmits signal S.
	4	ECTRN	Transmits echo canceler training signal.
	5	TRN	Transmits consecutive signals S, $\overline{S}$, and TRN.
	6	RATES	Transmits signals R1 to R3.
	7	EB1	Transmits consecutive signals E and B1
09 W (VOICE)	6-4	VSMODE	Controls coding method at voice output.
0A W	0	RTS	Request of transmission.
	1	EPT	Transmits echo protector tone.
	2	BRTS	Sets RTS of backward channel.
	3	STRN	Selects short or long training.
	6	DSPST	DSP start
	7	ILDCNT	Initial load control
0B W	1-0	CDLEV	Carrier Detect Threshold Level select.
	5-2	TXLEV	Set programmable attenuator for transmission.
	6	AGCH	AGC hold
	7	AGCRST	AGC reset
0C W (V32)	0	600 AC	Detects signal AC of 600 Hz.
	1	1800 AA	Detects signal AA of 1800 Hz.
	2	3000 AC	Detects signal AC of 3000 Hz.
	3	2250USB1	Detects unscrambled binary 1 at 2250 Hz.
	4	ANSDET	Detects answer tone.
	5	CPGDET	Detects call progress tone.
	6	1300	Detects signal of 1300 Hz.
	7	1650	Detects signal of 1650 Hz.

Control register functional summary (Continued)

REG (H)	BIT	SYMBOL	FUNCTION
0C W	0	2100 S1	Detects signal S1 of 2100 Hz.
(V22ORG)	1	2400 S1	Detects signal S1 of 2400 Hz.
	2	2700 S1	Detects signal S1 of 2700 Hz.
	3	2250USB1	Detects unscrambled binary 1 at 2250 Hz.
	4	ANSDET	Detects answer tone.
	5	CPGDET	Detects call progress tone.
	6	1100	Detects signal of 1100 Hz.
	7	2225	Detects signal of 2225 Hz.
0C W	0	900 S1	Detects signal S1 of 900 Hz.
(V22ANS)	1	1200 S1	Detects signal S1 of 1200 Hz.
	2	1500 S1	Detects signal S1 of 1500 Hz.
	3	1270USB1	Detects unscrambled binary 1 at 1270 Hz.
	4	ANSDET	Detects answer tone.
	5	CPGDET	Detects call progress tone.
	6	1100	Detects signal of 1100 Hz.
	7	980	Detects signal of 980 Hz.
0C W	0	600 AC	Detects signal AC of 600 Hz.
(V21ORG)	1	1800 AA	Detects signal AA of 1800 Hz.
	2	3000 AC	Detects signal AC of 3000 Hz.
	3	2250USB1	Detects unscrambled binary 1 at 2250 Hz.
	4	ANSDET	Detects answer tone.
	5	CPGDET	Detects call progress tone.
	6	1300	Detects signal of 1300 Hz.
	7	1650	Detects signal of 1650 Hz.
0C W	0	600 AC	Detects signal AC of 600 Hz.
(V21ANS)	1	1800 AA	Detects signal AA of 1800 Hz.
	2	3000 AC	Detects signal AC of 3000 Hz.
	3	2250USB1	Detects unscrambled binary 1 at 2250 Hz.
	4	ANSDET	Detects answer tone.
	5	CPGDET	Detects call progress tone.
	6	1300	Detects signal of 1300 Hz.
	7	980	Detects signal of 980 Hz.
0C W	0	600 AC	Detects signal AC of 600 Hz.
(Bell 103 ORG)	1	1800 AA	Detects signal AA of 1800 Hz.
	2	3000 AC	Detects signal AC of 3000 Hz.
	3	2250USB1	Detects unscrambled binary 1 at 2250 Hz.
	4	ANSDET	Detects answer tone.
	5	CPGDET	Detects call progress tone.
	6	1300	Detects signal of 1300 Hz.
	7	2225	Detects signal of 2225 Hz.

Control register functional summary (Continued)

REG (H)	BIT	SYMBOL	FUNCTION
0C W	0	600 AC	Detects signal AC of 600 Hz.
(Bell 103 ANS)	1	1800 AA	Detects signal AA of 1800 Hz.
	2	3000 AC	Detects signal AC of 3000 Hz.
	3	2250USB1	Detects unscrambled binary 1 at 2250 Hz.
	4	ANSDET	Detects answer tone.
	5	CPGDET	Detects call progress tone.
	6	1300	Detects signal of 1300 Hz.
	7	1270	Detects signal of 1270 Hz.
0C W	0	600 AC	Detects signal AC of 600 Hz.
(V17, V21ch2)	1	1800 AA	Detects signal AA of 1800 Hz.
	2	3000 AC	Detects signal AC of 3000 Hz.
	3	1750	Detects signal of 1750 Hz.
	4	ANSDET	Detects answer tone.
	5	CPGDET	Detects call progress tone.
	6	1300	Detects signal of 1300 Hz.
	7	1650	Detects signal of 1650 Hz.
0C R	0	500	Detects signal of 500 Hz.
(V29)	1	1700	Detects signal of 1750 Hz.
	2	2900	Detects signal of 2900 Hz.
	3	1750	Detects signal of 1750 Hz.
	4	ANSDET	Detects answer tone.
	5	CPGDET	Detects call progress tone.
	6	1300	Detects signal of 1300 Hz.
	7	1650	Detects signal of 1650 Hz.
0C R	0	1000	Detects signal of 1000 Hz.
(V27)	1	1800	Detects signal of 1800 Hz.
	2	2600	Detects signal of 2600 Hz.
	3	1750	Detects signal of 1750 Hz.
	4	ANSDET	Detects answer tone.
	5	CPGDET	Detects call progress tone.
	6	1300	Detects signal of 1300 Hz.
	7	1650	Detects signal of 1650 Hz.
0C W	0	600 AC	Detects signal AC of 600 Hz.
(VOICE)	1	1800 AA	Detects signal AA of 1800 Hz.
	2	3000 AC	Detects signal AC of 3000 Hz.
	3	2250USB1	Detects unscrambled binary 1 at 2250 Hz.
	4	ANSDET	Detects answer tone.
	5	CPGDET	Detects call progress tone.
	6	1300	Detects signal of 1300 Hz.
	7	1100	Detects signal of 1100 Hz.

Control register functional summary (Continued)

REG (H)	BIT	SYMBOL	FUNCTION
0D R	0	RATED	Detects rate signal.
	1	EED	Detects end signal.
	2	SQD	Indicates a state of received signal quality.
	3	FCD	Detects fast carrier.
	4	TRN	Indicates a state of training.
	5	PBDET	Detects PB tone.
	6	DSPRST	DSP reset
0E R	0	CTS	Ready for sending.
	1	DCD	Detects carrier
0E R (VOICE)	0	PBTONE NO	PB tone number
1C R	0	SB112D	Detects scrambled binary 1 at 1200 bps.
	1	SB124D	Detects scrambled binary 1 at 2400 bps.
	2	USB112D	Detects unscrambled binary 1 at 1200 bps.
	3	USB124D	Detects unscrambled binary 1 at 2400 bps.
1D R	0	PN0DET	Detects preparatory signal.
	1	PN1DET	Detects answer / termination signal.
	2	SB11DET	Detects SB11
	5-3	ERRCNT	Error Count
	6	BRKDET	Detects break signal.
1E W	0	LOOP2	Controls Loop2 test.
	1	PN0	Transmits preparatory signal.
	2	PN1	Transmits answer /termination signal.
	3	SB11	Transmits SB11
	4	PN511	Transmits signal 511PN for error test.
	5	ERR11	Transmits 1 to 1 signal for error test.
	7-6	TXCLK	Sets transmitter signal element timing.
1F W	0	ASYN	Selects synchronous or asynchronous.
	1	EXTEND	Sets extended asynchronous mode.
	3-2	WSIZE	Sets a character size for synchronous to asynchronous converter.
	4	SDA	Transmitted data clamped to A
	5	SDZ	Transmitted data clamped to Z
	6	RDZ	Received data clamped to Z
	7	SB1DEN	Controls detection of scrambled binary 1.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{DD}	–0.3 to V_{DD} + 0.3	V
Analog Input Voltage	V_{AIN}	–0.3 to V_{DD} + 0.3	V
Digital Input Voltage	V_{DIN}	–0.3 to V_{DD} + 0.3	V
Digital Output Voltage	V_{OUT}	–0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{STG}	–55 to + 150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	4.75	5.00	5.25	V
Operating Temperature	T_{op}	–20	—	70	°C

RECOMMENDED OPERATING CONDITIONS (ANALOG)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Impedance	R_{AI}	50	—	—	kΩ
Output Load Impedance	R_{AOL}	20	—	—	kΩ
Output Load Capacitance	C_{AOL}	—	—	100	pF
Analog Input Amplitude	V_{AIN}	—	—	V_{SG}	V_{PP}
SG Output Voltage	V_{SG}	2.35	2.40	2.45	V

ELECTRICAL CHARACTERISTICS

DC Characteristics

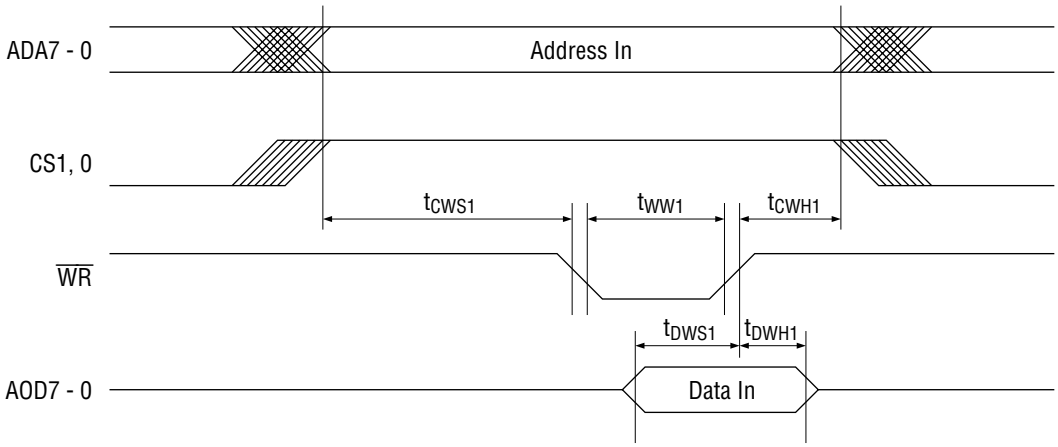
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = V_{DD}/0 V	–10	—	10	µA
Output Leakage Current	I_{LO}	V_{IN} = V_{DD}/0 V	–10	—	10	µA
High-level Input Voltage *1	V_{IH}	—	4.0	—	V_{DD} + 0.3	V
High-level Input Voltage *2	V_{IH}	—	2.4	—	V_{DD} + 0.3	V
Low-level Input Voltage *1	V_{IL}	—	–0.3	—	0.8	V
Low-level Input Voltage *2	V_{IL}	—	–0.3	—	0.8	V
High-level Output Voltage *1	V_{OH}	I_{OH} = –400 µA	4.2	—	—	V
High-level Output Voltage *2	V_{OH}	I_{OH} = –200 µA	4.2	—	—	V
Low-level Output Voltage *1	V_{OL}	I_{OL} = 3.2 mA	—	—	0.4	V
Low-level Output Voltage *2	V_{OL}	I_{OL} = 1.6 mA	—	—	0.4	V
Stand-by Current 1 (Sleep Mode)	I_{DDS1}	clock generator inactive state ($\overline{CKOEN}$ = 1)	—	—	2	mA
Stand-by Current 2 (Sleep Mode)	I_{DDS2}	clock generator active state ($\overline{CKOEN}$ = 0)	—	35	—	mA
Average Power Supply Current (Operating)	I_{DDO}	MCK = 3.888 MHz	—	100	—	mA

Notes: *1: Applied to RST, SLEEP pins.
*2: Applied to input pins except those of *1.
*3: Applied to ADA7 - 0 and AOD7 - 0 pins.
*4: Applied to output pins except those of *3.

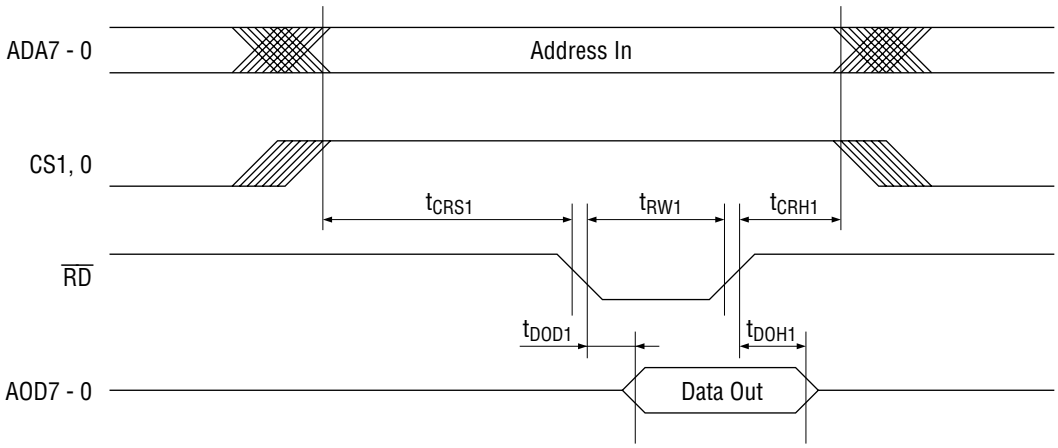
AC Characteristics (CPU Interface : 68 mode)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Address and Chip Select Setup Time (to $\overline{WR}$ Negative Edge)	t_{CWS1}	30	—	—	ns
Address and Chip Select Setup Time (to $\overline{WR}$ Positive Edge)	t_{CWH1}	15	—	—	ns
$\overline{WR}$ Pulse Width	t_{WW1}	45	—	—	ns
Data-in Setup Time	t_{DWS1}	30	—	—	ns
Data-in Hold Time	t_{DWH1}	15	—	—	ns
Address and Chip Select Setup Time (to $\overline{WR}$ Negative Edge)	t_{CRS1}	30	—	—	ns
Address and Chip Select Setup Time (to $\overline{RD}$ Positive Edge)	t_{CRH1}	15	—	—	ns
$\overline{RD}$ Pulse Width	t_{RW1}	45	—	—	ns
Data-out Delay Time (to $\overline{RD}$ Negative Edge)	t_{DOD1}	—	—	40	ns
Data-out Hold Time (to $\overline{RD}$ Positive Edge)	t_{DOH1}	0	—	—	ns

Write timing



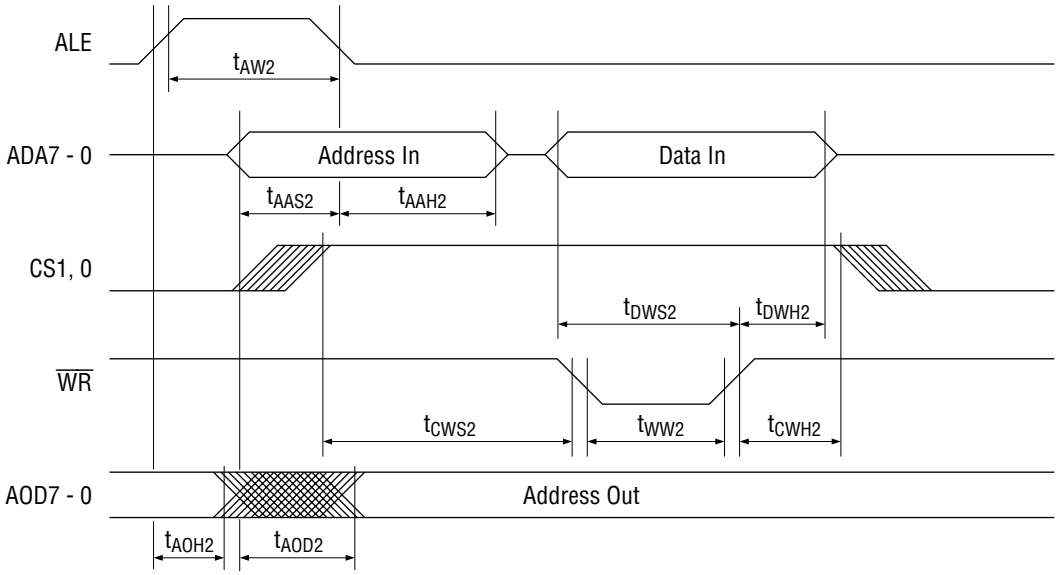
Read timing



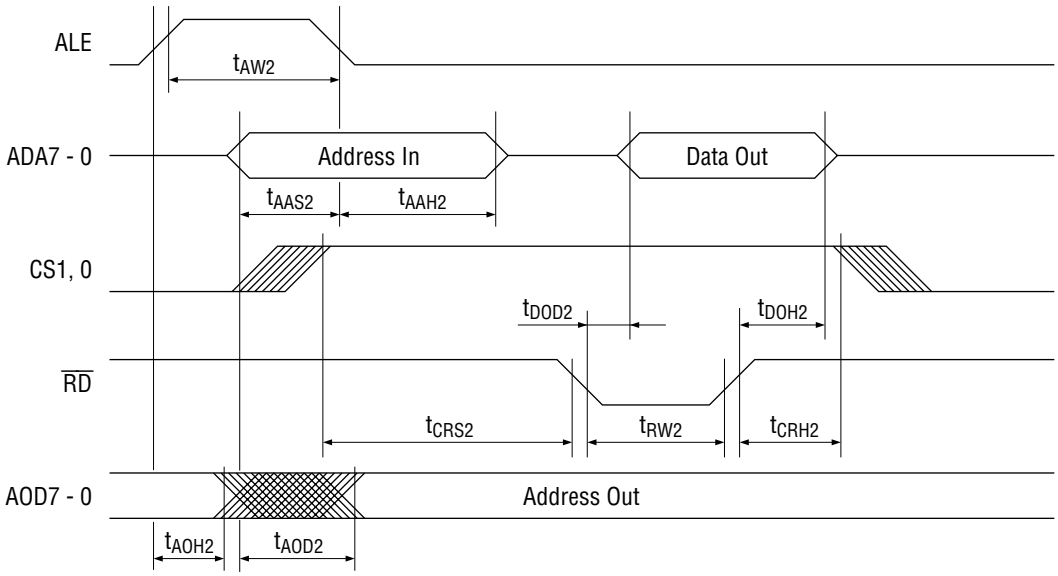
AC Characteristics (CPU Interface : 80 mode)

Parameter	Symbol	Min.	Typ.	Max.	Unit
ALE Pulse Width	t_{AW2}	30	—	—	ns
Address-in Setup Time	t_{AAS2}	30	—	—	ns
Address-in Hold Time	t_{AAH2}	15	—	—	ns
Chip Select Setup Time (to $\overline{WR}$ Negative Edge)	t_{CWS2}	30	—	—	ns
Chip Select Hold Time (to $\overline{WR}$ Positive Edge)	t_{CWH2}	15	—	—	ns
$\overline{WR}$ Pulse Width	t_{WW2}	45	—	—	ns
Data-in Setup Time	t_{DWS2}	30	—	—	ns
Data-in Hold Time	t_{DWH2}	15	—	—	ns
Address-out Hold Time	t_{AOH2}	0	—	—	ns
Address-out Delay Time	t_{AOD2}	—	—	40	ns
Chip Select Setup Time (to $\overline{RD}$ Negative Edge)	t_{CRS2}	30	—	—	ns
Chip Select Hold Time (to $\overline{RD}$ Positive Edge)	t_{CRH2}	15	—	—	ns
$\overline{RD}$ Pulse Width	t_{RW2}	45	—	—	ns
Data-out Delay Time (to $\overline{RD}$ Negative Edge)	t_{DOD2}	—	—	40	ns
Data-out Hold Time (to $\overline{RD}$ Positive Edge)	t_{DOH2}	0	—	—	ns

Write timing



Read timing



Analog Transmit Characteristics

Parameter		Symbol	Min.	Typ.	Max.	Unit	Note
Transmit Carrier	Output level (at TXLEV = 00)	TSFL	–11.5	–10	–8.5	dBm	
	Transmit signal to noise ratio	TSSN	—	65	—	dB	–10 dBm output
DTMF Tone	Frequency tolerance	TSDF	F – 10	F	F + 10	Hz	F = 1209, 1336, 1477, 1633, 697, 770, 852, 941 Hz
	Transmit level (at TXLEV = 00)	TSDLH	–7	–5.5	–4	dBm	High channel
		TSDLL	–8.5	–7	–5.5	dBm	Low channel
Answer Tone	Frequency tolerance	TSAF	F – 10	F	F + 10	Hz	F = 2100, 2225 Hz
	Transmit level (at TXLEV = 00)	TSAL	–11.5	–10	–8.5	dBm	

Analog Receive Characteristics

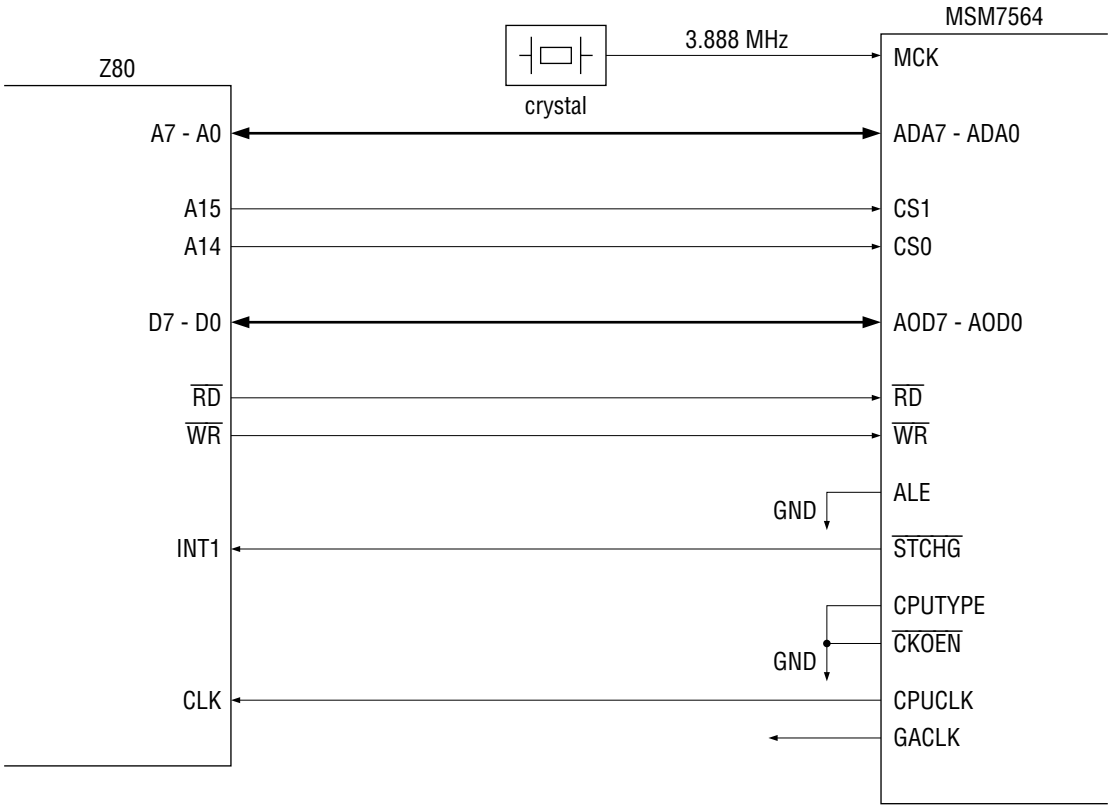
Parameter		Symbol	Min.	Typ.	Max.	Unit	Note
Receive Carrier	Input level	TRFL	–43	—	–10	dBm	
	Receive signal to noise ratio	TRSN	—	45	—	dB	–40 dBm input
Carrier Detector	Detect level	CDDL	–48	—	–43	dBm	
	Delay time	t_{CDD}	—	25	—	ms	
	Hold time	t_{CDH}	—	15	—	ms	
Answer Tone	Detect level	ATDL	–43	—	—	dBm	2100 Hz / 2225 Hz
	Delay time	t_{ATD}	—	25	—	ms	
	Hold time	t_{ATH}	—	25	—	ms	
Call Progress Tone	Detect level	CTDL	–43	—	—	dBm	350 to 620 Hz band
	Delay time	t_{CTD}	—	50	—	ms	
Other Tone	Detect level	OTDL	–43	—	—	dBm	ex. DTMF tone

Note: A unit (dBm) to signal power level is 600 Ω termination. 0 dBm is equal to 0.775 Vrms.

APPLICATION CIRCUITS

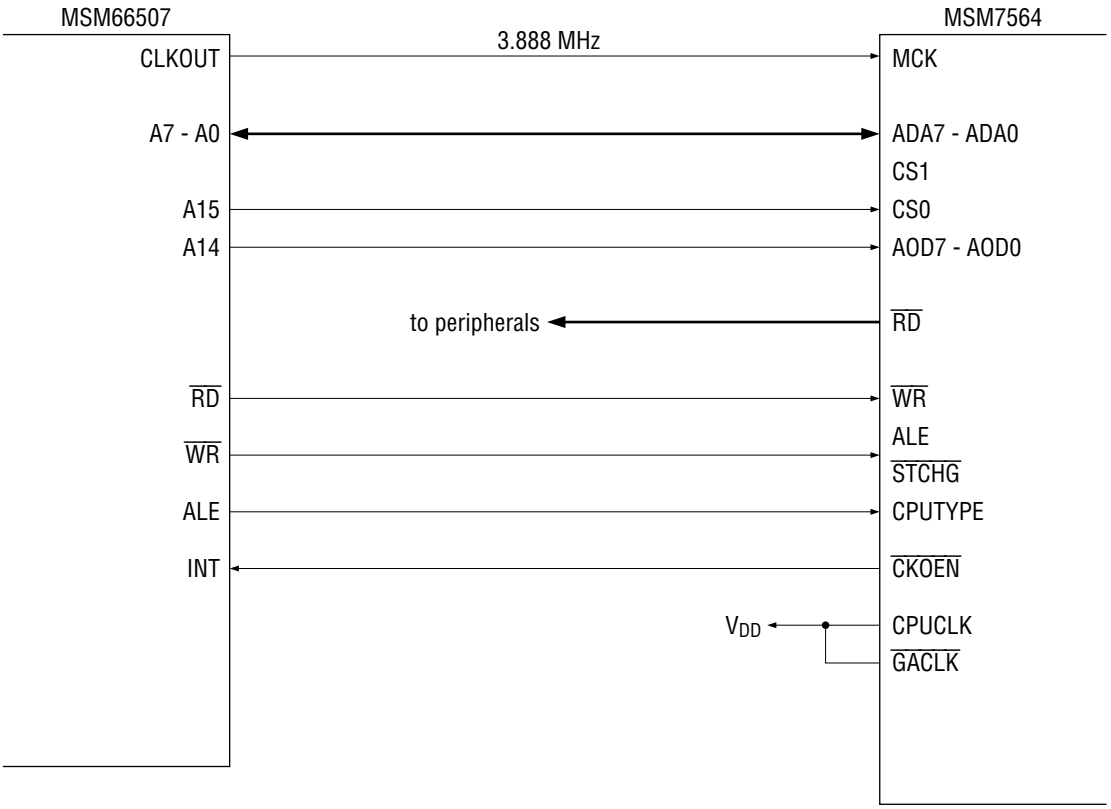
CPU Interface1

The modem supports an interface to connect directly to separate address-data bus such as a Motorola-compatible CPU (68 mode : ex. Z80). The master clock (3.888 MHz) is assumed to be supplied from an external crystal. The clock for Z80 or gate array clock generated in this device is sent from CPUCLK and GACLK pins. The outline of connection is as follows.



CPU Interface 2

The modem supports an interface to connect directly to a multiplexed address-data bus such as an Intel-compatible CPU (80 mode : ex. MSM66507). The master clock (3.888 MHz) is assumed to be supplied from clock out pin of an external CPU. Internal address latch and address output pins for peripherals are also provided. The outline of connection is as follows.



Analog Interface