1.1 Scope.

This specification covers the detail requirements for Class B microcircuits in accordance with 1.2.1 of MIL-STD-883, provisions for the use of MIL-STD-883 in conjunction with complaint non-JAN devices. The device is a 40 MHz Monolithic 256 × 24 Color Palette RAM-DAC.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	ADV453TQ/883B
−2	ADV453TE/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description	Lead Finish
Q	Q-40	40-Lead Dual-In-Line Package	Hot Solder DIP
E	E-44A	44-Lead LCC	Hot Solder DIP

1.3 Absolute Maximum Ratings.

Supply Voltage (V_{AA}) . . . . . +7.0 V
Digital Input Voltage (V_{IN}) to AGND . . . . . −0.5 V to V_{AA} +0.5 V
Analog Output Short Circuit Duration to Any Power Supply or Common . . . . . Indefinite
Power Dissipation . . . . . 1575 mW
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering 10 sec) . . . . . +300°C
Junction Temperature . . . . . +175°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = See MIL-M-38510 Appendix C
θ_{JA} = 120°C/W for Q
θ_{JA} = 50°C/W for E

ADV453—SPECIFICATIONS

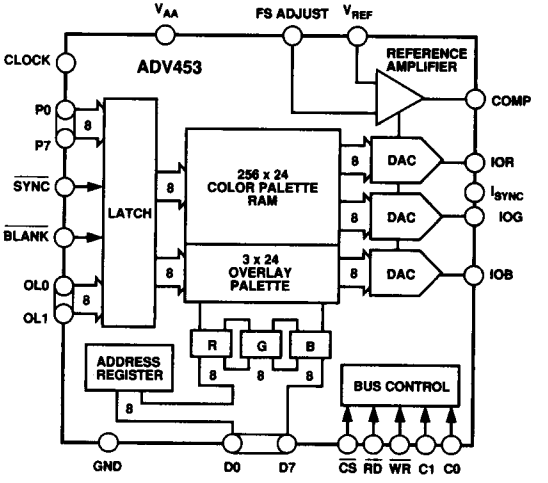
Table 1.

Test	Symbol	Limit Min	Limit Max	Group A Subgroups	Conditions[1] ($-55°C \le T_A \le +125°C$ unless otherwise noted)	Units
Resolution (Each DAC)		8.0	8.0	4		Bits
Relative Accuracy (Each DAC) Integral Nonlinearity	I_L		±2	1, 2, 3		LSB
Differential Nonlinearity	D_L		±1	1, 2, 3	Conversion Rate is 1 MHz	LSB
Gray Scale Error			±5	1, 2, 3	White Level Relative to Blank	% Gray Scale
Digital Input High Voltage	V_{IH}	2.4		7, 8		V
Digital Input Low Voltage	V_{IL}		0.8	7, 8		V
Digital Input Current	I_{IN}		10	1, 2, 3	V_{IN} = 0 V or V_{AA}	μA
Digital Input Capacitance[2]	C_{IN}		10	4		pF
Digital Output High Voltage	V_{OH}	2.4		1, 2, 3	I_{SOURCE} = 400 μA	V
Digital Output Low Voltage	V_{OL}		0.4	1, 2, 3	I_{SINK} = 3.2 mA	V
Floating State Output Current	I_{OZ}		10	1, 2, 3	V_{IN} = 0 V or V_{AA}	μA
Floating State Output Capacitance[2]	CD_{OUT}		20	4		pF
Gray Scale Current Range		15	22	1, 2, 3		mA
Output Current White Level Relative to Blank		17.69	20.40	1, 2, 3		mA
White Level Relative to Black		16.74	18.50			
Black Level Relative to Blank		0.95	1.90			
Blank Level on IOR, IOB		0	50	1, 2, 3		μA
Blank Level on IOG		6.29	8.96			mA
Sync Level on IOG		0	50			μA
DAC to DAC Matching			6	1, 2, 3	White Level Relative to Blank	%
Output Compliance[3]	V_{OC}	−1.0	1.4	1, 2, 3		V
Output Capacitance[2]	CA_{OUT}		40	4	I_{OUT} = 0 mA	pF
Voltage Reference Range[3]		1.14	1.26	1, 2, 3		V
Power Supply Current	I_{AA}		300	1, 2, 3		mA
Power Supply Rejection Ratio (White Level Relative to Black)	PSRR		30	1, 2, 3	V_{AA} = 5.0 V Delta V_{AA} = +5% or −5% (0.5 V 1 kHz Sinewave Applied to V_{AA})	dB
$\overline{CS}$ C0, C1 Setup Time	t_1	35		9, 10, 11		ns
$\overline{CS}$ C0, C1 Hold Time	t_2	35		9, 10, 11		ns
$\overline{RD}$, $\overline{WR}$ High Time	t_3	25		9, 10, 11		ns
$\overline{RD}$ Assert to Data Bus Driven	t_4	2		9, 10, 11		ns
$\overline{RD}$ Assert to Data Valid	t_5		100	9, 10, 11		ns
$\overline{RD}$ Negated to Data Bus Three Stated	t_6		20	9, 10, 11		ns
$\overline{RD}$, $\overline{WR}$ Low Time	t_7	50		9, 10, 11		ns

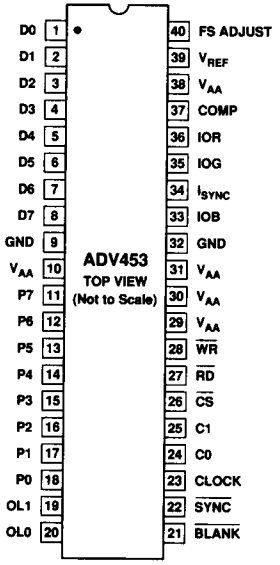
Test	Symbol	Limit Min	Limit Max	Group A Subgroups	Conditions[1] ($-55°C \le T_A \le +125°C$ unless otherwise noted)	Units
Write Data Setup Time	t_8	35		9, 10, 11		ns
Write Data Hold Time	t_9	10		9, 10, 11		ns
Pixel and Control Setup Time	t_{10}	7		9, 10, 11		ns
Pixel and Control Hold Time	t_{11}	3		9, 10, 11		ns
Clock Cycle Time[3]	t_{12}	25		9, 10, 11		ns
Clock Pulse Width High Time	t_{13}	7		9, 10, 11		ns
Clock Pulse Width Low Time	t_{14}	7		9, 10, 11		ns
Analog Output Delay	t_{15}		30	9, 10, 11	CLK = 4 MHz	ns
Analog Output Rise/Fall Time	t_{16}		8	9, 10, 11	CLK = 4 MHz	ns
Pipeline Delay[3]	t_{PD}		$2 \times t_{12}$	9, 10, 11		ns
Analog Output Skew	t_{SK}		2	9, 10, 11	CLK = 4 MHz	ns

NOTES
[1]V_{AA} = +4.75 V to +5.25 V, V_{REF} = 1.235 V, R_{SET} = 280 Ω, I_{SYNC} connected to IOG, unless otherwise specified.
[2]Tested on initial release and after any redesign which may affect this parameter.
[3]These tests are done on a pass/fail basis only. Minimum and/or maximum conditions (as appropriate) are used as input conditions.
[4]Digital input values are 0 to 3 V, with input rise/fall time, < 3 ns measured between the 10% and 90% points. Timing reference points are at 50% for inputs an outputs. See Figure 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



Q Package (DIP)



E Package (LCC)

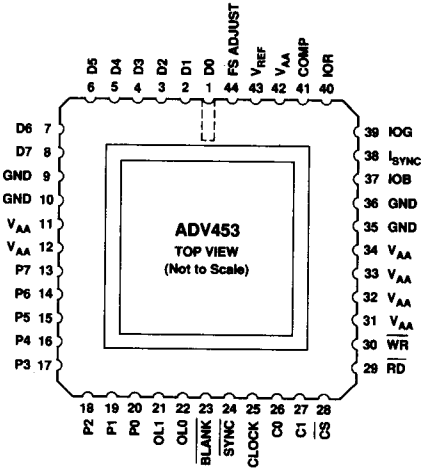


Table 2. Electrical Test Requirements

MIL-STD-883 Test Requirements	Subgroups (Per Method 5005 Table 1)
Interim Electrical Parameters (Method 5004)	1, 7, 9
Final Electrical Test Parameters (Method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A Test Requirements (Method 5005)	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group C and D Endpoint Electrical Parameters (Method 5005)	1, 7, 9

*PDA applies to subgroup 1.

4.3.2 Group C and D Inspections

a. Endpoint electrical parameters shall be as specified in Table 2 herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.
Test Condition A, B, C or D using the circuit in E Package Drawing.
T_A = 125°C, Min
Test Duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. Packing

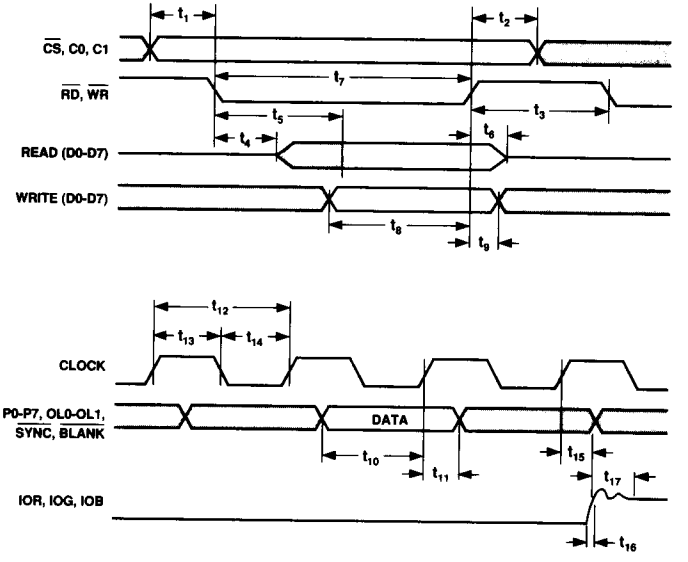
5.1 Packaging Requirements

The requirements for packaging shall be in accordance with MIL-M-38510.

Table 3.

Description	IOG (mA)	IOR, IOB (mA)	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
White Level	26.67	19.05	1	1	FFH
Video	Video + 9.05	Video + 1.44	1	1	Data
Video to Blank	Video + 1.44	Video + 1.44	0	1	Data
Black Level	9.05	1.44	1	1	00H
Black to Blank	1.44	1.44	0	1	00H
Blank Level	7.62	0	1	0	XXH
SYNC Level	0	0	0	0	XXH

Notes
1. Typical with full scale IOG = 26.67 mA.
2. V_{REF} = +1.235 V, R_{SET} = 280 Ω. I_{SYNC} connected to IOG.



NOTES
1. OUTPUT DELAY (t_{15}) MEASURED FROM THE 50% POINT OF THE RISING EDGE OF CLOCK TO THE 50% POINT OF FULL SCALE TRANSITION.
2. SETTLING TIME (t_{17}) MEASURED FROM THE 50% POINT OF FULL SCALE TRANSITION TO THE OUTPUT REMAINING WITHIN ±1LSB.
3. OUTPUT RISE/FALL TIME (t_{16}) MEASURED BETWEEN THE 10% AND 90% POINTS OF FULL SCALE TRANSITION.

Figure 1. Timing Diagrams