

HD14046B

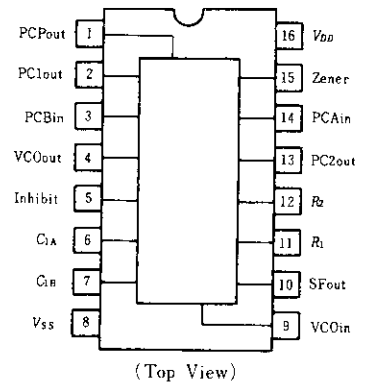
Phase-Locked Loop

The HD14046B phase-locked loop contains two phase comparators, a voltage-controlled oscillator (VCO), source follower, and zener diode. The comparators have two common signal inputs, PCAin and PCBin. Input PCAin can be used directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. The self-bias circuit adjusts small voltage signals in the linear region of the amplifier. Phase comparator 1 (an exclusive OR gate) provides a digital error signals PC1 out, and maintains 90° phase shift at the center frequency between PCAin and PCBin signals (both at 50% duty cycle). Phase comparator 2 (with leading edge sensing logic) provides digital error signals PC2out and PCPout, and maintains a 0° phase shift between PCAin and PCBin signals (duty cycle is immaterial). The linear VCO produces an output signal VCOout whose frequency is determined by the voltage of input VCOin and the capacitor and resistors connected to pins C1A, C1B, R1, and R2. The source-follower output SFout with an external resistor is used where the VCOin signal is needed but no loading can be tolerated. The inhibit input Inh, when high, disables the VCO and source follower to minimize standby power consumption. The zener diode can be used to assist in power supply regulation. Applications include FM and FSK modulation and demodulation, frequency synthesis and multiplication, frequency discrimination, tone decoding, data synchronization and conditioning, voltage-to-frequency conversion and motor speed control.

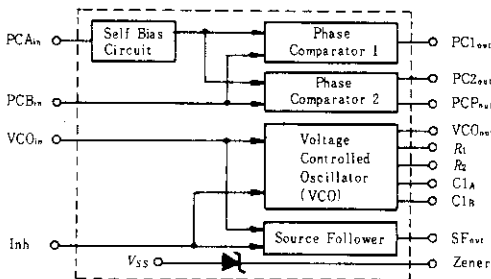
FEATURES

- VCO Frequency = 1.4MHz typ. @10V
- VCO Frequency Drift with Temperature = 0.04%/°C typ. @10V
- VCO Linearity = 1% typ.
- Quiescent Current = 5nA/pkg @5V
- Low Dynamic Power Dissipation = 70μW typ. @f₀ = 10kHz,
- V_{DD} = 5V, R₁ = 1MΩ, R₂ = ∞, R_{SF} = ∞
- Diode Protection on All Inputs
- Supply Voltage Range = 3 to 18V
- Pin-for-Pin Replacement for CD4046B and MC14046B

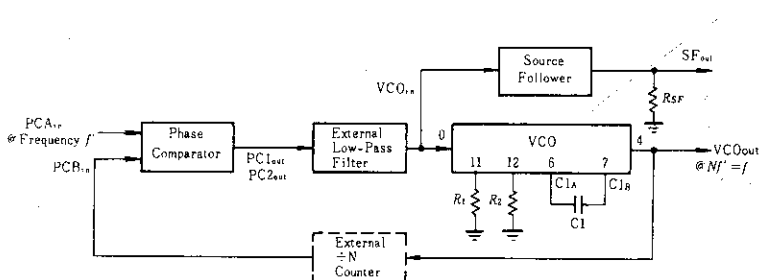
PIN ARRANGEMENT



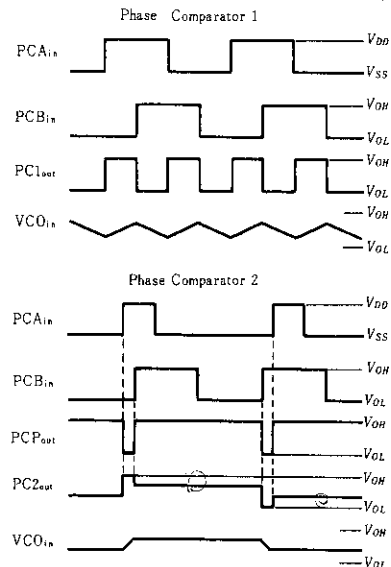
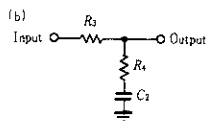
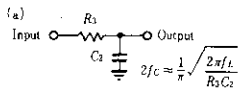
BLOCK DIAGRAM



■ GENERAL PHASE-LOCKED LOOP CONNECTIONS AND WAVEFORMS



Typical Low-Pass Filters



■ ELECTRICAL CHARACTERISTICS—1

Characteristic	Symbol	Test Conditions	-40°C		25°C		85°C		Unit	
			min	max	min	typ	max	min		max
Output Voltage	VOL	5.0	—	0.05	—	0	0.05	—	0.05	V
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	VOH	5.0	4.95	—	4.95	5.0	—	4.95	—	V
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage	VIL	5.0	—	1.5	—	2.25	1.5	—	1.5	V
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	VIH	5.0	3.5	—	3.5	2.75	—	3.5	—	V
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current	IOH	5.0	-1.0	—	-0.8	-1.7	—	-0.6	—	mA
		5.0	-0.2	—	-0.16	-0.36	—	-0.12	—	
		10	-0.5	—	-0.4	-0.9	—	-0.3	—	
		15	-1.4	—	-1.2	-3.5	—	-1.0	—	
	IOL	5.0	0.52	—	0.44	0.88	—	0.36	—	mA
		10	1.3	—	1.1	2.25	—	0.9	—	
15		3.6	—	3.0	8.8	—	2.4	—		
Input Current	Iin	15	—	±0.3	—	±0.0001	±0.3	—	±1.0	μA
Input Capacitance	Cin	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current	IDD	5.0	—	20	—	0.005	20	—	150	μA
		10	—	40	—	0.010	40	—	300	
		15	—	80	—	0.015	80	—	600	
Total Supply Current*	IT	5.0	—	—	—	1.46	—	—	—	μA
		10	—	—	—	2.91	—	—	—	
		15	—	—	—	4.37	—	—	—	

* To calculate total supply current at frequency other than 1kHz.

@VDD = 5.0V IT = (1.46 μA/kHz)f + IDD, @VDD = 10V IT = (2.91 μA/kHz)f + IDD, @VDD = 15V IT = (4.37 μA/kHz)f + IDD

■ ELECTRICAL CHARACTERISTICS—2 ($C_L = 50\text{ pF}$, $T_a = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD} (V)	Test Conditions	min	typ	max	Unit
Output Rise Time	t_r	5.0		—	180	400	ns
		10		—	90	200	
		15		—	65	160	
Output Fall Time	t_f	5.0		—	100	200	ns
		10		—	50	100	
		15		—	37	80	

● PHASE COMPARATORS 1 and 2

Characteristic	Symbol	V_{DD} (V)	Test Conditions	min	typ	max	Unit
Input Resistance	PCBin	5.0		1.0	2.0	—	M Ω
		10		0.2	0.4	—	
		15		0.1	0.2	—	
	PCBin	15		15	1500	—	
Minimum Input Sensitivity	$\cdot V_{in}$	5.0	AC Coupled—PCBin,	—	200	400	mV _{p-p}
		10	C Series=1000pF,	—	400	800	
		15	$f = 50\text{ kHz}$	—	700	1400	
DC Coupled-PCBin,PCBin		5~15		See Noise Immunity			

● VOLTAGE CONTROLLED OSCILLATOR(VCO)

Characteristic	Symbol	V_{DD} (V)	Test Conditions	min	typ	max	Unit
Maximum Frequency	f_{max}	5.0	$V_{COin} = V_{DD}$, $C_1 = 50\text{ pF}$, $R_1 = 5\text{ k}\Omega$, $R_2 = \infty$	0.35	0.70	—	MHz
		10		0.7	1.4	—	
		15		1.0	1.9	—	
Temperature-Frequency Stability		5.0	$R_2 = \infty$	—	0.12	—	%/°C
		10		—	0.04	—	
		15		—	0.015	—	
Linearity		5.0	$V_{COin} = 2.50\text{ V} \pm 0.30\text{ V}$, $R_1 \geq 10\text{ k}\Omega$	—	1	—	%
		10	$V_{COin} = 5.00\text{ V} \pm 2.50\text{ V}$, $R_1 \geq 400\text{ k}\Omega$	—	1	—	
		15	$V_{COin} = 7.50\text{ V} \pm 5.00\text{ V}$, $R_1 \geq 1000\text{ k}\Omega$	—	1	—	
Output Duty Cycle		5~15		—	50	—	%
Input Resistance (VCOin)	R_{in}	15		15	1500	—	M Ω

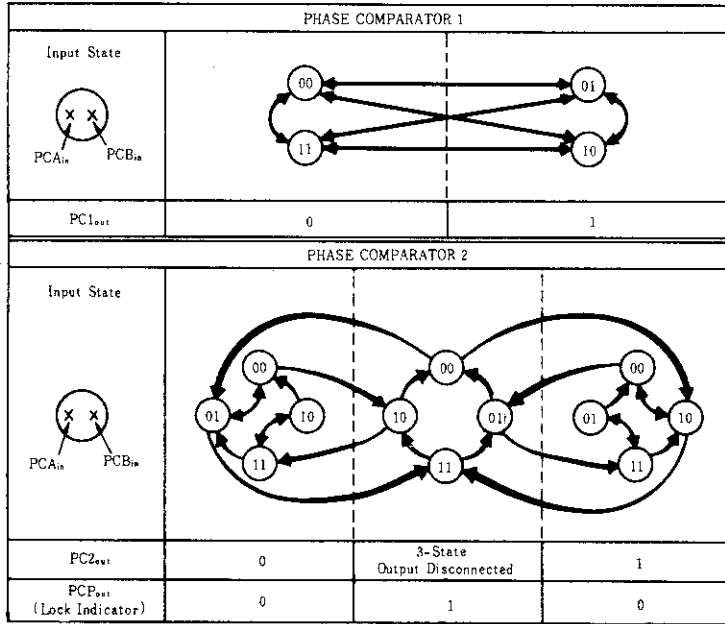
● SOURCE-FOLLOWER

Characteristic	Symbol	V_{DD} (V)	Test Conditions	min	typ	max	Unit
Offset Voltage		5.0	$V_{COin} = SF_{out}$, $R_{SF} > 50\text{ k}\Omega$	—	1.65	2.5	V
		10		—	1.65	2.5	
		15		—	1.65	2.5	
Linearity		5.0	$V_{COin} = 2.50\text{ V} \pm 0.30\text{ V}$, $R_{SF} > 50\text{ k}\Omega$	—	0.1	—	%
		10	$V_{COin} = 5.00\text{ V} \pm 2.50\text{ V}$, $R_{SF} > 50\text{ k}\Omega$	—	0.6	—	
		15	$V_{COin} = 7.50\text{ V} \pm 5.00\text{ V}$, $R_{SF} > 50\text{ k}\Omega$	—	0.8	—	

● ZENER DIODE

Characteristic	Symbol	V_{DD} (V)	Test Conditions	min	typ	max	Unit
Zener Voltage	V_Z		$I_Z = 50\text{ }\mu\text{A}$	6.3	7.0	7.7	V
Dynamic Resistance	R_Z		$I_Z = 1\text{ mA}$	—	100	—	Ω

■ PHASE COMPARATORS STATE DIAGRAMS





Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

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