19-1403; Rev 0; 11/98

EVALUATION KIT MANUAL FOLLOWS DATA SHEET

MAXIM

Compact, High-Efficiency, Dual-Output Step-Up and LCD Bias DC-DC Converter

General Description

The MAX1677 is a compact, high-efficiency, dual-output boost converter for portable devices needing two regulated supplies, typically for logic and liquid crystal displays (LCDs). Operation with inputs as low as 0.7V allows the MAX1677 to accept 1, 2, or 3-cell alkaline, NiCd, or NiMH batteries as well as 1-cell lithium-ion batteries. The device requires no external FETs and can maintain regulation while consuming only 20µA, making it ideal for hand-held pen-input and PDA devices operating with low-current "sleep" states.

The MAX1677's primary regulator supplies up to 350mA at either a factory-preset 3.3V or an adjustable 2.5V to 5.5V output. On-chip synchronous rectification provides efficiencies up to 95%. 300kHz (or externally clocked) pulse-width-modulation (PWM) operation is particularly suitable for applications needing low noise, such as those with wireless features. The primary converter also features pin-selectable pulse-frequency-modulation (PFM) operation that consumes only 20µA. A 1µA shutdown state also minimizes battery drain.

The MAX1677's secondary step-up converter supplies up to +28V or -28V for LCD bias, varactor tuning, or other high-voltage, low-current functions. Other MAX1677 features include precision reference, logic control inputs for both regulators, and an uncommitted comparator for low-battery detection or a reset function. The MAX1677 is supplied in Maxim's compact 16-pin QSOP package, which occupies no more space than a standard SO-8.

Applications

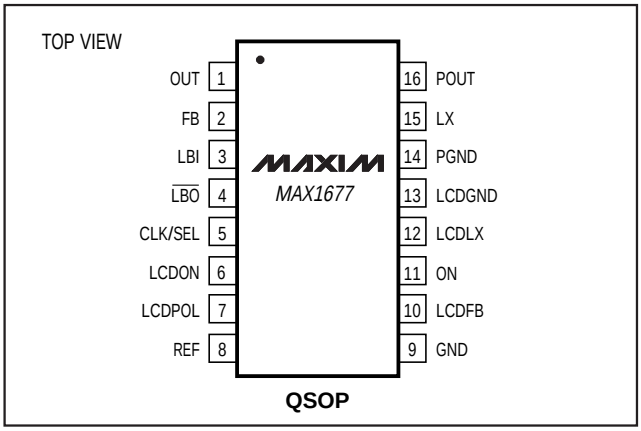
PDAs

Hand-Held Terminals

Portable Phones

Portable Instruments

Pin Configuration



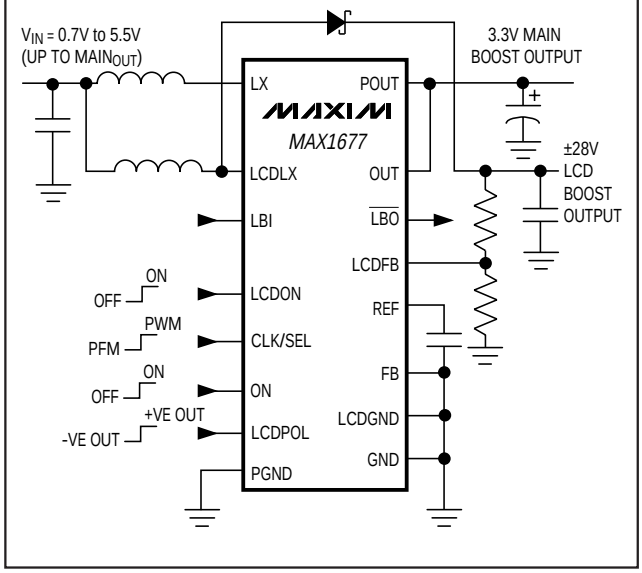
Features

- **No External FETs Required**
- **Main Output**
  - **Up to 350mA for Logic Supply**
  - **Fixed 3.3V or Adjustable (2.5V to 5.5V)**
  - **Synchronous Rectification for High Efficiency (up to 95%)**
  - **300kHz (200kHz to 400kHz Synchronizable) Fixed-Frequency PWM Operation**
- **Secondary Output**
  - **Up to +28V or -28V for LCD Bias**
  - **Programmable Current Limit**
- **0.7V to 5.5V Input Voltage Range**
- **20µA Quiescent Current**
- **1µA Shutdown Current**
- **Low-Battery Comparator**
- **Small 16-Pin QSOP Package**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1677EEE	-40°C to +85°C	16 QSOP

Typical Operating Circuit



Compact, High-Efficiency, Dual-Output Step-Up and LCD Bias DC-DC Converter

ABSOLUTE MAXIMUM RATINGS

OUT, LCDON, ON, POUT, LBI, $\overline{LBO}$,
LX to GND .....-0.3V to +6V
CLK/SEL, LCDPOL, REF, LCDFB,
FB to GND .....-0.3V to (V_{OUT} + 0.3V)
LCDLX to GND .....-0.3V to +30V
PGND, LCDGND to GND .....-0.3V to +0.3V
POUT to OUT.....-0.3V to +0.3V

Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 8.3mW/°C above +70°C).....696mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{OUT} = 3.3V, C_{REF} = 0.1µF, POUT = OUT, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL						
Input Voltage Range	V_{IN}	(Note 1)	0.7		5.5	V
Minimum Start-Up Voltage	$V_{STARTUP}$	T_A = +25°C, I_{LOAD} < 1mA		0.9	1.1	V
Reference Voltage	V_{REF}	I_{REF} = 0	1.23	1.25	1.27	V
Reference Load Regulation		I_{REF} = 0 to 50µA (Note 2)		2	15	mV
Reference Line Rejection		V_{OUT} = 2.5V to 5.5V		0.2	5	mV
Supply Current Main DC On, LCD Off	I_{LCDOFF}	No load, current into OUT		20	40	µA
Supply Current All On, Main DC-DC in PFM Mode	I_{PFM}	No load, current into OUT		35	60	µA
Supply Current All On, Main DC-DC in PWM Mode	I_{PWM}	No load, current into OUT		115	300	µA
Supply Current in Shutdown				0.3	5	µA
MAIN BOOST DC-DC						
Output Voltage	V_{OUT}	FB = GND, 0 ≤ I_{LX} ≤ 350mA, CLK/SEL = OUT (Note 3)	3.20	3.30	3.43	V
FB Regulation Voltage	$V_{FB(REG)}$	Adjustable mode, CLK/SEL = OUT (Note 3)	1.225	1.25	1.275	V
FB Input Current	I_{FB}	V_{FB} = 1.3V		0.02	50	nA
Output Voltage Adjustment Range			2.5		5.5	V
Start-Up to Normal Mode Transition Voltage (Note 4)	$V_{LOCKOUT}$		2.1		2.4	V
Line Regulation		I_{OUT} = 150mA, V_{IN} = 2V to 3V		0.6		%
Load Regulation		CLK/SEL = OUT, V_{IN} = 2.4V, I_{LOAD} = 10mA to 200mA		1		%
Frequency in Start-Up Mode	$f_{STARTUP}$	V_{OUT} = 1.5V	40		300	kHz
LX Leakage Current	$I_{LX(LEAK)}$			0.2	5	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{OUT} = 3.3V, C_{REF} = 0.1µF, POUT = OUT, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LX On-Resistance	$R_{LX(ON)N}$	N-channel		0.22	0.5	Ω
	$R_{LX(ON)P}$	P-channel		0.4	1.0	
LX Current Limit	$I_{LX(PWM)}$	N-channel PWM mode	550	670	800	mA
	$I_{LX(PFM)}$	N-channel PFM mode	250	350	450	
P-Channel Synchronous Rectifier Turn-Off Current in PFM Mode			40	90	140	mA
Internal Oscillator	f	CLK/SEL = OUT	240	300	360	kHz
Oscillator Maximum Duty Cycle	D		80	85	90	%
External Clock Frequency Range			200		400	kHz
LOGIC AND CONTROL INPUTS						
Input Leakage Current		ON, LCDON, LCDPOL, CLK/SEL			1	µA
ON Input Threshold	$V_{ON(LOW)}$	1.1V < V_{OUT} < 5.5V			$0.2V_{OUT}$	V
	$V_{ON(HIGH)}$		$0.8V_{OUT}$			
LCDON, LCDPOL, CLK/SEL Input Threshold	V_{IL}	V_{OUT} > 2.5V			$0.2V_{OUT}$	V
	V_{IH}		$0.8V_{OUT}$			
LBI Falling Threshold	$V_{LBI(TH)}$		599	614	629	mV
LBI Hysteresis				1		%
$\overline{LBO}$ Output Low Voltage	$V_{\overline{LBO}(LO)}$	Sink current = 1mA			0.1	V
LBI Input Bias Current	$I_{LBI(BIAS)}$				50	nA
$\overline{LBO}$ Leakage Current	$I_{\overline{LBO}(LEAK)}$	$V_{\overline{LBO}}$ = 5.5V			1	µA
LCD BIAS DC-DC						
LCDLX Voltage					28	V
LCDLX Switch Current Limit		LCDPOL = OUT or GND	300	350	450	mA
		LCDPOL connected to OUT or GND through 50kΩ	150	225	300	
LCDLX Switch Resistance	R_{LCDLX}	V_{OUT} = 3.3V		1.0	1.4	Ω
LCDLX Leakage Current		V_{LCDLX} = 28V			1	µA
LCDFB Set Point		Positive LCD, LCDPOL = OUT	1.225	1.25	1.275	V
		Negative LCD, LCDPOL = GND	-15	0	15	mV
LCDFB Input Bias Current					50	nA
LCD Line Regulation		I_{LOAD} = 5mA, V_{IN} = 1.2V to 3.6V, Figure 2		0.1		%/V
LCD Load Regulation		I_{LOAD} = 0 to 5mA, V_{IN} = 2.4V, Figure 2		0.5		%
Maximum LCDLX On-Time	$t_{ON\ LCD}$		3.4	4.3	5.2	µs
Minimum LCDLX Off-Time		Operating mode	0.8	1	1.2	µs
		Start-up mode (positive or negative)	3.0	4.0	5.0	
LCDFB Voltage for Start-Up Mode		LCDPOL = OUT		0.75		V
		LCDPOL = GND		0.5		

ELECTRICAL CHARACTERISTICS

(V_{OUT} = 3.3V, C_{REF} = 0.1µF, POUT = OUT, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
GENERAL					
Supply Current Main DC On, LCD Off	I_{LCDOFF}	No load, current into OUT		40	µA
Supply Current All On, Main DC-DC in PFM Mode	I_{PFM}	No load, current into OUT		60	µA
Supply Current All On, Main DC-DC in PWM Mode	I_{PWM}	No load, current into OUT		300	µA
Supply Current in Shutdown				5	µA
MAIN BOOST DC-DC					
Output Voltage	V_{OUT}	FB = GND, 0 ≤ I_{LX} ≤ 350mA, CLK/SEL = OUT (Note 3)	3.17	3.4	V
FB Regulation Voltage	$V_{FB(REG)}$	Adjustable mode, CLK/SEL = OUT (Note 3)	1.22	1.28	V
Start-Up to Normal Mode Transition Voltage (Note 4)	$V_{LOCKOUT}$		2.1	2.4	V
LX Leakage Current	$I_{LX(LEAK)}$			5	µA
LX Current Limit	$I_{LX(PWM)}$	N-channel PWM mode	550	900	mA
	$I_{LX(PFM)}$	N-channel PFM mode	250	500	
Internal Oscillator	f	CLK/SEL = OUT	240	360	kHz
External Clock Frequency Range			200	400	kHz
LOGIC AND CONTROL INPUTS					
ON Input Threshold	$V_{ON(LOW)}$	1.1V < V_{OUT} < 5.5V		0.2V_{OUT}	V
	$V_{ON(HIGH)}$		0.8V_{OUT}		
LCDON, LCDPOL, CLK/SEL Input Threshold	V_{IL}			0.2V_{OUT}	V
	V_{IH}		0.8V_{OUT}		
LBI Falling Threshold	$V_{LBI(TH)}$		599	629	mV
$\overline{LBO}$ Output Low Voltage	$V_{\overline{LBO}(LO)}$	Sink current = 1mA		0.1	V
LCD BIAS DC-DC					
LCDLX Switch Current Limit		LCDPOL = OUT or GND	300	450	mA
		LCDPOL connected to OUT or GND through 50kΩ	150	300	
LCDFB Set Point		Positive LCD, LCDPOL = OUT	1.22	1.28	V
		Negative LCD, LCDPOL = GND	-20	+20	mV

Note 1: The MAX1677 operates in bootstrap mode (operates from the output voltage). Once started, it will operate down to 0.7V input. If V_{IN} exceeds the set V_{OUT}, V_{OUT} will follow one diode drop below V_{IN}.

Note 2: C_{REF} = 0.22µF for applications where I_{REF} > 10µA.

Note 3: In low-power mode (CLK/SEL = GND), the output voltage regulates 1% higher than in low-noise mode (CLK/SEL = OUT or synchronized).

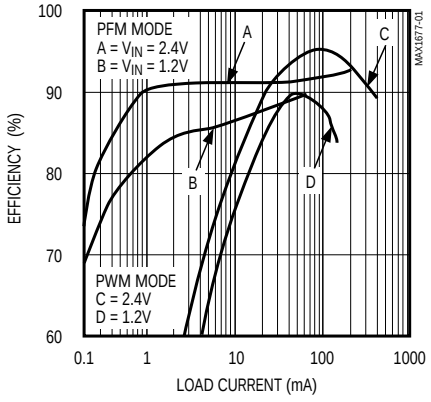
Note 4: The device is in a start-up mode when V_{OUT} is below this value.

Note 5: Specifications to -40°C are guaranteed by design and not production tested.

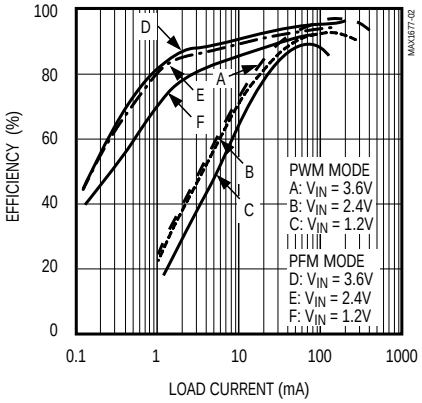
Typical Operating Characteristics

(Circuits of Figures 2 and 3, T_A = +25°C, unless otherwise noted.)

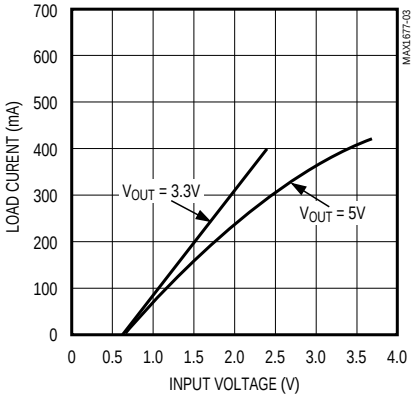
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 3.3V)



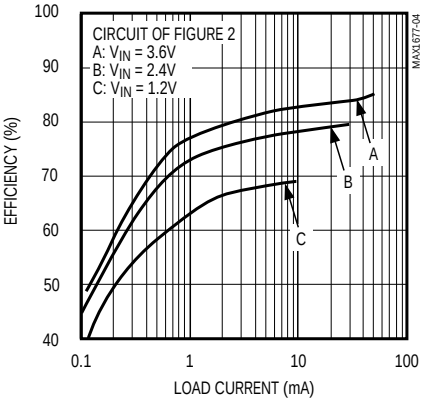
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 5V)



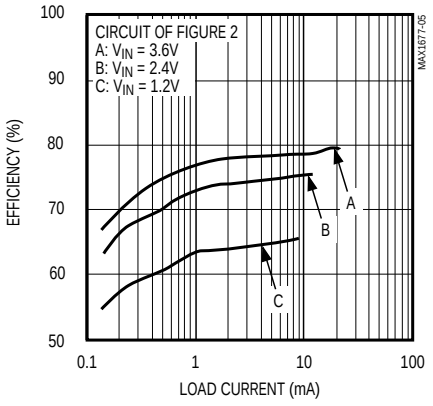
MAXIMUM LOAD CURRENT vs. BATTERY INPUT VOLTAGE (PWM MODE)



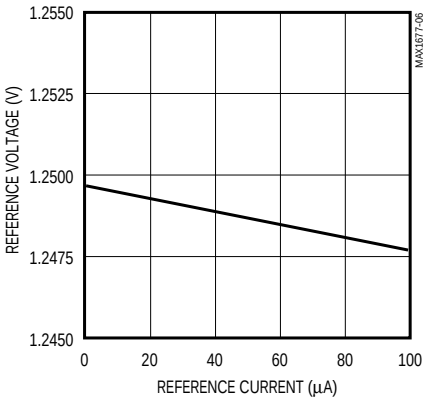
EFFICIENCY vs. LOAD CURRENT (LCD V_{OUT} = 12V)



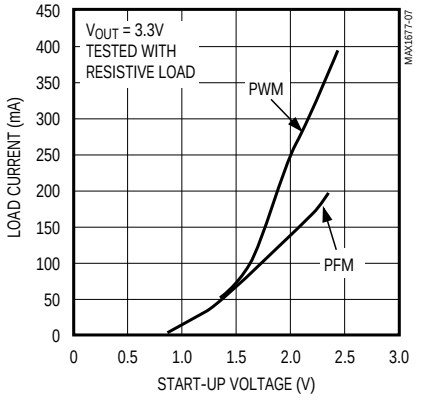
EFFICIENCY vs. LOAD CURRENT (LCD V_{OUT} = 20V)



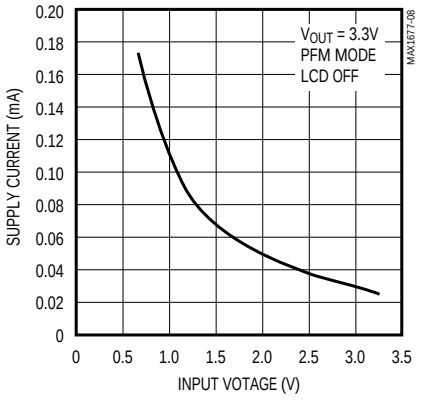
REFERENCE VOLTAGE vs. REFERENCE CURRENT



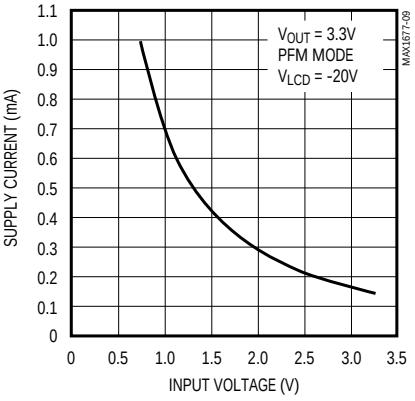
LOAD CURRENT vs. START-UP VOLTAGE



NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (LCD OFF)



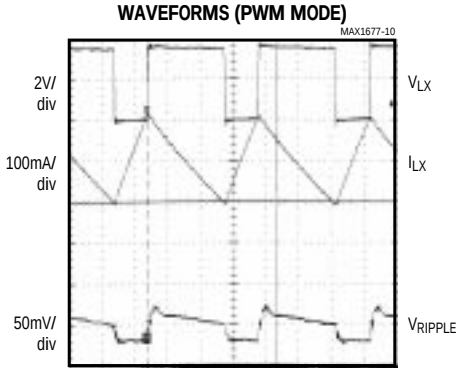
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (LCD ON)



Typical Operating Characteristics (continued)

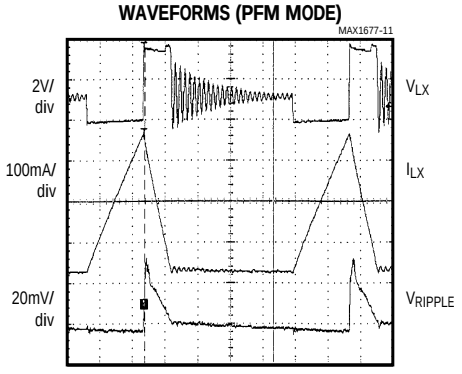
(Circuits of Figures 2 and 3, T_A = +25°C, unless otherwise noted.)

MAIN BOOST CONVERTER SWITCHING WAVEFORMS (PWM MODE)



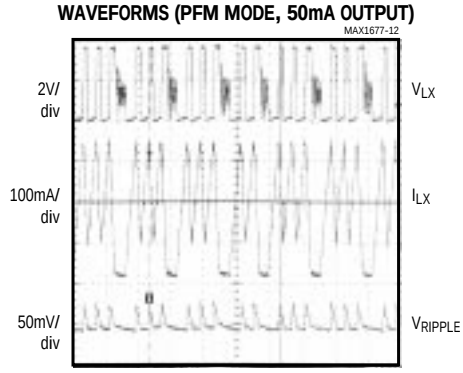
2.4V_{IN}, 3.3V_{OUT}, 200mA I_{OUT}

MAIN BOOST CONVERTER SWITCHING WAVEFORMS (PFM MODE)



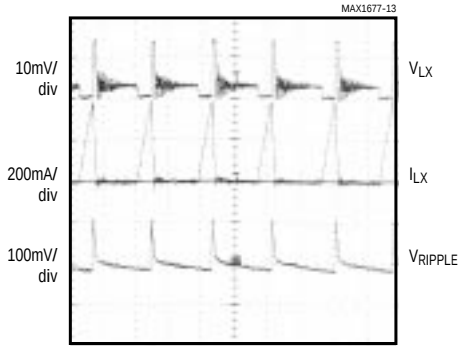
1.2V_{IN}, 3.3V_{OUT}, 20mA I_{OUT}

MAIN BOOST CONVERTER SWITCHING WAVEFORMS (PFM MODE, 50mA OUTPUT)



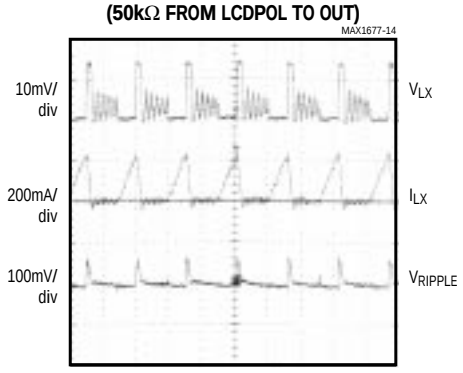
PFM, 1.2V_{IN}, 3.3V_{OUT}, 50mA I_{OUT}

LCD SWITCHING WAVEFORMS



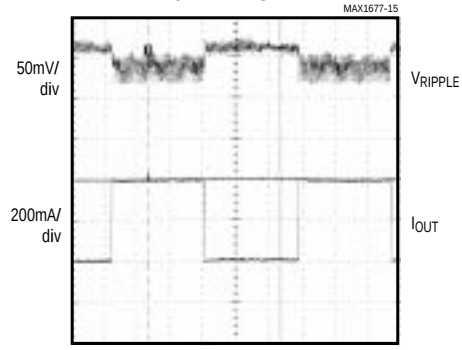
LDCLX CURRENT LIMIT = 350mA, 2.4V_{IN}, +12V_{OUT}, 10mA LOAD

LCD SWITCHING WAVEFORMS (50kΩ FROM LCDPOL TO OUT)



LCDLX CURRENT LIMIT = 225mA, 2.4V_{IN}, +12V_{OUT}, 10mA LOAD

MAIN BOOST CONVERTER LOAD TRANSIENT

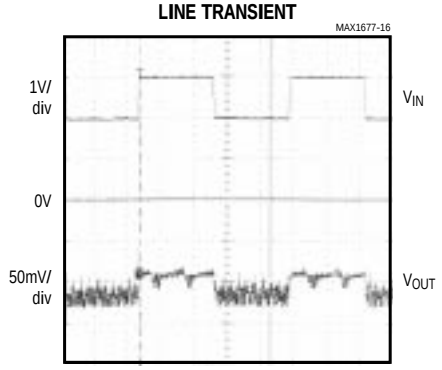


V_{IN} = 2.4V, V_{OUT} = 3.3V
I_{LOAD} = 0 to 200mA

Typical Operating Characteristics (continued)

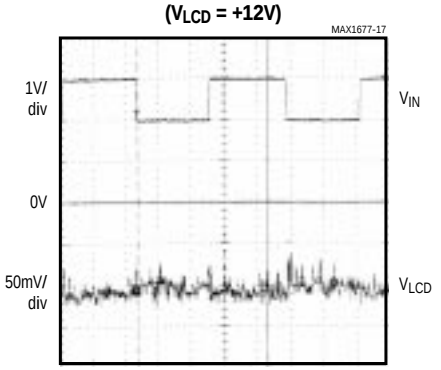
(Circuits of Figures 2 and 3, T_A = +25°C, unless otherwise noted.)

MAIN BOOST CONVERTER LINE TRANSIENT



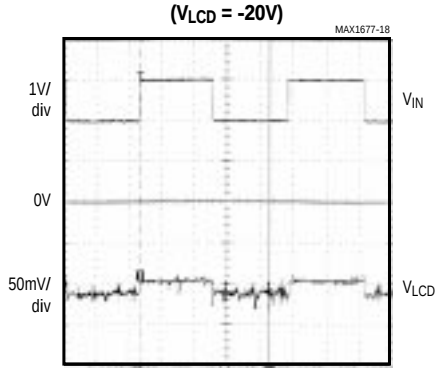
V_{IN} = 2V TO 3V, V_{OUT} = 3.3V,
I_{LOAD} = 150mA

LCD LINE TRANSIENT (V_{LCD} = +12V)



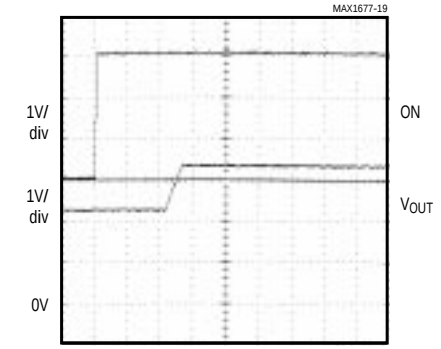
V_{IN} = 2V TO 3V, V_{LCD} = +12V,
I_{OUT} = 5mA

LCD LINE TRANSIENT (V_{LCD} = -20V)



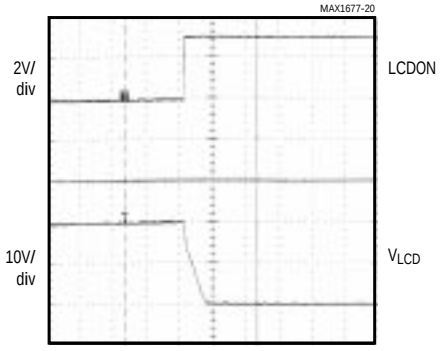
V_{IN} = 2V TO 3V, V_{LCD} = -20V,
I_{OUT} = 5mA

MAIN BOOST CONVERTER START-UP DELAY



V_{IN} = 2.4V, V_{OUT} = 3.3V,
I_{LOAD} = 10mA

LCD START-UP DELAY



V_{IN} = 2.4V, V_{LCD} = -20V,
I_{OUT} = 5mA

Compact, High-Efficiency, Dual-Output Step-Up and LCD Bias DC-DC Converter

Pin Description

PIN	NAME	FUNCTION
1	OUT	Output Sense Input. The device is powered from OUT. Bypass to GND with a 0.1µF ceramic capacitor. Connect OUT to POUT through a 10Ω series resistor.
2	FB	Dual Mode™ Main Boost Feedback Input. Connect to GND for 3.3V output. Connect a voltage-divider from OUT to FB to adjust the output in the 2.5V to 5.5V range (Figure 5).
3	LBI	Low-Battery-Comparator Input. Threshold is 614mV. Set the low-battery trip-point with an external voltage divider (Figure 7).
4	$\overline{LBO}$	Open-Drain, Low-Battery Output. $\overline{LBO}$ is low when LBI is below 614mV, otherwise it remains high.
5	CLK/SEL	Sync Clock and PWM Select Input. CLK/SEL = low: low-power, low-quiescent-current PFM mode. CLK/SEL = high: low-noise, high-power PWM mode at 300kHz. CLK/SEL = driven with external clock of 200kHz to 400kHz, synchronized PWM high-power mode.
6	LCDON	LCD Enable Input. Drive high to turn on LCD boost converter. Main DC-DC must also be on.
7	LCDPOL	LCD Polarity Select Input. Sets LCD boost converter polarity and peak current output (Table 2).
8	REF	1.25V Reference Output. Bypass with 0.1µF.
9	GND	Ground
10	LCDFB	LCD Feedback Input. Threshold is 1.25V for positive with LCDPOL high, and 0 for negative with LCDPOL low.
11	ON	I.C. Enable Input. Drive high to enable the MAX1677.
12	LCDLX	LCD Boost 28V Switch Drain
13	LCDGND	Source of the Internal N-Channel DMOS LCD Boost-Converter Switch
14	PGND	Source of the Internal N-Channel Main Boost-Converter Switch
15	LX	Main Output Boost Internal Switch Drain
16	POUT	Boost DC-DC Converter Power Output. Source of internal P-channel MOSFET main boost-converter synchronous rectifier.

Dual Mode is a trademark of Maxim Integrated Products.

Detailed Description

The MAX1677 is a highly efficient dual-output power supply for battery-powered devices. On-chip are two complete step-up DC-DC converters to power main logic and bias an LCD (Figure 1). The main boost converter (MBC) has on-chip P-channel and N-channel MOSFETs that provide synchronous-rectified voltage conversion for maximum efficiency at loads up to 300mA. See Table 1 for available output current with typical battery configurations. The output voltage of the MBC is factory-preset to 3.3V, or can be set from 2.5V to 5.5V with external resistors (dual-mode operation). Either fixed-frequency PWM or low-operating-current PFM operation can be selected for the MBC using the CLK/SEL input (Table 2).

The LCD boost converter (LCD) includes an internal N-channel DMOS switch to generate positive or negative voltages up to ±28V. The polarity of the LCD output is set by LCDPOL input (Table 3). Figure 2 shows the MAX1677 configured for a positive LCD output voltage with a 3.3V main output. Figure 3 shows the MAX1677 configured for a negative LCD output. LCDPOL also allows the current limit of LCDLX to be reduced from 350mA to 225mA to allow minimum-size inductors in low-current LCD applications (typically for LCD loads <10mA).

Also included in the MAX1677 are a precision 1.25V reference that sources up to 50µA, logic shutdown control for the MBC and LCD (the MBC must be on for the LCD to operate), and a low-battery comparator.

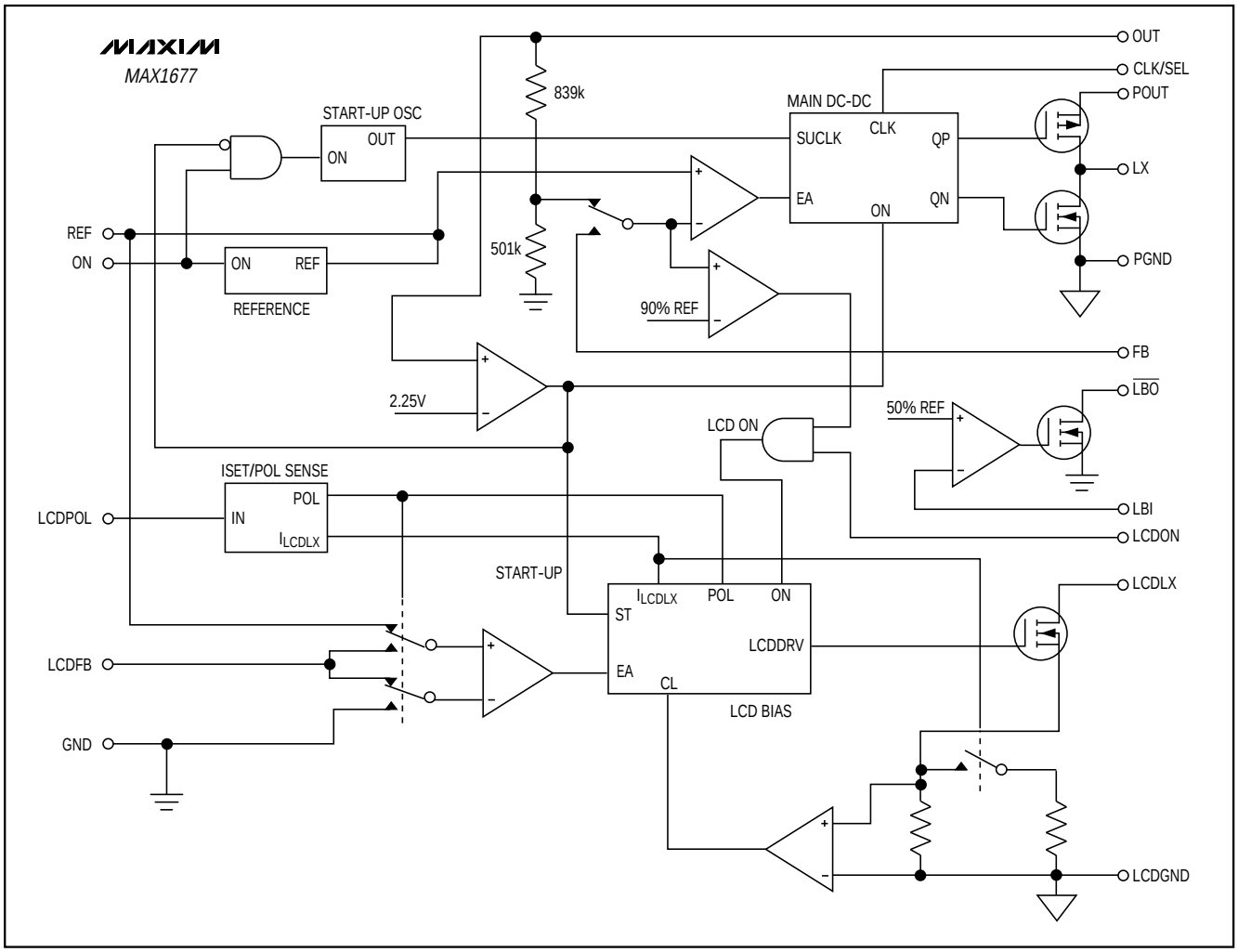


Figure 1. Functional Block Diagram

Table 1. Main Boost Converter Available Output Current

NUMBER OF CELLS	INPUT VOLTAGE (V)	MBC OUTPUT VOLTAGE (V)	MBC OUTPUT CURRENT (mA) PWM/PFM
1 Alk/NiCd/NiMH	1.2	3.3	140/150
1 Alk/NiCd/NiMH	1.2	5	100/70
2 Alk/NiCd/NiMH	2.4	3.3	350/170
2 Alk/NiCd/NiMH	2.4	5	260/125
1 Alk/NiCd/NiMH or 1 Li-Ion	3.6	5	350/170

Main Boost Converter (MBC)

The MBC operates either in PFM mode, 300kHz PWM mode, or externally synchronized PWM mode as selected by the CLK/SEL input (Table 2). PWM mode offers fixed-frequency operation and maximum output power. PFM mode offers the lowest IC operating current. LX current limit is reduced in PFM mode to increase efficiency and minimize output ripple.

PWM Mode

When CLK/SEL is high, the MAX1677 operates in its high-power, low-noise PWM mode, switching at the 300kHz internal oscillator frequency. The MOSFET switch pulse-width is modulated to control the power transferred on each switching cycle and regulate the

Compact, High-Efficiency, Dual-Output Step-Up and LCD Bias DC-DC Converter

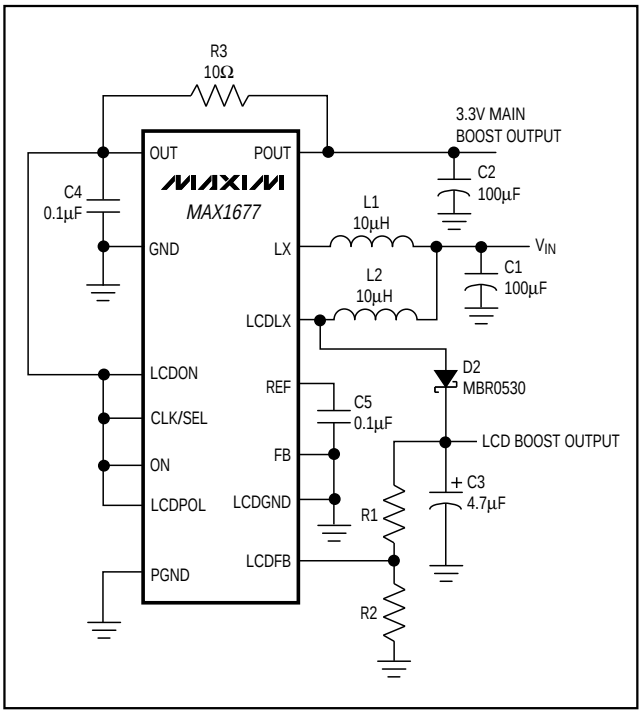


Figure 2. LCD Converter in Positive Mode

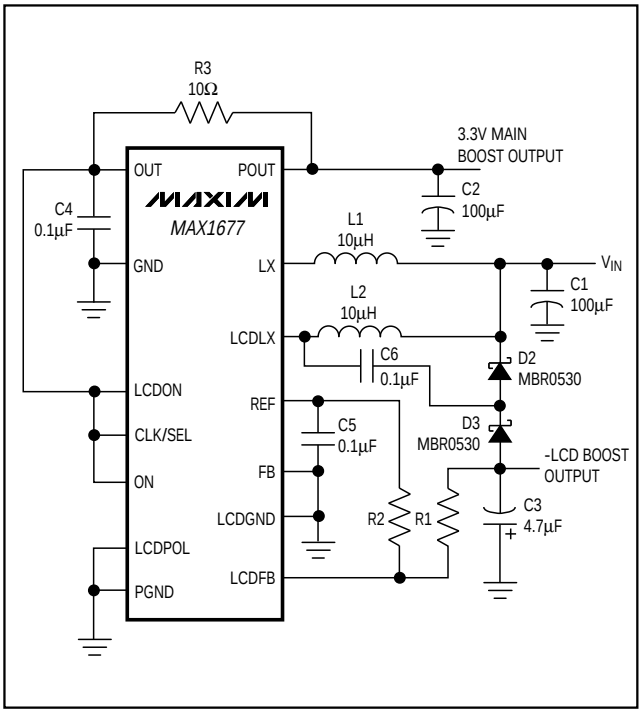


Figure 3. LCD Converter in Negative Mode

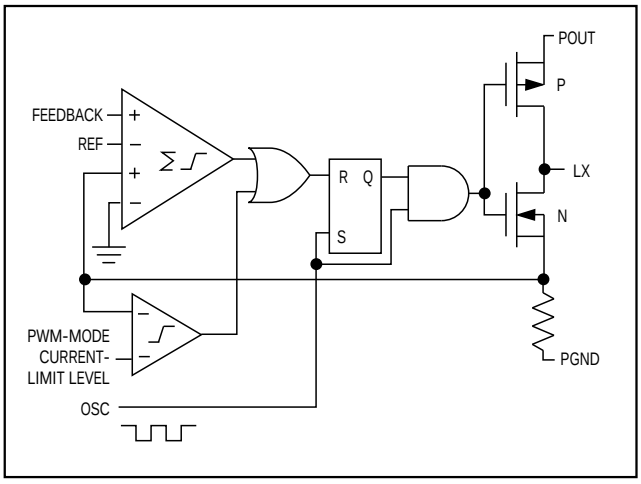


Figure 4. Controller Block Diagram in PWM Mode

output voltage. In PWM mode, the MBC can supply up to 350mA. Switching harmonics generated by the fixed-frequency operation are consistent and easily filtered.

During PWM operation, the rising edge of the internal clock sets a flip-flop, which turns on the N-channel MOSFET (Figure 4). The switch turns off when the sum of the voltage-error, slope-compensation, and current-feedback signals trips the multi-input comparator and resets the flip-flop; the switch remains off for the rest of the cycle. Changes in the output voltage error signal shift the inductor current level and modulate the MOSFET pulse width.

Clock-Synchronized PWM

The MAX1677 operates as a clock-synchronized current-mode PWM when a clock signal (200kHz to 400kHz) is applied to CLK/SEL. This allows switching harmonics to be positioned to avoid sensitive frequency bands, such as those near IF frequencies in wireless applications.

Low Power PFM Mode

Pulling CLK/SEL low places the MAX1677 in low-power standby mode. During standby mode, PFM operation regulates the output voltage by transferring a fixed amount of energy during each cycle, and then modulating the switching frequency to control the power delivered to the output. The device switches only as needed to service the load, resulting in the highest possible efficiency at light loads and an operating current of only 20µA. The MBC can supply up to 170mA when in PFM mode (Table 1).

During PFM operation, the error comparator detects when the output voltage is out of regulation and sets a

flip-flop, turning on the N-channel MOSFET switch (Figure 5). When the inductor current ramps to the PFM mode current limit (350mA), the current-sense comparator resets a flip-flop. The flip-flop turns off the N-channel switch and turns on the P-channel synchronous rectifier. The energy stored in the inductor is transferred to the output through the P-channel switch. A second flip-flop, previously reset by the switch's "on" signal, inhibits the next cycle until the inductor current is depleted and the output is out of regulation. This forces operation with discontinuous inductor current in PFM mode.

Start-Up Oscillator

The MBC employs a low-voltage start-up oscillator to ensure a 1.1V (0.9V typical) start-up voltage. On start-up, if the output voltage is less than 2.25V, the P-channel switch stays off and the N-channel pulses at a 25% duty cycle. When the output voltage exceeds 2.25V, the normal PWM or PFM control circuitry takes over. Once the MBC is in regulation, it can operate with inputs down to 0.7V since the internal power for the IC is taken from OUT. The MBC cannot supply full output current until OUT reaches 2.5V.

Table 2. Selecting MBC Operating Mode

CLK/SEL	MBC MODE	FEATURES
0	Low-Power PFM	Lowest Supply Current
1	PWM	High Output Current, Fixed-Frequency Ripple
Ext Clock (200Hz to 400kHz)	Synchronized PWM	High Output Current, Synchronized Ripple Frequency

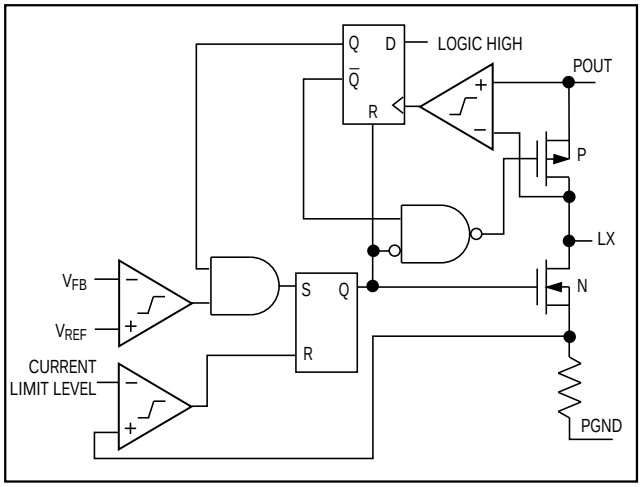


Figure 5. Controller Block Diagram in PFM Mode

Synchronous Rectifier

The MAX1677 MBC features an internal 1Ω P-channel synchronous rectifier. Synchronous rectification typically improves efficiency by 5% or more over similar non-synchronous step-up designs. In PWM mode, the synchronous rectifier turns on during the second half of each cycle. In PFM mode, an internal comparator turns on the synchronous rectifier when the voltage at LX exceeds the MBC output, and then turns it off when the inductor current drops below 90mA (typ).

The on-chip synchronous rectifier allows the external Schottky diode to be omitted in designs that operate from inputs exceeding 1.4V. In circuits operating below 1.4V (1-cell inputs, for example), connecting a Schottky diode in parallel with the internal synchronous rectifier (from LX to POUT) provides the lowest start-up voltage.

LCD Boost Converter (LCD)

The LCD converter can be configured for a positive or negative output by setting the LCDPOL pin and using the appropriate circuit (Figures 2 and 3, and Table 3). A combination of peak current limiting and a pair of one-shot timers control LCD switching. During the on-cycle the internal N-channel DMOS switch turns on, and inductor current ramps up until either the switch peak current limit is reached or the 5.2µs maximum on-time expires (typically at low input voltages). After the on-cycle terminates, the switch turns off and the output capacitor charges. The switch remains off until the error comparator initiates another cycle.

The LCDLX current limit is set by LCDPOL, as outlined in Table 3. The lower, 225mA peak current setting allows tiny low-current "chip" inductors to be used when powering smaller (less than 15 square inches) liquid crystal panels. Use the following equation to determine which LCDLX current-limit setting is required.

$$I_{LCD} = (0.7 \cdot I_{PK(LCD)} \cdot V_{IN(MIN)}) / (2 \cdot V_{LCD(MAX)})$$

where I_{LCD} is the output current, $V_{IN(MIN)}$ is the minimum expected input voltage, $V_{LCD(MAX)}$ is the maximum required LCD output voltage, and $I_{PK(LCD)}$ is 350mA or 225mA as set by LCDPOL. The 0.7 term is a correction factor to conservatively account for typical switch, inductor, and diode losses.

The LCD boost is enabled when both ON and LCDON are high, *and* the MBC output voltage is within 90% of its set value. A soft-start start-up mode with increased off time reduces transient input current when the LCD is activated.

Compact, High-Efficiency, Dual-Output Step-Up and LCD Bias DC-DC Converter

Table 3. Setting LCD Output Polarity and Peak Inductor Current

LCD OUTPUT POLARITY	LCDPOL CONNECTED TO:	L_{CDLX} PEAK INDUCTOR CURRENT (mA)
Positive	OUT	350
Negative	GND	350
Positive	OUT through 50kΩ	225
Negative	GND through 50kΩ	225

Shutdown: ON and LCDON

A logic-low level at ON shuts down all MAX1677 circuits including the LCD converter, reference, and LBI comparator. A logic-high level at LCDON activates the LCD boost converter. The LCD boost converter can only be activated when ON is high. When ON is low, the MAX1677 draws 1µA.

Low-Battery Comparator

The MAX1677 has an on-chip comparator for low-battery detection. If the voltage at LBI falls below 614mV, $\overline{LBO}$ (an open-drain output) sinks current to GND. The low-battery trip level is set by two resistors (Figure 6). Since the LBI input current is less than 50nA, large resistor values (R6 ≤ 130kΩ) can be used to minimize input loading. Calculate R5 as follows:

$$R5 = R6\ [(V_{TRIP} / 0.614V) - 1]$$

Connect a pull-up resistor (R8) to $\overline{LBO}$ when driving CMOS logic. $\overline{LBO}$ is an open-drain output and can be pulled as high as 6V regardless of the voltage at OUT. When LBI is above 0.614V, $\overline{LBO}$ is high impedance. If the LBI comparator is not used, ground LBI.

Since the low-battery comparator is noninverting, hysteresis can be added by connecting a resistor (R7) from LBI to $\overline{LBO}$ as shown in Figure 7. When $\overline{LBO}$ is high, the series combination of R8 and R7 source current into the summing node at LBI (no current flows into the IC).

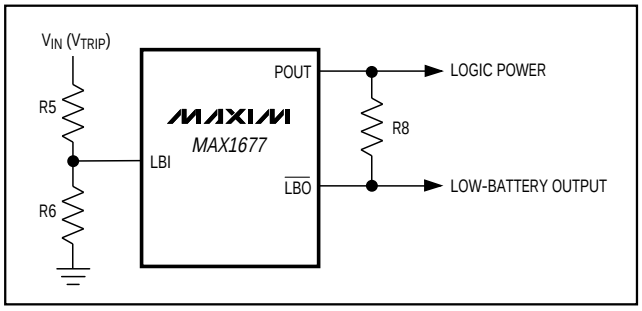


Figure 6. Setting the Low-Battery Trip Threshold

Design Procedure

The MBC feedback pin (FB) features Dual Mode operation. With FB grounded, the MBC output is preset to 3.3V. It can also be adjusted from 2.5V to 5.5V with external resistors, R3 and R4, as shown in Figure 8. To set the output voltage externally, select resistor R4 in the 10kΩ to 200kΩ range. Calculate R3 using:

$$R3 = R4\ [(V_{OUT} / 1.25V) - 1]$$

Setting the LCD Output Voltage

For either positive or negative LCD output voltages, set the voltage with two external resistors, R1 and R2, as shown in Figures 2 and 3. Since the input current at FB has a maximum of 50nA, large resistors can be used without significant accuracy loss. Begin by selecting R2 in the 10kΩ to 200kΩ range and calculate R1 using one of the following two equations (for positive or negative output).

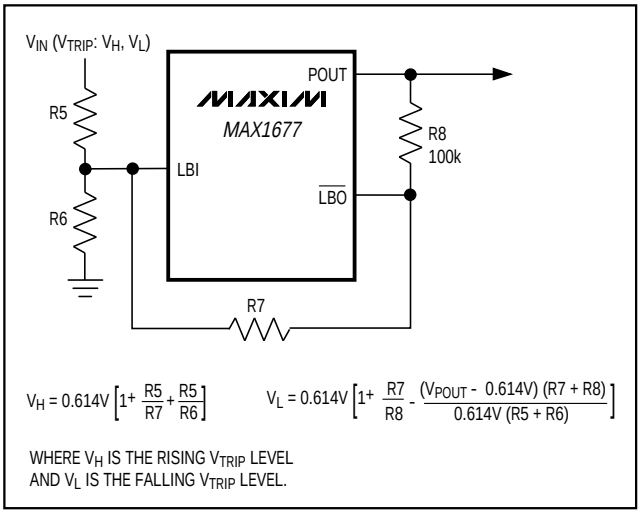


Figure 7. Adding External Hysteresis to the LBI Comparator

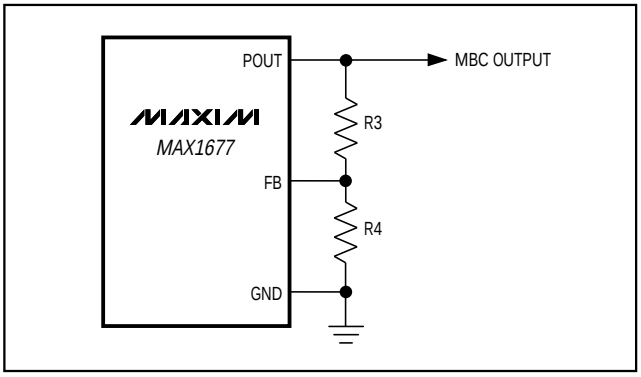


Figure 8. Setting the MBC Output Voltage Externally

For a positive LCD output, connect LCDPOL to OUT as shown in Figure 2. This sets the threshold at LCDFB to 1.25V. Select R2 and the desired output voltage (V_{LCD}), and calculate R1:

For positive LCD output: $R1 = R2\ [(V_{LCD} / 1.25V) - 1]$

Figure 3 shows the standard circuit for generating a negative LCD supply. This connection limits V_{LCD} to values between $-V_{IN}$ and -28V. If a smaller negative output voltage is required, D2's cathode can be connected to V_{IN} rather than ground. This alternate connection permits output voltages from 0 to $-|28 - V_{IN}|$.

For a negative LCD output voltage, connect LCDPOL to GND. The feedback threshold voltage of LCDFB is set to 0. Select R2 and the desired output voltage (V_{LCD}), and calculate R1:

For positive LCD output: $R1 = R2 \cdot |V_{LCD}| / 1.25V$

To minimize ripple in the LCD output and prevent subharmonic noise caused by switching pulse grouping, it may be necessary in some PC board layouts to connect a small capacitor in parallel with R1. For R1 values in 500kΩ to 2MΩ range, 22pF is usually adequate.

Many LCD bias applications require an adjustable output voltage. In Figure 9, an external control voltage (generated by a potentiometer, DAC, filtered PWM control signal, or other source) is coupled to LCDFB through the resistor R_{ADJ}. The output voltage of this circuit, for both positive and negative outputs, is given by:

$$V_{OUT} = V_{INIT} + (R1 / R_{ADJ})(V_{LCDFB} - V_{ADJ})$$

where V_{INIT} is the initial output obtained without the added adjust voltage, as calculated in one of the preceding two equations. V_{LCDFB} is 1.25V for the positive configuration, and 0 for the negative configuration. R_{ADJ} sets the output adjustment span, which is $1.25V \cdot R1 / R_{ADJ}$ for either polarity output. Note that raising V_{ADJ} lowers V_{OUT} in positive output designs, while in negative output designs, raising V_{ADJ} increases the magnitude of the negative output.

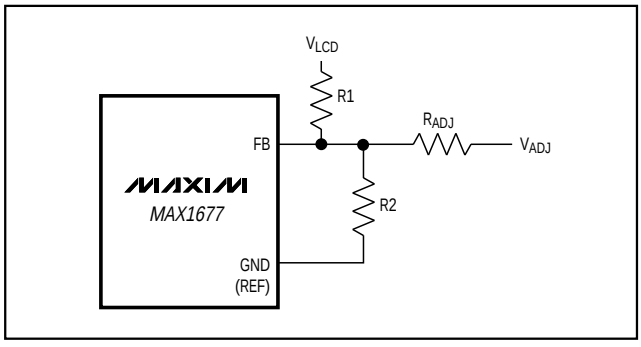


Figure 9. Adjusting LCD Output Voltage

Higher LCD Output Voltages

If the application requires LCD output voltages greater than +28V, use the connection in Figure 10. This circuit adds one capacitor-diode charge pump stage to increase the output voltage without increasing the voltage stress on the LCDLX pin. The maximum output voltage of the circuit is +55V and output current is slightly less than half that available from the standard circuit in Figure 2. In Figure 10, diodes D1, D2, and D3 should be at least 30V-rated Schottky diodes such as 1N5818 or MBR0530L or equivalent. Capacitors C1 and C2 should also be rated for 30V, while C3 must be rated for the maximum set output voltage.

Applications Information

Inductor Selection

The MAX1677's high switching frequency allows the use of small surface-mount inductors. The 10µH values shown in Figures 2 and 3 are recommended for most applications, although values between 4.7µH and 47µH are suitable. Smaller inductance values typically offer a smaller physical size for a given series resistance, allowing the smallest overall circuit dimensions. Larger inductance values exhibit higher output current capability, but larger physical dimensions.

Use inductors with a ferrite core or equivalent; powder iron cores are not recommended for use with the MAX1677's high switching frequencies. The inductor's incremental saturation rating ideally should exceed the

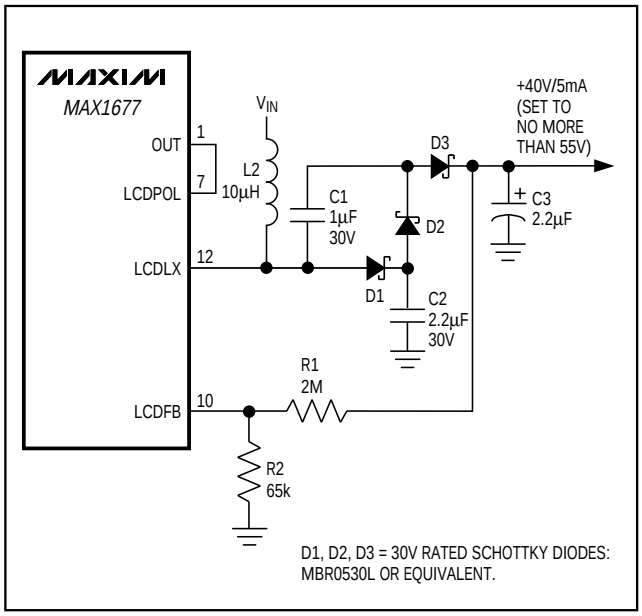


Figure 10. Higher LCD Output Voltage

selected current limit, however it is generally acceptable to bias most inductors into saturation by as much as 20% (although this may reduce efficiency).

For best efficiency, select inductors with resistance no greater than the internal N-channel FET resistance in each boost converter (220mΩ for the MBC, and 1Ω for the LCD). The inductor is effectively in series with the input at all times, so inductor wire losses can be roughly approximated by $I_{IN}^2 \cdot R_L$. See Table 4 for a list of inductor suppliers.

The LCD boost converter (LCD) features selectable inductor/switch current limit of 350mA or 225mA. The higher current setting provides the greatest output current, while the lower setting allows the smallest inductor size.

External Diodes

The MAX1677's on-chip synchronous rectifier allows the normally required external Schottky diode to be omitted from the MBC in designs whose input exceeds 1.4V. In circuits that need to operate below 1.4V (1-cell inputs for example), connecting a Schottky diode in parallel with the internal synchronous rectifier (from LX to POUT) provides the lowest start-up voltage. Suitable devices are the 1N5817 or MBR0520L, however the diode current rating need not match the peak switch current, since most of the current is handled by the on-chip synchronous rectifier.

Since the LCD boost converter (LCD) does not have synchronous rectification, an external diode is always needed. High switching speed demands a high-speed rectifier. For best efficiency, Schottky diodes such as the 1N5818 and MBR0530L are recommended. Be sure that the diode current rating exceeds the peak current set by LCDPOL, and that the diode voltage rating exceeds the LCD output voltage. In particularly cost-sensitive applications, and if the LCD's 225mA peak current is set, a high-speed silicon signal diode (such as an 1N4148) may be used instead of a Schottky diode, but with reduced efficiency.

Table 4. Component Suppliers

SUPPLIER	PHONE	FAX
INDUCTORS		
Coilcraft: DO and DT series	847-639-6400	847-639-1469
Murata: LQH4 and LQH3C series	814-237-1431	814-238-0490
Sumida: CD, CDR, and RCH series	847-956-0666	847-956-0702
TDK: NLC Series	847-390-4373	847-390-4428
CAPACITORS		
AVX: TPS series	803-946-0690	803-626-3123
Matsuo: 267 series	714-969-2591	714-960-6492
Sanyo: OS-CON and GX series	619-661-6835	619-661-1055
Sprague: 595D series	603-224-1961	603-224-1430
DIODES		
Motorola: MBR0520	602-303-5454	602-994-6430
Nihon: EC11 FS1 series	805-867-2555	805-867-2698

Input Bypass Capacitors

A low-ESR input capacitor connected in parallel with the battery will reduce peak currents and input-reflected noise. Battery bypassing is especially helpful at low input voltages and with high-impedance batteries (such as alkaline types). Benefits include improved efficiency and lower useful end-of-life voltage for the battery. 100µF is typically recommended for 2-cell applications. Small ceramic capacitors may also be used for light loads or in applications that can tolerate higher input ripple. Only one input bypass capacitor is typically needed for both the MBC and LCD.

Output Filter Capacitors

For most applications, a 100µF, 10V, low-ESR output filter capacitor is recommended for the MBC output. A surface-mount tantalum capacitor typically exhibits 30mV ripple when the MBC is stepping up from 1.2V to 3.3V at 100mA. OS-CON and ceramic capacitors offer lowest ESR, while low-ESR tantalums offer a good balance between cost and performance.

The LCD output typically exhibits less than 1% peak-to-peak ripple with 4.7µF of filter capacitance. This can be either a ceramic or tantalum type, but be sure that the capacitor voltage rating exceeds the LCD output voltage. If the LCD's 225mA peak switch current setting is used, the designer can choose lower output ripple or reduce the output filter to 2.2µF. Ceramic capacitors will exhibit lower ripple than equivalent value (or even higher value) tantalums due to lower ESR.

Layout Considerations

The MAX1677's high-frequency operation makes PC board layout important for minimizing ground bounce and noise. Protect sensitive analog grounds by using a star ground configuration. Minimize ground noise by connecting PGND, the input bypass capacitor ground terminal, and the output filter capacitor ground terminal to a single point (star ground configuration). Also, minimize lead lengths to reduce stray capacitance and trace resistance. Where an external resistor-divider is used to set output voltage, the trace from FB or LCDFB to the feedback resistors should be extremely short to minimize coupling from LX and LCDLX. To maximize efficiency and minimize output ripple, use a ground plane and connect the MAX1677 GND and PGND pins directly to the ground plane. Consult the MAX1677 evaluation kit for a full PC board example.

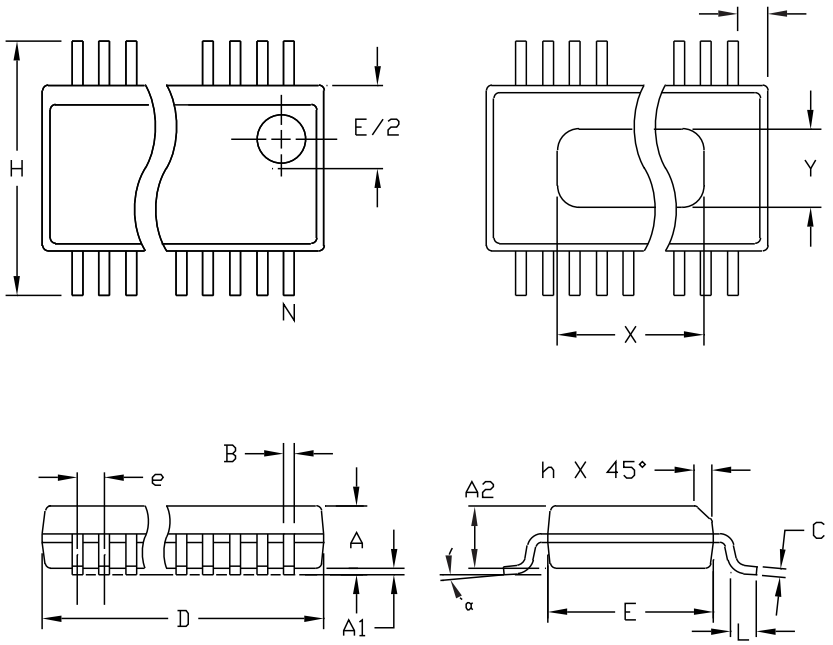
Chip Information

TRANSISTOR COUNT: 1221

Compact, High-Efficiency, Dual-Output Step-Up and LCD Bias DC-DC Converter

Package Information

QSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.

MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	B	1/1