19-2330; Rev 0; 1/02

MAXIM

Single-Supply 3V/5V, Voltage-Output, Dual, Precision 12-Bit DACs

General Description

The MAX5234/MAX5235 precision, dual-output, 12-bit digital-to-analog converters (DACs) consume only 360µA from a single 5V (MAX5235) or 325µA from a single 3V (MAX5234) supply. These devices feature output buffers that swing Rail-to-Rail®. The internal gain amplifiers maximize the dynamic range of the DAC output.

The MAX5234/MAX5235 feature a 13.5MHz 3-wire serial interface compatible with SPI™, QSPI™, and MICROWIRE™. Each DAC input is organized as an input register followed by a DAC register. A 16-bit shift register loads data into the input registers. Input registers update the DAC registers independently or simultaneously. In addition, programmable control bits allow power-down with 1kΩ or 200kΩ internal loads.

The MAX5234/MAX5235 are fully specified over the extended industrial temperature range (-40°C to +85°C) and are available in space-saving 10-pin µMAX packages.

Applications

Industrial Process Controls

Automatic Test Equipment

Digital Offset and Gain Adjustment

Motion Control

µP-Controlled Systems

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

SPI/QSPI are trademarks of Motorola, Inc.

MICROWIRE is a trademark of National Semiconductor Corp.

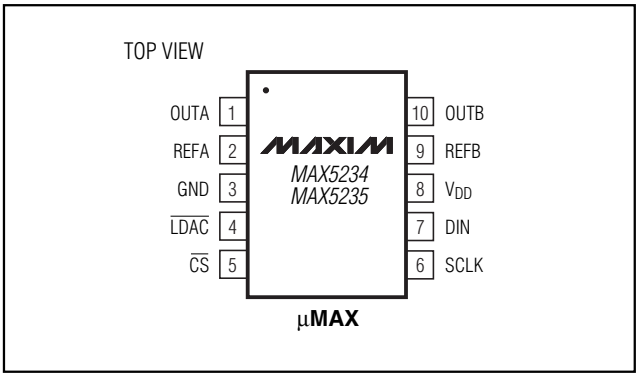
Features

- **Guaranteed 1/2LSB INL (max)**
- **Low Supply Current**
  325µA (Normal Operation)
  0.4µA (Full Power-Down Mode)
- **Single-Supply Operation**
  3V (MAX5234)
  5V (MAX5235)
- **Space-Saving 10-Pin µMAX Package**
- **Output Buffers Swing Rail-to-Rail**
- **Power-On Reset Clears Registers and DACs to Zero**
- **Programmable Shutdown Modes with 1kΩ or 200kΩ Internal Loads**
- **Resets to Zero**
- **13.5MHz SPI/QSPI/MICROWIRE-Compatible, 3-Wire Serial Interface**
- **Buffered Output Drives 5kΩ || 100pF**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	INL (LSB)
MAX5234AEUB	-40°C to +85°C	10 µMAX	±0.5
MAX5234BEUB	-40°C to +85°C	10 µMAX	±1
MAX5235AEUB	-40°C to +85°C	10 µMAX	±0.5
MAX5235BEUB	-40°C to +85°C	10 µMAX	±1

Pin Configuration



Single-Supply 3V/5V, Voltage-Output, Dual, Precision 12-Bit DACs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
Digital Inputs to GND .....-0.3V to +6V
REF_, OUT_ to GND .....-0.3V to (V_{DD} + 0.3V)
Maximum Current into Any Pin.....50mA

Continuous Power Dissipation (T_A = +70°C)
10-Pin µMAX (derate 5.60mW/°C above +70°C).....444mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX5235

(V_{DD} = +4.5V to +5.5V, GND = 0, V_{REFA} = V_{REFB} = +2.5V, R_L= 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution	N		12			Bits
Integral Nonlinearity	INL	MAX5235A (Note 1)			±0.5	LSB
		MAX5235B (Note 1)			±1	
Differential Nonlinearity	DNL				±1	LSB
Offset Error	V_{OS}	(Note 2)			±5	mV
Gain Error					±3	LSB
Full-Scale Voltage	V_{FS}	Code = FFF hex, T_A = +25°C (Note 3)	4.087	4.095	4.103	V
Full-Scale Temperature Coefficient	TCV_{FS}	Normalized to 4.095V		2		ppm/°C
Offset Temperature Coefficient	TCV_{OS}			±8		µV/°C
Power-Supply Rejection	PSR	4.5V ≤ V_{DD} ≤ 5.5V		15	200	µV
DC Crosstalk		(Note 4)			100	µV
REFERENCE INPUT						
Reference Input Range	V_{REF}	(Note 5)	0.25		2.60	V
Reference Input Resistance	R_{REF}	Minimum with code 555 hex and AAA hex	28	37		kΩ
Reference Current in Shutdown	I_{REF}				±1	µA
MULTIPLYING MODE PERFORMANCE						
Reference -3dB Bandwidth, Slew-Rate Limited		Input code = FFF hex, $V_{REF\_}$ = 0.5V_{P-P} + 1.5V_{DC}		350		kHz
Reference Feedthrough		Input code = 000 hex, $V_{REF\_}$ = 3.6V_{P-P} + 1.8V_{DC}, f = 1kHz		-80		dB
Signal-to-Noise plus Distortion Ratio	SINAD	Input code = FFF hex, $V_{REF\_}$ = 2V_{P-P} + 1.5V_{DC}, f = 10kHz		79		dB

ELECTRICAL CHARACTERISTICS—MAX5235 (continued)

(V_{DD} = +4.5V to +5.5V, GND = 0, V_{REFA} = V_{REFB} = +2.5V, R_L= 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUT						
Input High Voltage	V_{IH}		0.7 x V_{DD}			V
Input Low Voltage	V_{IL}				0.3 x V_{DD}	V
Input Hysteresis	V_{HYS}			200		mV
Input Leakage Current		Digital inputs = 0 or V_{DD}			±1	µA
Input Capacitance				8		pF
DYNAMIC PERFORMANCE						
Voltage-Output Slew Rate	SR			0.6		V/µs
Voltage-Output Settling Time		To ±0.5LSB, V_{STEP} = ±4V, 0.25V ≤ V_{OUT} ≤ (V_{DD} - 0.25V)		10		µs
Output-Voltage Swing		(Note 6)		0 to V_{DD}		V
Time Required for Output to Settle After Turning on V_{DD}		(Note 7)			70	µs
Time Required for Output to Settle After Exiting Full Power-Down		(Note 7)			70	µs
Time Required for Output to Settle After Exiting DAC Power-Down		(Note 7)			60	µs
Digital Feedthrough		$\overline{CS}$ = V_{DD}, f_{SCLK} = 100kHz, V_{SCLK} = $5V_{P-P}$		5		nV-s
Major-Carry Glitch Energy				40		nV-s
POWER SUPPLIES						
Power-Supply Voltage	V_{DD}		4.5		5.5	V
Power-Supply Current	I_{DD}	(Note 8)		360	450	µA
Power-Supply Current in Power-Down and Shutdown Modes	I_{SHDN}	Full power-down mode		1	5	µA
		One DAC shutdown mode		190	215	
		Both DACs shutdown mode		26	42	

Single-Supply 3V/5V, Voltage-Output, Dual, Precision 12-Bit DACs

ELECTRICAL CHARACTERISTICS—MAX5234

(V_{DD} = +2.7V to +3.6V, GND = 0, V_{REFA} = V_{REFB} = +1.25V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution	N		12			Bits
Integral Nonlinearity	INL	MAX5234A (Note 1)			±0.5	LSB
		MAX5234B (Note 1)			±1	
Differential Nonlinearity	DNL				±1	LSB
Offset Error	V_{OS}	(Note 2)			±5	mV
Gain Error	GE				±6	LSB
Full-Scale Voltage	V_{FS}	Code = FFF hex, T_A = +25°C (Note 3)	2.041	2.0475	2.054	V
Temperature Coefficient	TCV_{FS}	Normalized to 2.0475V		4		ppm/°C
Offset Temperature Coefficient	TCV_{OS}			±8		µV/°C
Power-Supply Rejection	PSR	2.7V ≤ V_{DD} ≤ 3.6V		18	280	µV
DC Crosstalk		(Note 4)			100	µV
REFERENCE INPUT						
Reference Input Range	V_{REF}	(Note 5)	0.25		1.50	V
Reference Input Resistance	R_{REF}	Minimum with code 555 hex and AAA hex	28	37		kΩ
Reference Current in Shutdown	I_{REF}				±1	µA
MULTIPLYING MODE PERFORMANCE						
Reference -3dB Bandwidth, Slew-Rate Limited		Input code = FFF hex, $V_{REF\_}$ = 0.5V_{P-P} + 0.75V_{DC}		350		kHz
Reference Feedthrough		Input code = 000 hex, $V_{REF\_}$ = 1.6V_{P-P} + 0.8V_{DC}, f = 1kHz		-80		dB
Signal-to-Noise plus Distortion Ratio	SINAD	Input code = FFF hex, $V_{REF\_}$ = 0.6V_{P-P} + 0.9V_{DC}, f = 10kHz		79		dB
DIGITAL INPUTS						
Input High Voltage	V_{IH}		0.7 x V_{DD}			V
Input Low Voltage	V_{IL}				0.3 x V_{DD}	V
Input Hysteresis	V_{HYS}			200		mV
Input Leakage Current		Digital inputs = 0 or V_{DD}			±1	µA
Input Capacitance				8		pF
DYNAMIC PERFORMANCE						
Voltage-Output Slew Rate	SR			0.6		V/µs
Voltage-Output Settling Time		To ±0.5LSB, V_{STEP} = ±2V, 0.25V ≤ V_{OUT} ≤ (V_{DD} - 0.25V)		10		µs
Output-Voltage Swing		(Note 6)		0 to V_{DD}		V

ELECTRICAL CHARACTERISTICS—MAX5234 (continued)

(V_{DD} = +2.7V to +3.6V, GND = 0, V_{REFA} = V_{REFB} = +1.25V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Time Required for Output to Settle After Turning on V_{DD}		(Note 7)			60	µs
Time Required for Output to Settle After Exiting Full Power-Down		(Note 7)			60	µs
Time Required for Output to Settle After Exiting DAC Power-Down		(Note 7)			50	µs
Digital Feedthrough		$\overline{CS}$ = V_{DD}, f_{SCLK} = 100kHz, V_{SCLK} = $3V_{P-P}$		5		nV-s
Major Carry Glitch Energy				115		nV-s
POWER SUPPLIES						
Power-Supply Voltage	V_{DD}		2.7		3.6	V
Power-Supply Current	I_{DD}	(Note 8)		325	430	µA
Power-Supply Current in Power-Down and Shutdown Modes	I_{SHDN}	Full power-down mode		0.4	5	µA
		One DAC shutdown mode		175	200	
		Both DACs shutdown mode		25	40	

TIMING CHARACTERISTICS—MAX5235 (FIGURES 1 AND 2)

(V_{DD} = +4.5V to +5.5V, GND = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Clock Period	t_{CP}		74			ns
SCLK Pulse Width High	t_{CH}		30			ns
SCLK Pulse Width Low	t_{CL}		30			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		30			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		30			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		10			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}		30			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		75			ns
$\overline{LDAC}$ Pulse Width Low	t_{LDL}		30			ns
$\overline{CS}$ Rise to $\overline{LDAC}$ Rise Hold Time	t_{CSLD}	(Note 9)	40			ns

TIMING CHARACTERISTICS—MAX5234 (FIGURES 1 AND 2)

(V_{DD} = +2.7V to +3.6V, GND = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Clock Period	t_{CP}		74			ns
SCLK Pulse Width High	t_{CH}		30			ns
SCLK Pulse Width Low	t_{CL}		30			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		30			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		30			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		10			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}		30			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		75			ns
$\overline{LDAC}$ Pulse Width Low	t_{LDL}		30			ns
$\overline{CS}$ Rise to $\overline{LDAC}$ Rise Hold Time	t_{CSLD}	(Note 9)	75			ns

Note 1: Accuracy is guaranteed in the following way:

V_{DD}	$V_{REF\_}$	ACCURACY GUARANTEED FROM CODE	TO CODE
3	1.250	20	4095
5	2.500	10	4095

Note 2: Offset is measured at the code closest to 10mV.

Note 3: Gain from $V_{REF\_}$ to $V_{OUT\_}$ is typically 1.638 x CODE/4096.

Note 4: DC crosstalk is measured as follows: set DAC A to midscale, and DAC B to zero, and measure DAC A output; then change DAC B to full scale and measure ΔV_{OUT} for DAC A. Repeat the same measurement with DAC A and DAC B interchanged. DC crosstalk is the maximum ΔV_{OUT} measured.

Note 5: The DAC output voltage is derived by gaining up V_{REF} by 1.638 x CODE/4096. This gain factor may cause V_{OUT} to try to exceed the supplies. The maximum value of V_{REF} in the reference input range spec prevents this from happening at full scale. The minimum V_{REF} value of 0.25V is determined by linearity constraints, not DAC functionality.

Note 6: Accuracy is better than 1LSB for V_{OUT} = 10mV to V_{DD} - 180mV.

Note 7: Guaranteed by design. Not production tested.

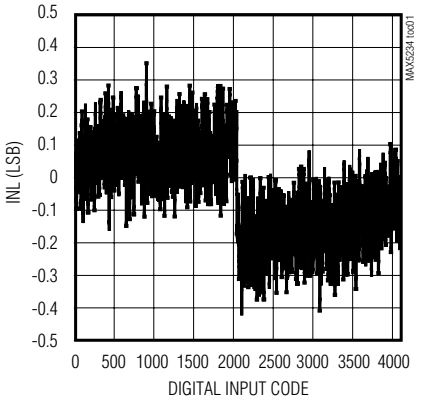
Note 8: R_{LOAD} = ∞ and digital inputs are at either V_{DD} or GND. V_{OUT} = full-scale output voltage.

Note 9: This timing requirement applies only to $\overline{CS}$ rising edges, which execute commands modifying the DAC input register contents.

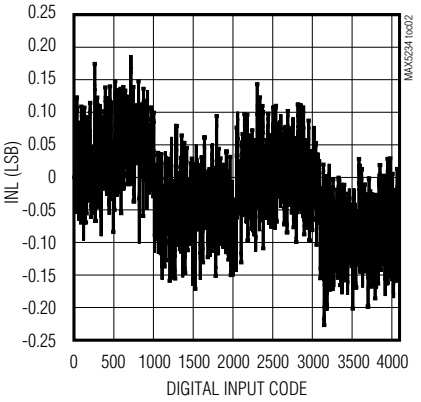
Typical Operating Characteristics

(V_{DD} = +5V (MAX5235) V_{DD} = +3V (MAX5234), R_L = 5kΩ, C_L = 100pF, V_{REF} = +1.25V (MAX5234), V_{REF} = +2.5V (MAX5235), C_{REF} = 0.1µF ceramic ll 2.2µF electrolytic, both DACs on, V_{OUT} = full scale, T_A = +25°C, unless otherwise noted.)

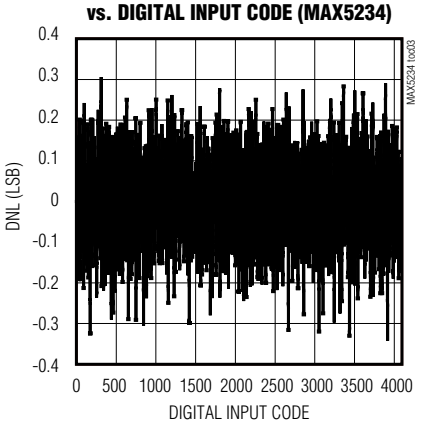
INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE (MAX5234)



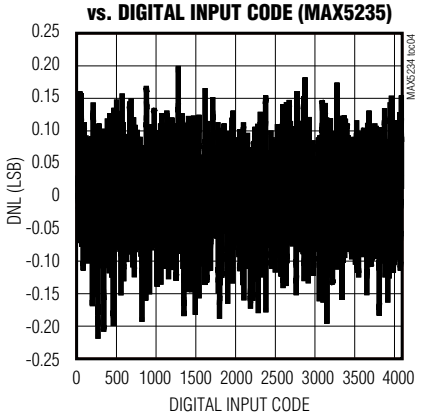
INTEGRAL NONLINEARITY vs. DIGITAL CODE (MAX5235)



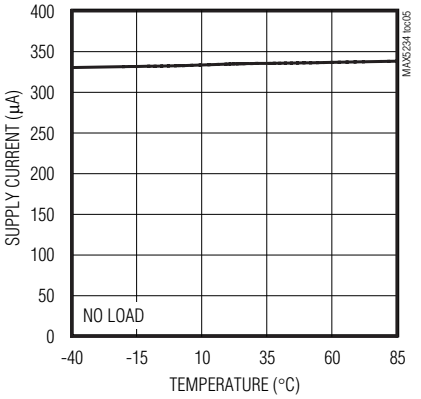
DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE (MAX5234)



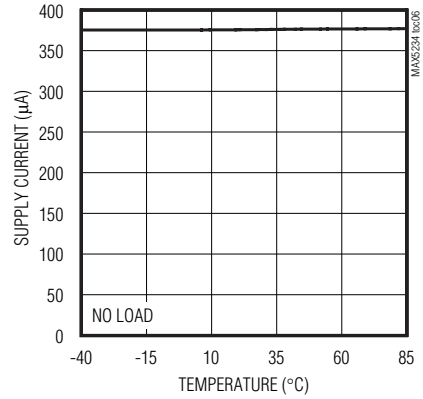
DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE (MAX5235)



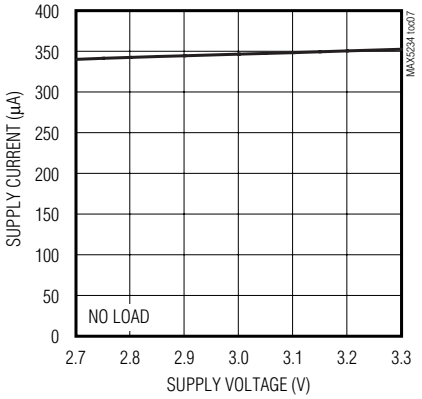
MAX5234 SUPPLY CURRENT vs. TEMPERATURE



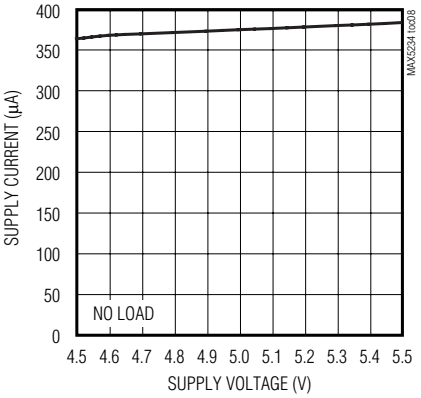
MAX5235 SUPPLY CURRENT vs. TEMPERATURE



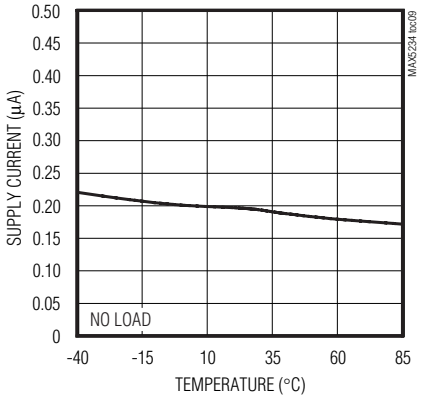
MAX5234 SUPPLY CURRENT vs. SUPPLY VOLTAGE



MAX5235 SUPPLY CURRENT vs. SUPPLY VOLTAGE



MAX5234 FULL POWER-DOWN SUPPLY CURRENT vs. TEMPERATURE

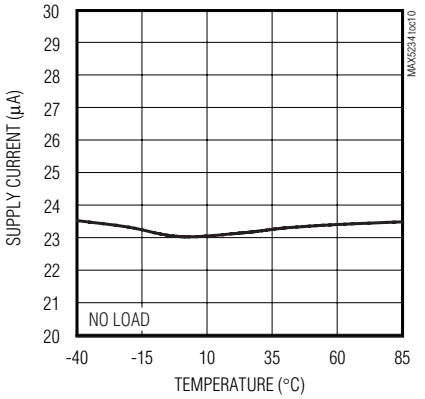


Single-Supply 3V/5V, Voltage-Output, Dual, Precision 12-Bit DACs

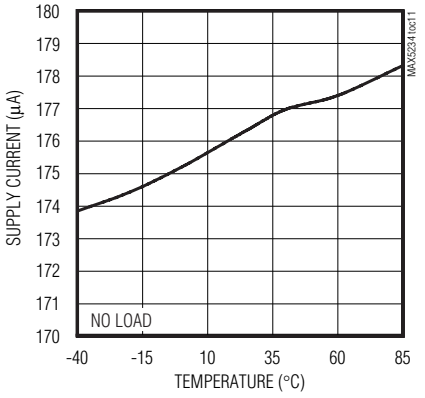
Typical Operating Characteristics (continued)

(V_{DD} = +5V (MAX5235) V_{DD} = +3V (MAX5234), R_L = 5kΩ, C_L = 100pF, V_{REF} = +1.25V (MAX5234), V_{REF} = +2.5V (MAX5235), C_{REF} = 0.1µF ceramic ll 2.2µF electrolytic, both DACs on, V_{OUT} = full scale, T_A = +25°C, unless otherwise noted.)

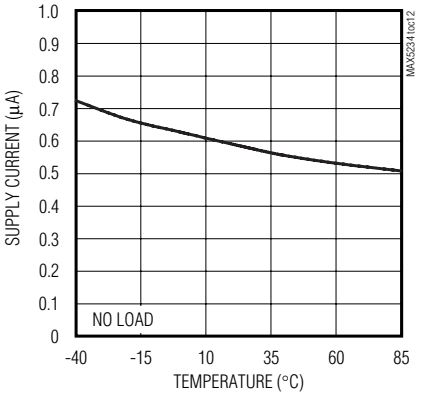
MAX5234
BOTH DACs SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



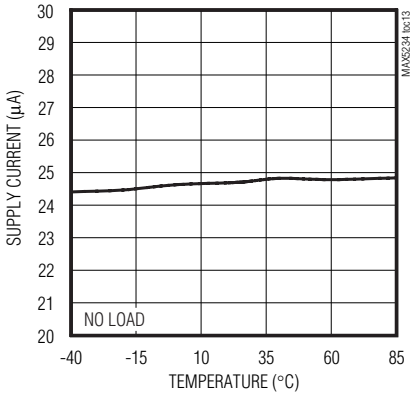
MAX5234
ONE DAC SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



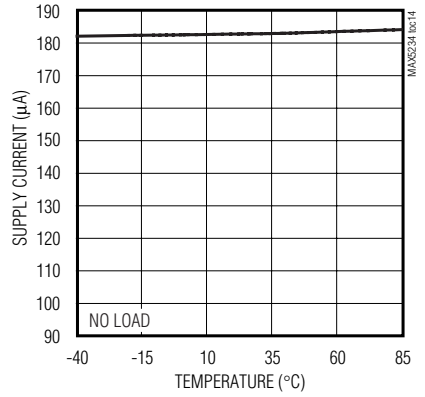
MAX5235
FULL POWER-DOWN SUPPLY CURRENT vs. TEMPERATURE



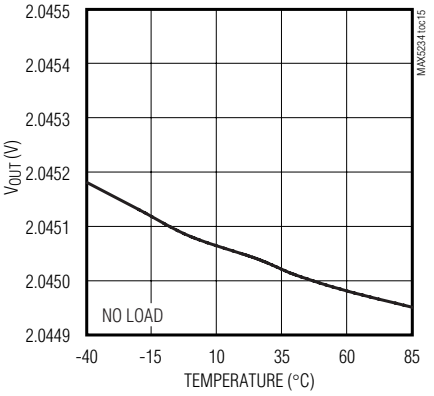
MAX5235
BOTH DACs SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



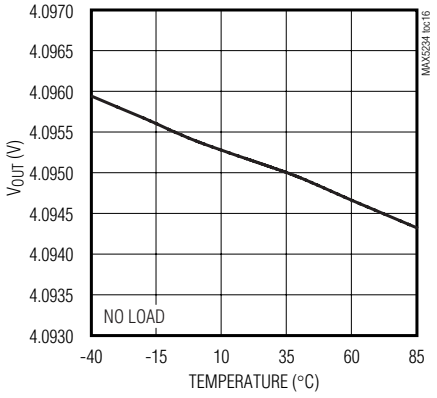
MAX5235
ONE DAC SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



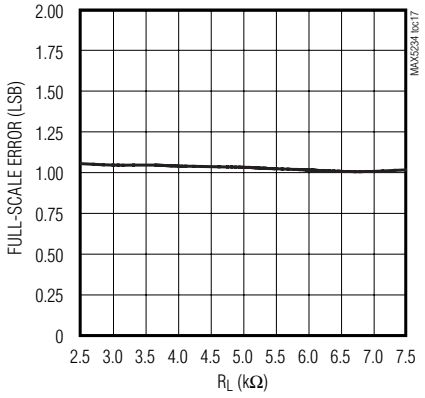
MAX5234
FULL-SCALE OUTPUT vs. TEMPERATURE



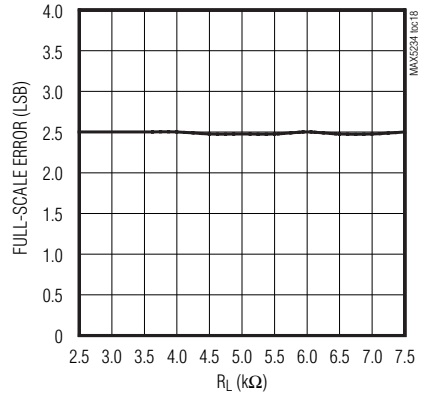
MAX5235
FULL-SCALE OUTPUT vs. TEMPERATURE



MAX5234
FULL-SCALE ERROR vs. RESISTIVE LOAD



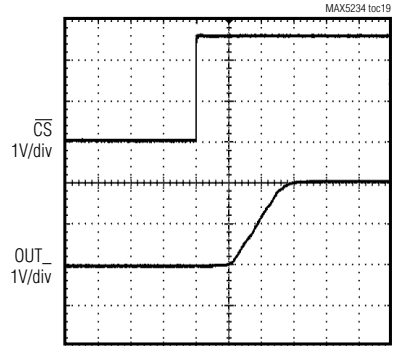
MAX5235
FULL-SCALE ERROR vs. RESISTIVE LOAD



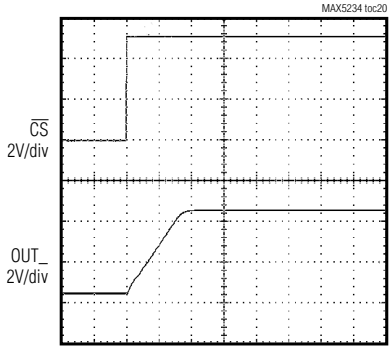
Typical Operating Characteristics (continued)

(V_{DD} = +5V (MAX5235) V_{DD} = +3V (MAX5234), R_L = 5kΩ, C_L = 100pF, V_{REF} = +1.25V (MAX5234), V_{REF} = +2.5V (MAX5235), C_{REF} = 0.1µF ceramic ll 2.2µF electrolytic, both DACs on, V_{OUT} = full scale, T_A = +25°C, unless otherwise noted.)

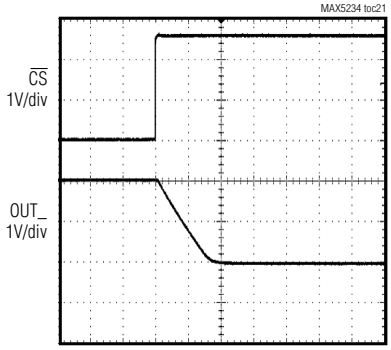
MAX5234
DYNAMIC RESPONSE RISE TIME



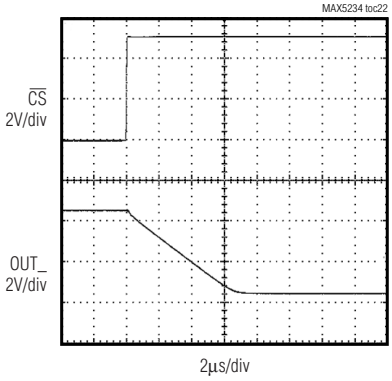
MAX5235
DYNAMIC RESPONSE RISE TIME



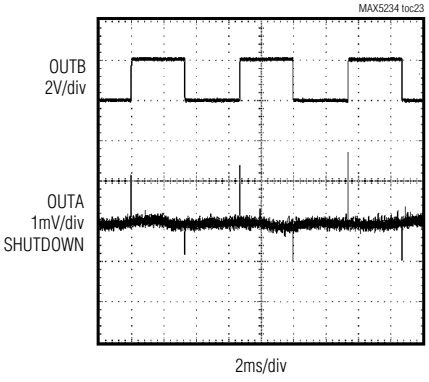
MAX5234
DYNAMIC RESPONSE FALL TIME



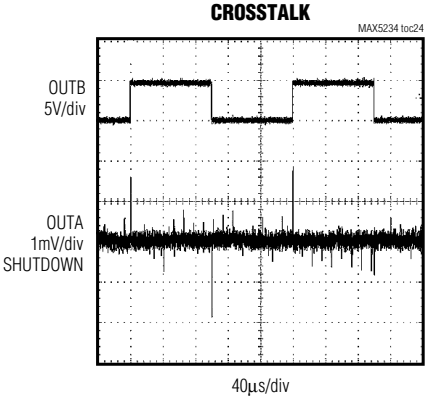
MAX5235
DYNAMIC RESPONSE FALL TIME



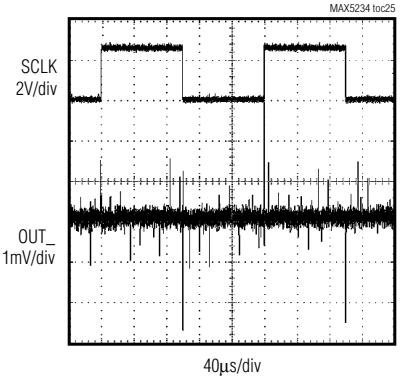
MAX5234
CROSSTALK



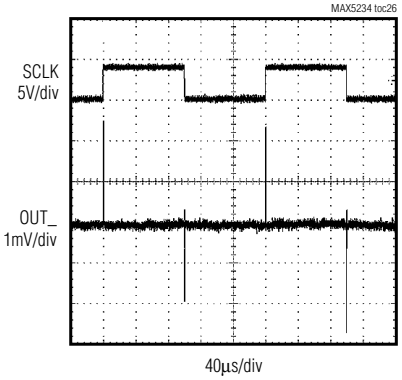
MAX5235
CROSSTALK



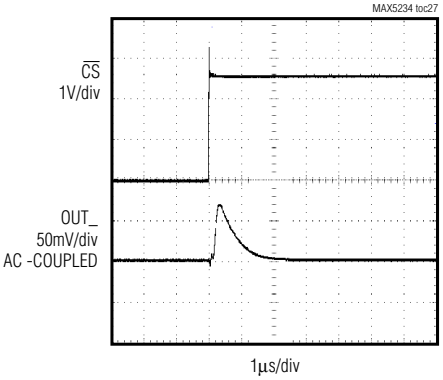
MAX5234
DIGITAL FEEDTHROUGH



MAX5235
DIGITAL FEEDTHROUGH



MAX5234
MAJOR-CARRY GLITCH

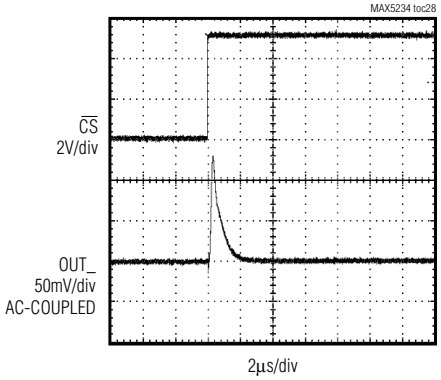


Single-Supply 3V/5V, Voltage-Output, Dual, Precision 12-Bit DACs

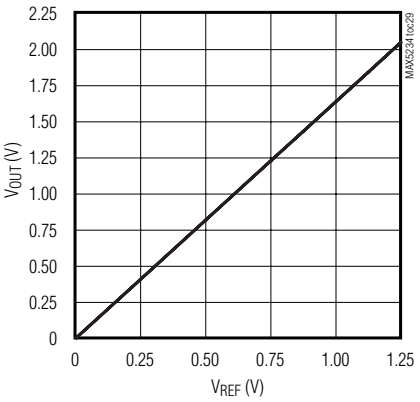
Typical Operating Characteristics (continued)

(V_{DD} = +5V (MAX5235) V_{DD} = +3V (MAX5234), R_L = 5kΩ, C_L = 100pF, V_{REF} = +1.25V (MAX5234), V_{REF} = +2.5V (MAX5235), C_{REF} = 0.1µF ceramic ll 2.2µF electrolytic, both DACs on, V_{OUT} = full scale, T_A = +25°C, unless otherwise noted.)

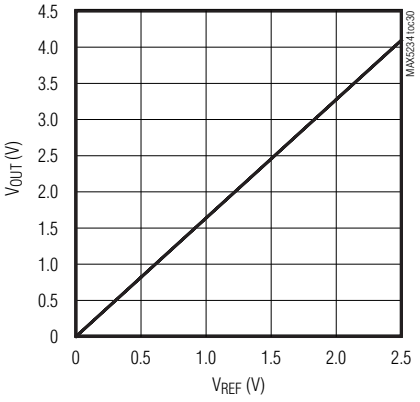
MAX5235
MAJOR-CARRY GLITCH



MAX5234
FULL-SCALE OUTPUT VOLTAGE
vs. REFERENCE VOLTAGE



MAX5235
FULL-SCALE OUTPUT VOLTAGE
vs. REFERENCE VOLTAGE



Pin Description

PIN	NAME	FUNCTION
1	OUTA	DAC A Output
2	REFA	Reference for DAC A
3	GND	Ground
4	$\overline{LDAC}$	Load DACs A and B
5	$\overline{CS}$	Chip Select Input
6	SCLK	Shift Register Serial Clock Input
7	DIN	Serial Data Input
8	V_{DD}	Positive Supply
9	REFB	Reference for DAC B
10	OUTB	DAC B Output

Detailed Description

The MAX5234/MAX5235 12-bit, voltage-output DACs are easily configured with a 3-wire SPI, QSPI, MICROWIRE serial interface. The devices include a 16-bit data-in/data-out shift register and have an input consisting of an input register and a DAC register. In addition, these devices employ precision trimmed internal resistors to produce a gain of 1.6384V/V, maximizing the output voltage swing, and a programmable shutdown output impedance of 1kΩ or 200kΩ. The full-scale output voltage is 4.095V for the MAX5235 and 2.0475V for the MAX5234. These devices produce a weighted output voltage proportional to the digital input code with an inverted rail-to-rail ladder network (Figure 3).

External Reference

The reference inputs accept both AC and DC values with a voltage range extending from 0.25V to 2.6V for the MAX5235 and 0.25V to 1.5V for the MAX5234. For proper operation **do not** exceed the input voltage range limits. Determine the output voltage using the following equation:

$$V_{OUT\_} = (V_{REF\_} \times NB / 4096) \times 1.6384V/V$$

where NB is the numeric value of the DACs binary input code (0 to 4095), $V_{REF\_}$ is the reference voltage, and 1.6384V/V is the gain of the internal output amplifier.

The code-dependent reference input impedance ranges from a minimum of 28kΩ to several GΩ at code 0. The code-dependent reference input capacitance is typically 23pF.

Output Amplifier

The output amplifiers have internal resistors that provide for a gain of 1.6384V/V. These trimmed resistors minimize gain error. The output amplifiers have a typical slew rate of 0.6V/µs and settle to 1/2LSB within 10µs (typ) with a load of 5kΩ in parallel with 100pF. Use the serial interface to set the shutdown output impedance of the amplifiers to 1kΩ or 200kΩ.

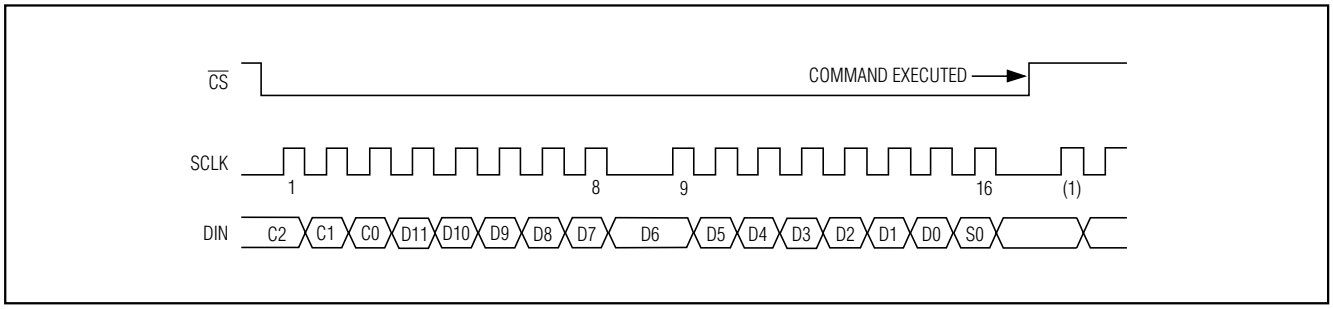


Figure 1. Serial Interface Timing

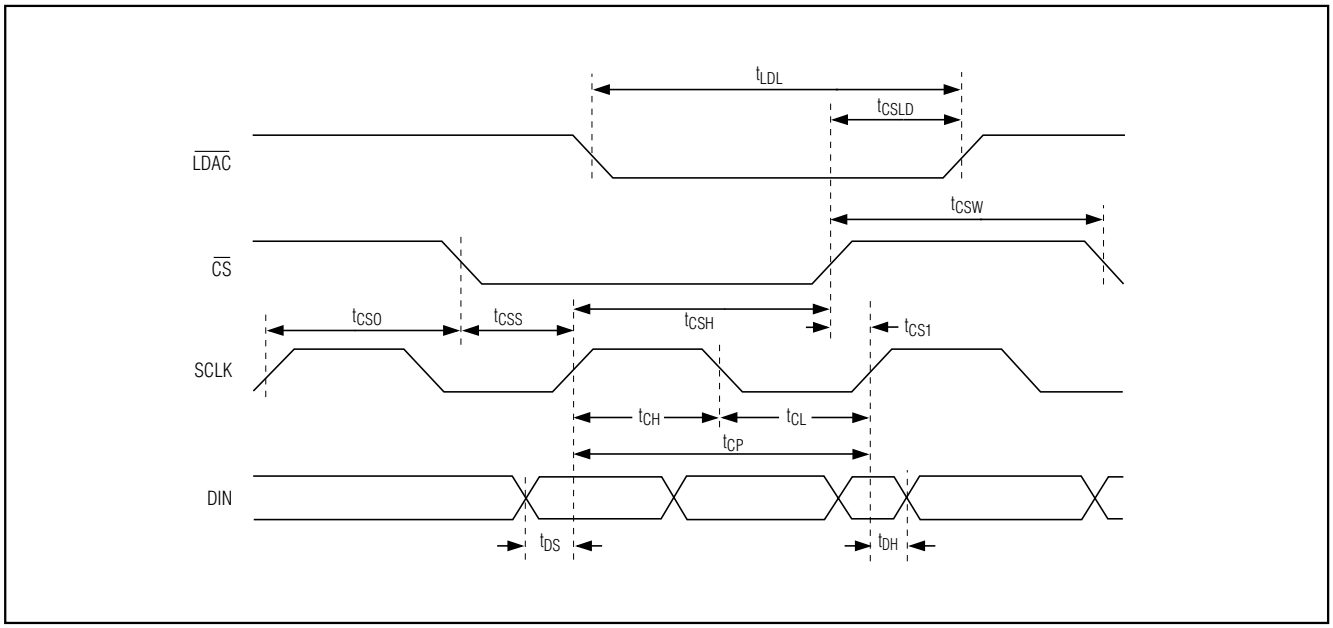


Figure 2. Detailed Serial Interface Timing

Serial Interface

The 3-wire serial interface (SPI, QSPI, and MICROWIRE compatible) used in the MAX5234/MAX5235 allows for complete control of DAC operations (Figures 4 and 5). Figures 1 and 2 show the timing for the serial interface. The serial word consists of 3 control bits followed by 12 data bits (MSB first) and 1 sub-bit as described in Tables 1, 2, and 3. When the 3 control bits are all zero or all 1, D11–D8 are used as additional control bits, allowing for greater DAC functionality.

The digital inputs allow any of the following: loading the input register(s) without updating the DAC register(s), updating the DAC register(s) from the input register(s), or updating the input and DAC register(s) simultaneously. The control bits and D11–D8 allow the DACs to operate independently.

Send the 16-bit data as one 16-bit word (QSPI) or two 8-bit packets (SPI and MICROWIRE), with $\overline{CS}$ low during this period. The control bits and D11–D8 determine which registers update and the state of the registers when exiting shutdown. The 3-bit control and D11–D8 determine the following:

- Registers to be updated
- Selection of the power-down modes

The general timing diagram of Figure 1 illustrates data acquisition. Driving $\overline{CS}$ low enables the device to receive data. Otherwise, the interface control circuitry is disabled. With $\overline{CS}$ low, data at DIN is clocked into the

Single-Supply 3V/5V, Voltage-Output, Dual, Precision 12-Bit DACs

Table 1. Serial Data Format

MSB <---------- 16 bits of serial data ----------> LSB		
3 Control Bits	MSB.....12 Data Bits.....LSB	Sub Bit
C2...C0	D11.....D0	S0

register on the rising edge of SCLK. As $\overline{CS}$ goes high, data is latched into the input and/or DAC registers, depending on the control bits and D11–D8. The maximum clock frequency guaranteed for proper operation is 13.5MHz. Figure 2 depicts a more detailed timing diagram of the serial interface.

Power-Down and Shutdown Modes

As described in Tables 2 and 3, several serial interface commands put one or both of the DACs into shutdown mode. Shutdown modes are completely independent for each DAC. In shutdown, the amplifier output becomes high impedance, and OUT_ terminates to GND through the 200kΩ (typ) gain resistors. Optionally (see Tables 2 and 3), OUT_ can have a termination of 1kΩ to GND.

Full power-down mode shuts down the main bias generator and both DACs. The shutdown impedance of the DAC outputs can still be controlled independently, as described in Tables 2 and 3.

A serial interface command exits shutdown mode and updates a DAC register. Each DAC can exit shutdown at the same time or independently (see Tables 2 and 3). For example, if both DACs are shut down, updating the DAC A register causes DAC A to power up, while DAC B remains shut down. In full power-down mode, powering up either DAC also powers up the main bias generator. To change from full power-down to both DACs shutdown mode requires the waking of at least one DAC between states.

When powering up the MAX5234/MAX5235 (powering V_{DD}), allow 60µs (MAX5234) or 70µs (MAX5235) for the output to stabilize. When exiting full power-down mode, allow 60µs max (MAX5234) or 70µs max (MAX5235) for the output to stabilize. When exiting DAC shutdown mode, allow 50µs max (MAX5234) or 60µs max (MAX5235) for the output to stablize.

Load DAC Input ($\overline{LDAC}$)

Asserting $\overline{LDAC}$ asynchronously loads the DAC registers from their corresponding input registers (DACs that are shut down remain shut down). The $\overline{LDAC}$ input is totally asynchronous and does not require any activity on $\overline{CS}$, SCLK, or DIN in order to take effect. If $\overline{LDAC}$ is asserted coincident with a rising edge of $\overline{CS}$, which executes a serial command modifying the value of either DAC input register, then $\overline{LDAC}$ must remain asserted for at least 30ns following the $\overline{CS}$ rising edge. This requirement applies only for serial commands that modify the value of the DAC input registers.

Applications Information

Definitions

Integral Nonlinearity (INL)

Integral nonlinearity (Figure 6a) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit (closest approximation to the actual transfer curve) or a line drawn between the endpoints of the transfer function, once offset and gain errors have been nullified. For a DAC, the deviations are measured at every single step.

Differential Nonlinearity (DNL)

Differential nonlinearity (Figure 6b) is the difference between an actual step height and the ideal value of 1LSB. If the magnitude of the DNL is less than 1LSB, the DAC guarantees no missing codes and is monotonic.

Offset Error

The offset error (Figure 6c) is the difference between the ideal and the actual offset point. For a DAC, the offset point is the step value when the digital input is zero. This error affects all codes by the same amount and can usually be compensated for by trimming.

Gain Error

Gain error (Figure 6d) is the difference between the ideal and the actual full-scale output voltage on the transfer curve, after nullifying the offset error. This error alters the slope of the transfer function and corresponds to the same percentage error in each step.

Settling Time

The settling time is the amount of time required from the start of a transition until the DAC output settles to its new output value within the converter's specified accuracy.

Digital Feedthrough

Digital feedthrough is noise generated on the DAC's output when any digital input transitions. Proper board layout and grounding significantly reduces this noise, but there is always some feedthrough caused by the DAC itself.

Unipolar Output

Figure 7 shows the MAX5234/MAX5235 configured for unipolar, rail-to-rail operation with a gain of 1.6384V/V. The MAX5235 produces a 0 to 4.095V output with 2.5V reference while the MAX5234 produces a range of 0 to

Table 2. Serial Interface Programming Commands

16-BIT SERIAL WORD					FUNCTION
C2	C1	C0	D11.....D0	S0*	
0	0	1	12-bit DAC data	0	Load input register A; DAC registers are unchanged.
0	1	0	12-bit DAC data	0	Load input register A; all DAC registers are updated.
0	1	1	12-bit DAC data	0	Load all DAC registers from the shift register (start up both DACs with new data, and load the input registers).
1	0	0	X X X X X X X X X X X X	0	Update both DAC registers from their respective input registers (start up both DACs with data previously stored in the input registers).
1	0	1	12-bit DAC data	0	Load input register B; DAC registers are unchanged.
1	1	0	12-bit DAC data	0	Load input register B; all DAC registers are updated.
1	1	1	P1A P1B X X X X X X X X X X	0	Power down both DACs respectively according to bits P1A and P1B (see Table 3). Internal bias remains active.
0	0	0	0 0 1 X X X X X X X X X	0	Update DAC register A from input register A (start up DAC A with data previously stored in input register A).
0	0	0	0 1 1 P1A P1B X X X X X X	0	Full power-down. Power down the main bias generator and power down both DACs respectively according to bits P1A and P1B (see Table 3).
0	0	0	1 0 1 X X X X X X X X X	0	Update DAC register B from input register B (start up DAC B with data previously stored in input register B).
0	0	0	1 1 0 P1A X X X X X X X X	0	Power down DAC A according to bit P1A (see Table 3).
0	0	0	1 1 1 P1B X X X X X X X X	0	Power down DAC B according to bit P1B (see Table 3).

X = Don't care.

** = S0 must be zero for proper operation.*

2.0475V output with a 1.25V reference. Table 4 lists the unipolar output codes.

Bipolar Output

The MAX5234/MAX5235 can be configured for a bipolar output, as shown in Figure 8. The output voltage is given by the equation:

$$V_{OUT} = V_{REF} [((1.6348 \times NB) / 4096) - 1]$$

where NB represents the numeric value of the DAC's binary input code. Table 5 shows digital codes and the corresponding output voltage for Figure 8's circuit.

Using an AC Reference

In applications where the reference has an AC signal component, the MAX5234/MAX5235 have multiplying capabilities within the reference input voltage range specifications. Figure 9 shows a technique for applying a sinusoidal input to REF_, where the AC signal is offset before being applied to the reference input.

Table 3. P1 Shutdown Modes

P1(A/B)	SHUTDOWN MODE
0	Shut down with internal 1kΩ load to GND
1	Shut down with internal 200kΩ load to GND

Digital Calibration and Threshold Selection

Figure 10 shows the MAX5234/MAX5235 in a digital calibration application. With a bright light value applied to the photodiode (on), the DAC is digitally ramped until it trips the comparator. The microprocessor (µP) stores this "high" calibration value. Repeat the process with a dim light (off) to obtain the dark current calibration. The µP then programs the DAC to set an output voltage at the midpoint of the two calibrated values. Applications include tachometers, motion sensing, automatic readers, and liquid clarity analysis.

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Table 4. Unipolar Code Table (Gain = 1.6384)

DAC CONTENTS MSB LSB	ANALOG OUTPUT
1111 1111 1 111 (0)	$+V_{REF}\left(\frac{4095}{4096}\right)\times 1.6384$
1000 0000 0 001 (0)	$+V_{REF}\left(\frac{2049}{4096}\right)\times 1.6384$
1000 0000 0 000 (0)	$+V_{REF}\left(\frac{2048}{4096}\right)\times 1.6384 = V_{REF}$
0111 1111 1 111 (0)	$+V_{REF}\left(\frac{2047}{4096}\right)\times 1.6384$
0000 0000 0001 (0)	$+V_{REF}\left(\frac{1}{4096}\right)\times 1.6384$
0000 0000 0 000 (0)	0V

Note: *() are for the sub-bit.*

Table 5. Bipolar Code Table

DAC CONTENTS MSB LSB	ANALOG OUTPUT
1111 1111 1 111 (0)	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0 001 (0)	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0 000 (0)	0V
0111 1111 111 (0)	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 001 (0)	$-V_{REF}\left(\frac{2047}{2048}\right)$
0000 0000 000 (0)	$-V_{REF}\left(\frac{2048}{2048}\right) = -V_{REF}$

Note: *() are for the sub-bit.*

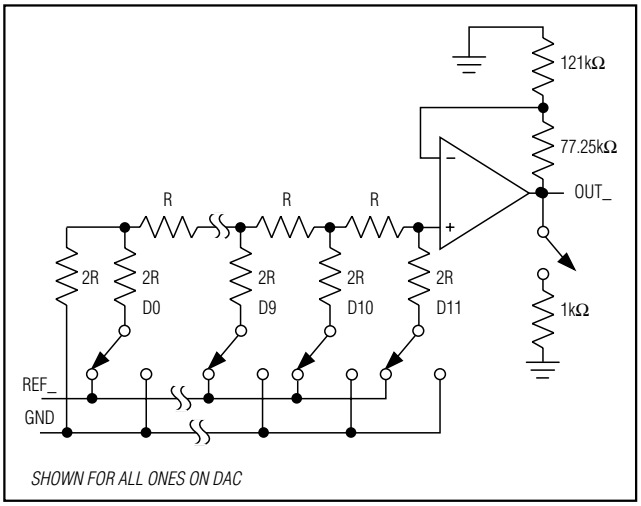

Figure 3. Simplified DAC Circuit Diagram

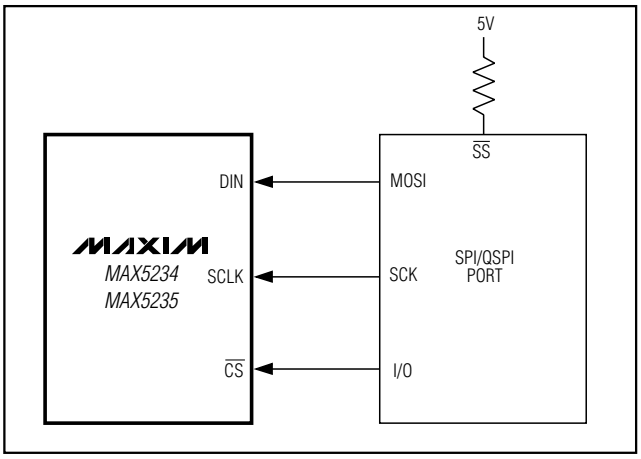

Figure 4. SPI/QSPI Interface Connections

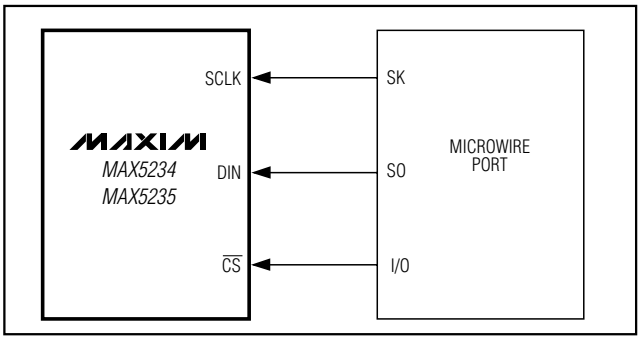

Figure 5. Connections for MICROWIRE

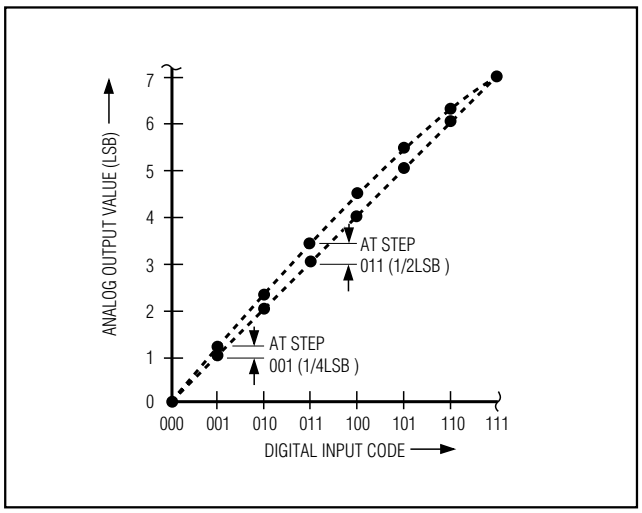

Figure 6a. Integral Nonlinearity

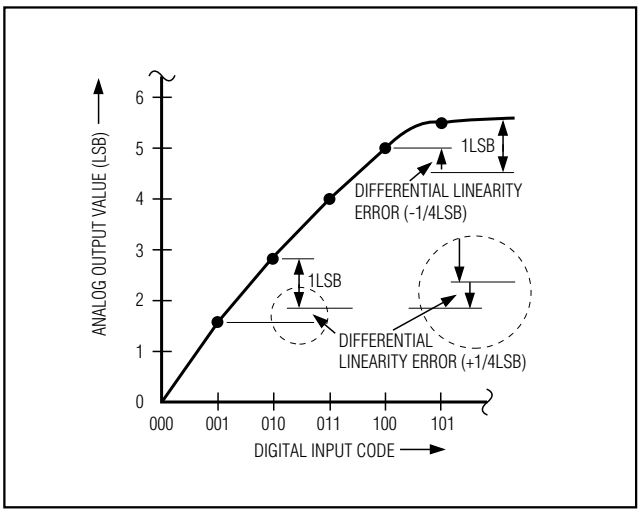

Figure 6b. Differential Nonlinearity

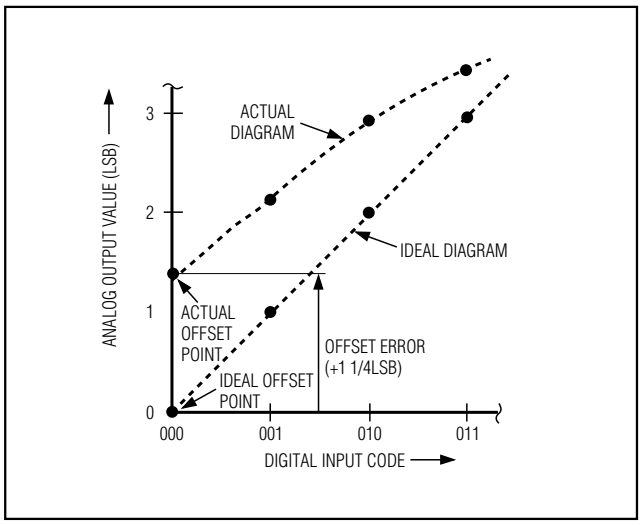

Figure 6c. Offset Error

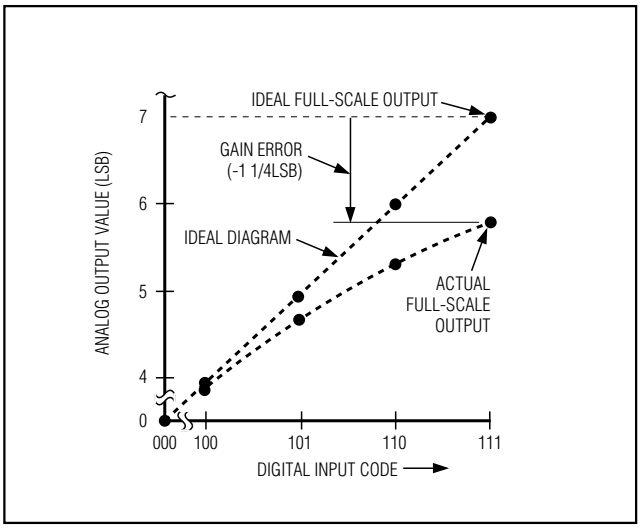

Figure 6d. Gain Error

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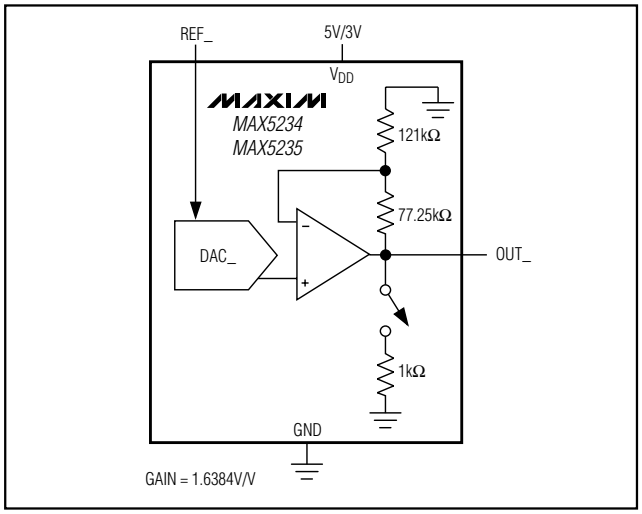


Figure 7. Unipolar Output Circuit (Rail-to-Rail)

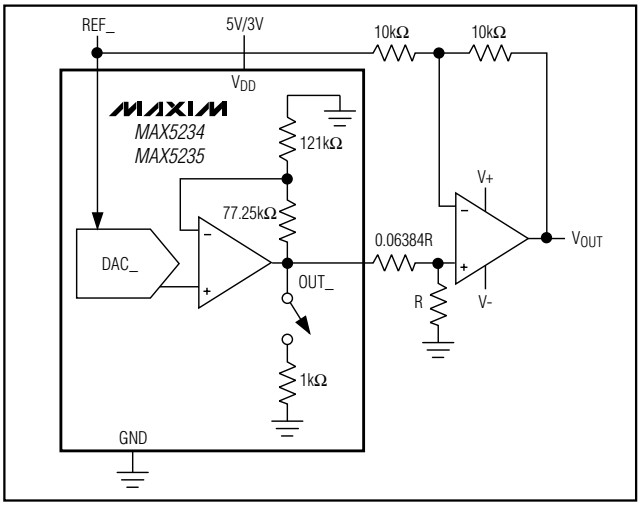


Figure 8. Bipolar Output Circuit

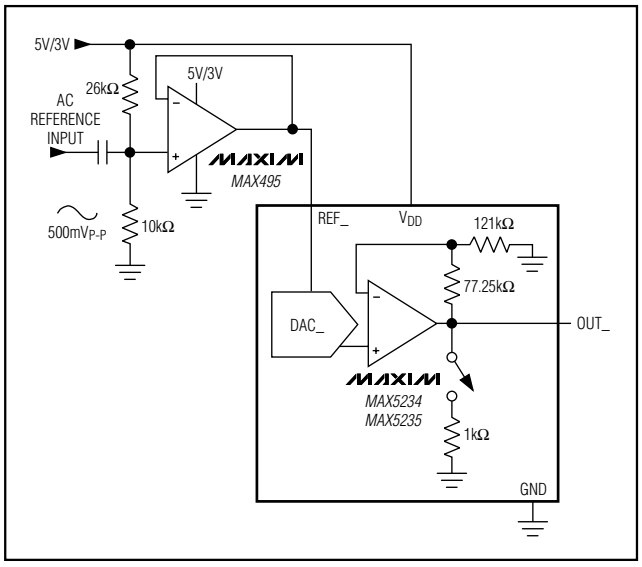


Figure 9. External Reference with AC Components

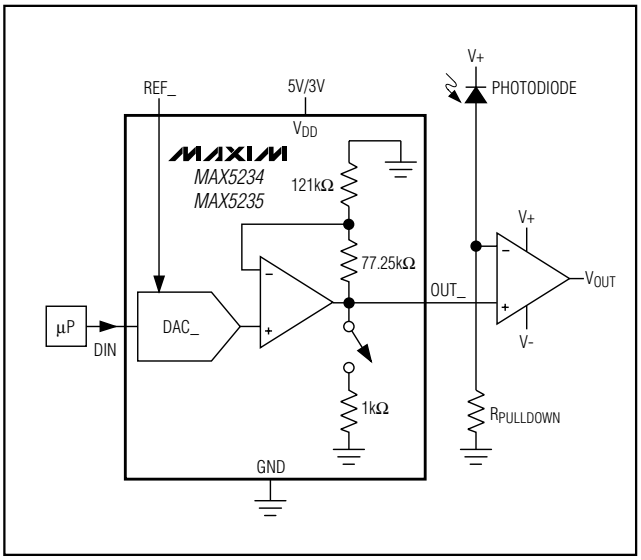


Figure 10. Digital Calibration

Digital Control of Gain and Offset

The two DACs can be used to control the offset and gain for curve-fitting nonlinear functions, such as transducer linearization or analog compression/expansion applications. The input signal is used as the reference for the gain-adjust DAC, whose output is summed with the output from the offset-adjust DAC. The relative weight of each DAC output is adjusted by R1, R2, R3, and R4 (Figure 11).

Sharing a Common DIN Line

Several MAX5234/MAX5235 may share one common DIN signal line (Figure 12). In this configuration, the data bus is common to all devices; data is not shifted through a daisy-chain. The SCLK and DIN lines are shared by all devices, but each IC needs its own dedicated $\overline{CS}$ line.

Power-Supply Considerations

On power-up, the input and DAC registers clear (set to zero code). Bypass the power supply with a 4.7µF

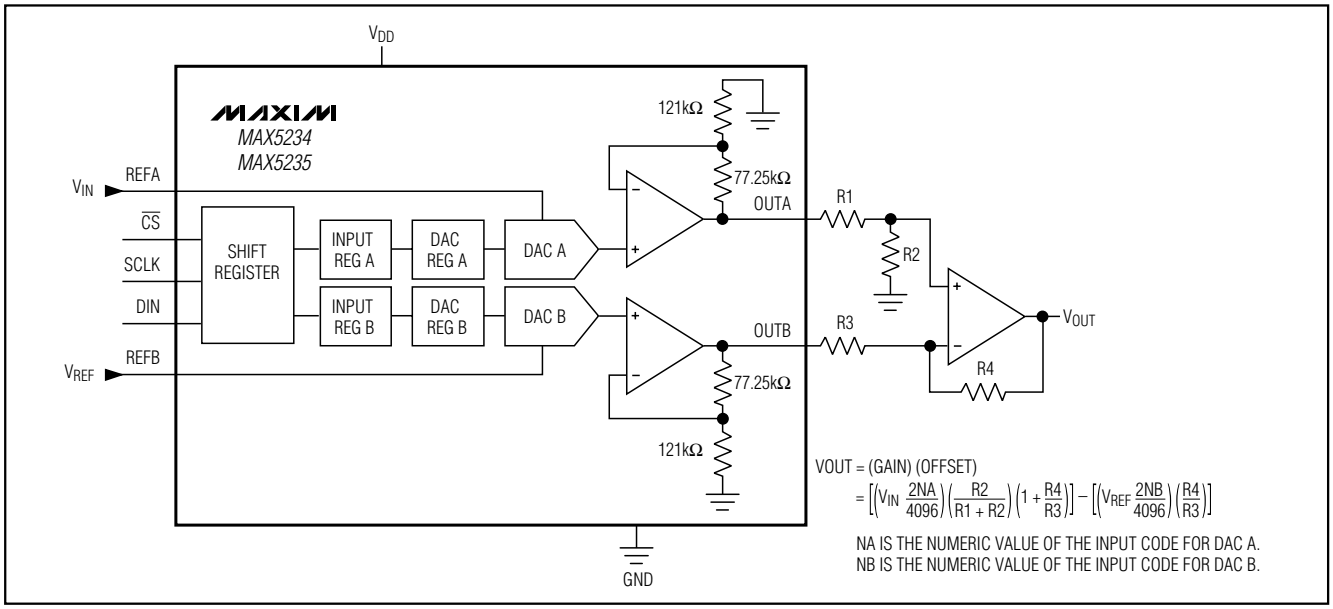


Figure 11. Digital Control of Gain and Offset

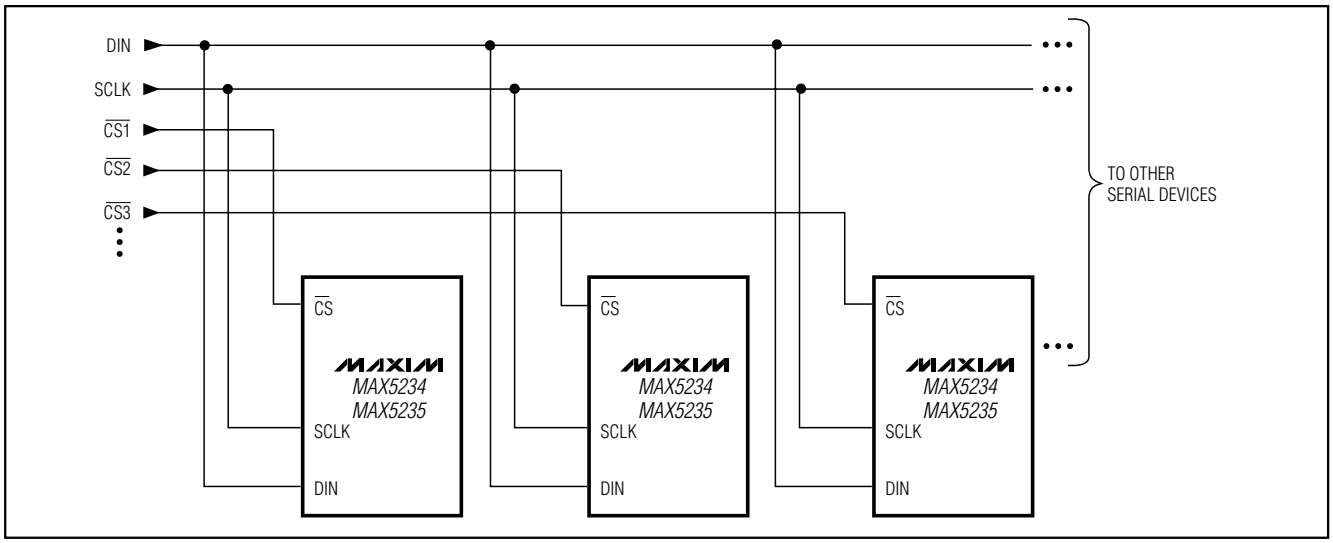


Figure 12. Multiple MAX5234/MAX5235 Sharing a Common DIN Line

capacitor in parallel with a 0.1µF capacitor to GND. Minimize lead lengths to reduce lead inductance.

Grounding and Layout Considerations

Digital and AC transient signals on GND can create noise at the output. Connect GND to the highest quality ground available. Use proper grounding techniques, such as a multilayer board with a low-inductance ground plane or star connect all ground return paths back to the MAX5234/MAX5235 GND. Carefully lay out the traces between channels to reduce AC cross-coupling and crosstalk. Wire-wrapped boards and sockets are not recommended. If noise becomes an issue, shielding may be required.

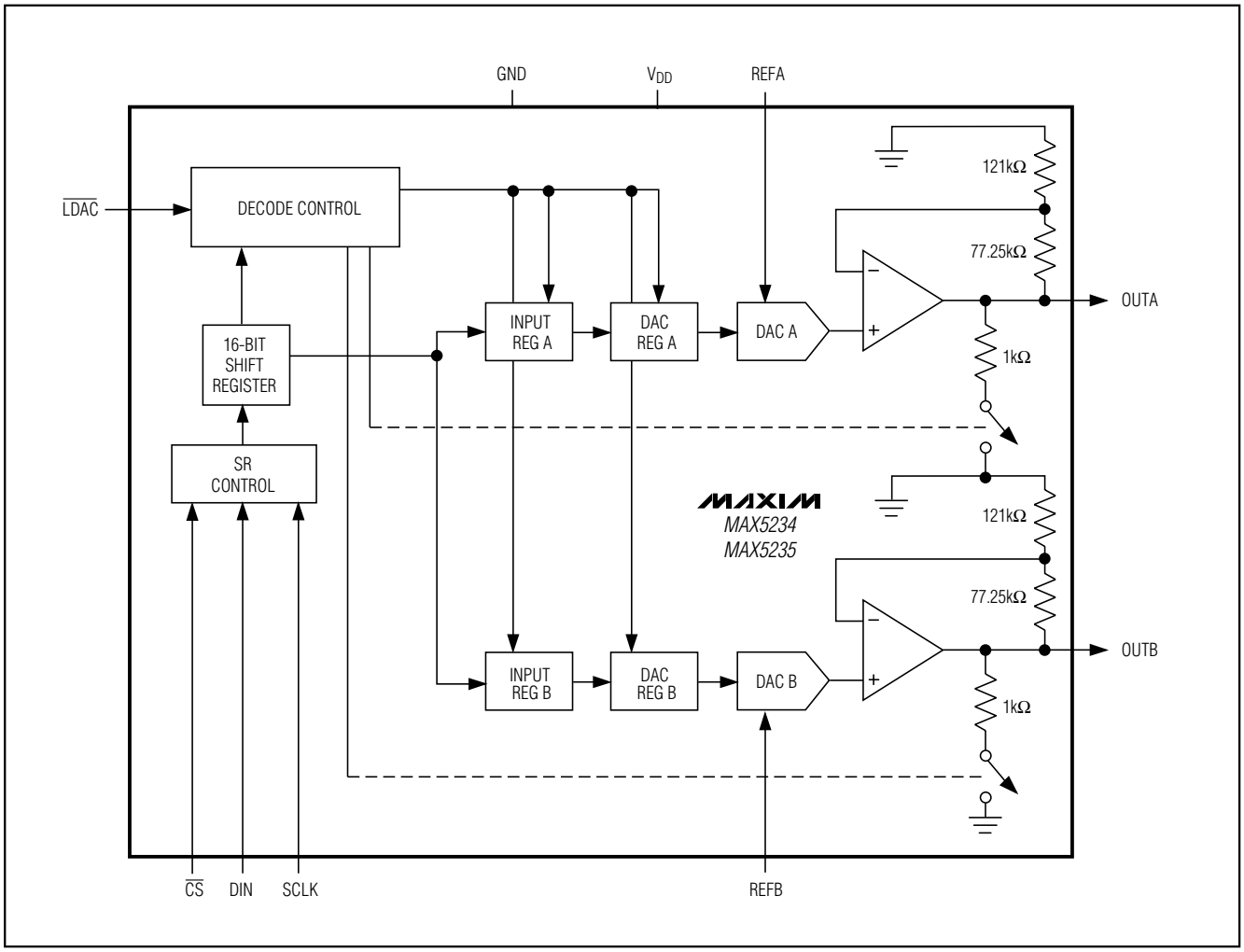
Chip Information

TRANSISTOR COUNT: 4184

PROCESS: BiCMOS

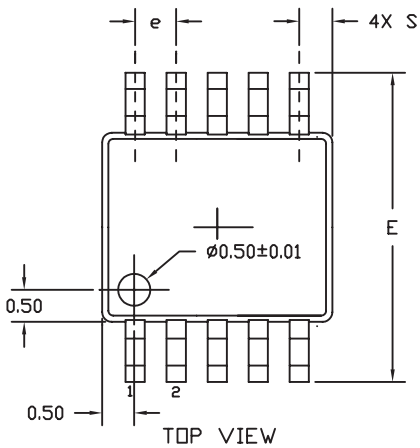
Single-Supply 3V/5V, Voltage-Output, Dual, Precision 12-Bit DACs

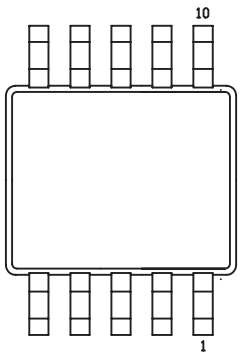
Functional Diagram



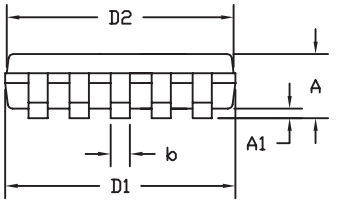
Package Information

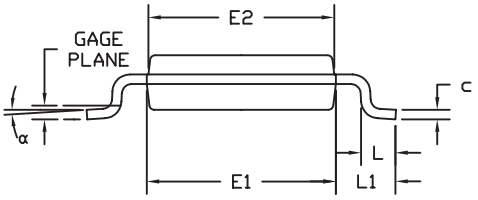
10LUMAX.EPS





	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.037	0.043	0.94	1.10
A1	0.002	0.006	0.05	0.15
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
E	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		.498 REF	
α	0°	6°	0°	6°





NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO187.

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 10L uMAX

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0061	H	1/1