OKI semiconductor

MSM5839B

DOT MATRIX LCD 40 DOT SEGMENT DRIVER

GENERAL DESCRIPTION

The OKI MSM5839BGS is a dot matrix LCD's segment driver LSI which is fabricated by low power CMOS metal gate technology. This LSI consists of 40-bit shift register (two 20-bit shift registers), 40-bit latch (two 20-bit latches), 40-bit level shifter and 40-bit 4-level driver.

It converts serial data, which is received from LCD controller LSI, to parallel data and outputs LCD driving waveform to the LCD panel.

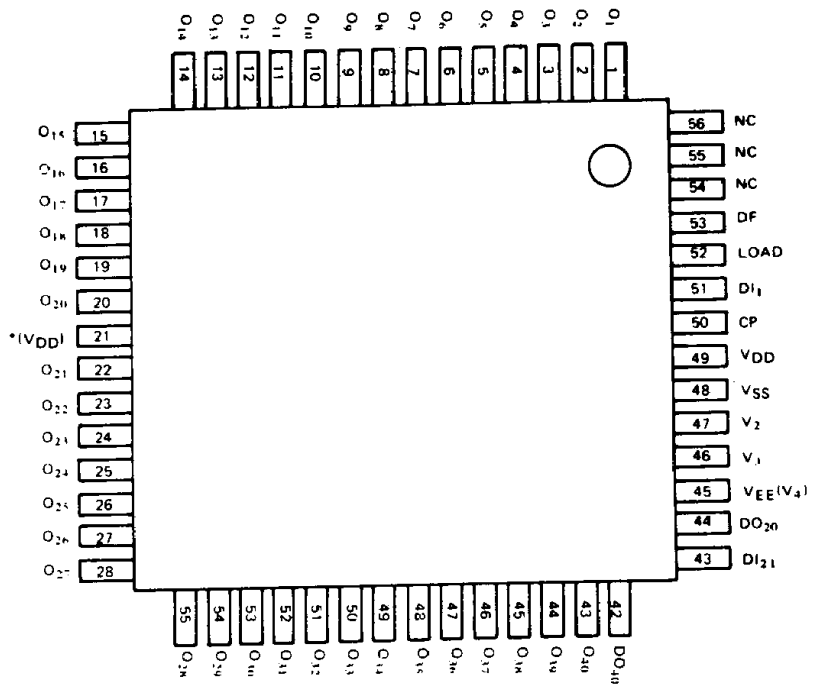
This LSI can drive a variety of LCD panel because the bias voltage, which determines the LCD driving voltage, can be optionally supplied from the external source.

FEATURES

- Supply voltage: 4.5 ~ 5.5V
- LCD driving voltage: 8 ~ 18V
- Applicable LCD duty: 1/16 ~ 1/128
- Bias voltage can be supplied externally
- 56 pin (s) plastic QFP (QFP56-P-910-K)
- 56 pin (s) plastic QFP (QFP56-P-910-L)
- 56 pin (s) -V plastic QFP (QFP56-P-910-VK)

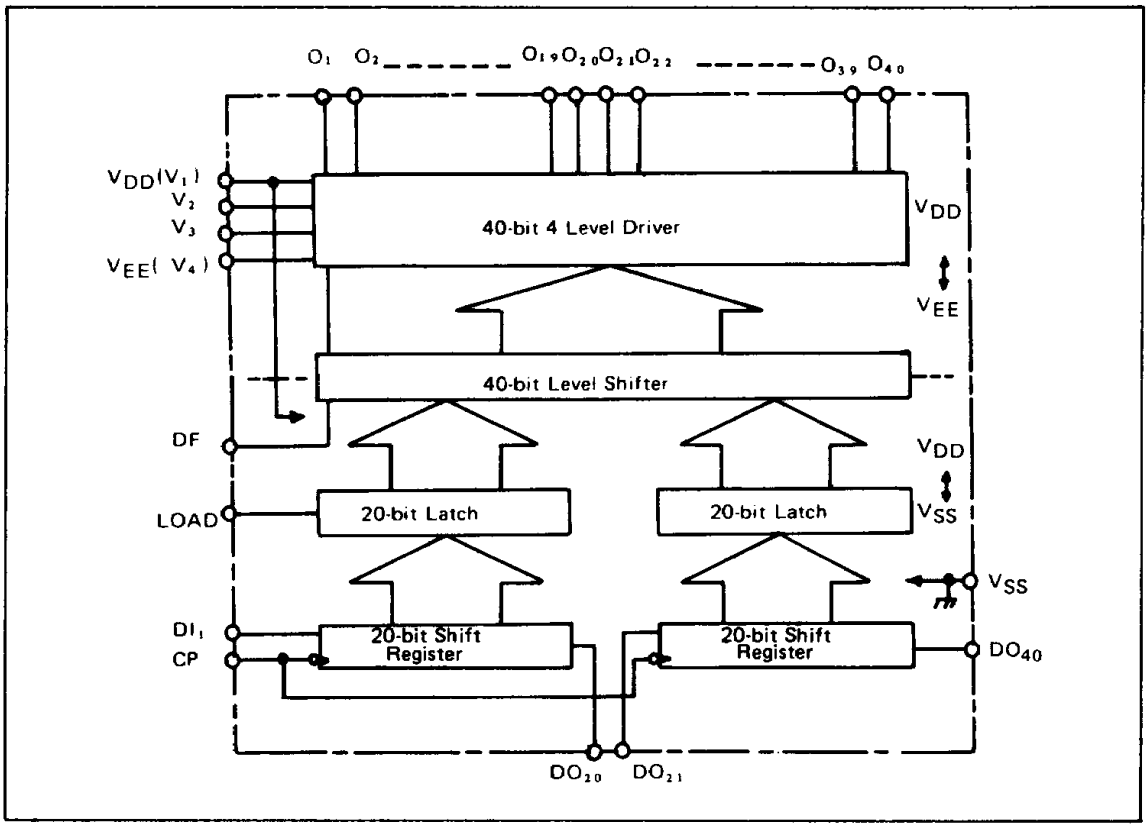
PIN CONFIGURATION

(Top view) 56 pin (s) plastic QFP



*This pin is internally connected with V_{DD}, so it must not be connected to other signals. It is also prohibited to use the 21 pin as a V_{DD} independently. This pin may be used as a line reinforcing V_{DD}.

BLOCK DIAGRAM

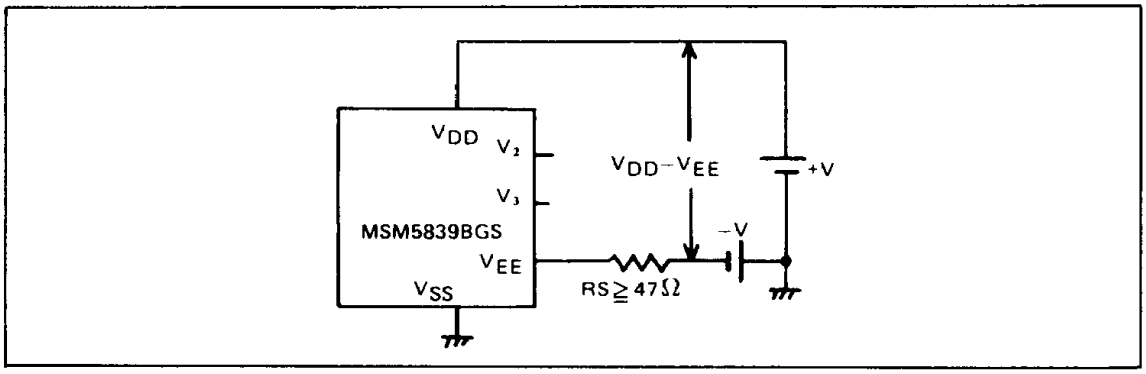


ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Limits	Unit
Supply voltage (1)	V_{DD}	T_a = 25°C	−0.3 ~ 6	V
Supply voltage (2)	$V_{DD} - V_{EE}$*1	T_a = 25°C	0 ~ 18	V
	$V_{DD} - V_{EE}$*2	T_a = 25°C	0 ~ 18	V
Input voltage	V_I	T_a = 25°C	−0.3 ~ V_{DD} + 0.3	V
Storage temperature	T_{stg}	–	−55 ~ +150	°C

*1 : $V_{DD} > V_2 > V_3 > V_{EE}$

*2 : When a series resistance of more than 47Ω is connected as shown below.

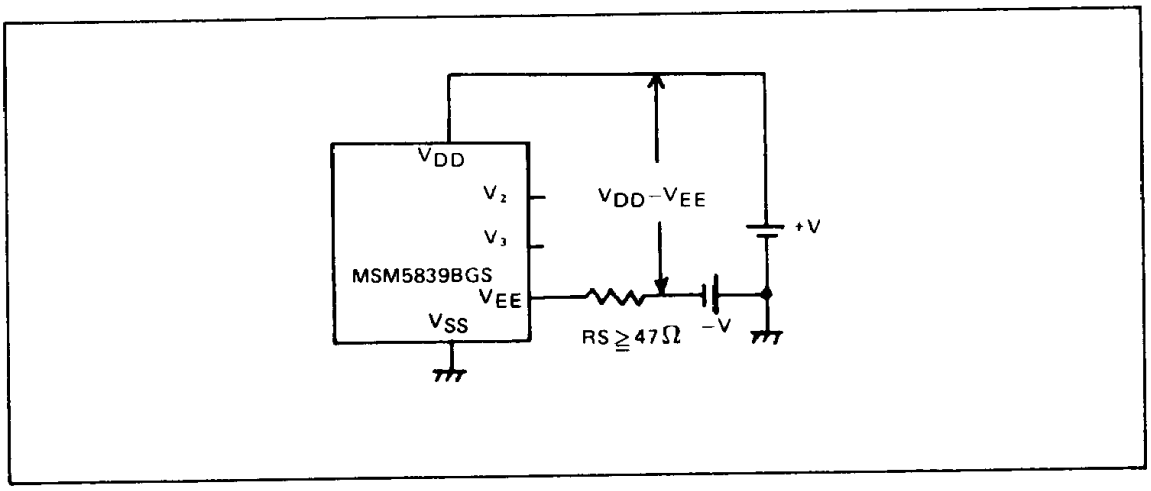


OPERATING RANGE

Parameter	Symbol	Condition	Limit	Unit
Supply voltage (1)	V_{DD}	–	4.5 ~ 5.5	V
Supply voltage (2)	$V_{DD} - V_{EE}$*1	–	8 ~ 16	V
	$V_{DD} - V_{EE}$*1*2	–	8 ~ 18	V
Operating temperature	T_{op}	–	−20 ~ + 85	°C

*1 : $V_{DD} > V_2 > V_3 > V_{EE}$

*2 : When a series resistance of more than 47Ω is connected as shown below.



D.C. CHARACTERISTICS

(V_{DD} = 5V ± 10%, T_a = −20 ~ +85°C)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
"H" input voltage	V_{IH}*1	—	0.8V_{DD}	–	–	V
"L" input voltage	V_{IL}*1	—	–	–	0.2V_{DD}	V
"H" input current	I_{IH}*1	$V_{IH} = V_{DD}$	–	–	1	μA
"L" input current	I_{IL}*1	V_{IL} = 0V	–	–	−1	μA
"H" output voltage	V_{OH}*2	I_0 = −0.4mA	$V_{DD} - 0.4$	–	–	V
"L" output voltage	V_{OL}*2	I_0 = 0.4mA	–	–	0.4	V
ON resistance	R_{ON}*4	$V_{DD} = V_{EE}$ = 10V $\lvert V_N - V_O \rvert$ = 0.25V*3	–	3.5	7	kΩ
Current consumption	I_{DD}	CP = DC $V_{DD} - V_{EE}$ = 18V No load	–	–	100	μA

*1 : LOAD, CP, DI_1, DI_{21}, DF

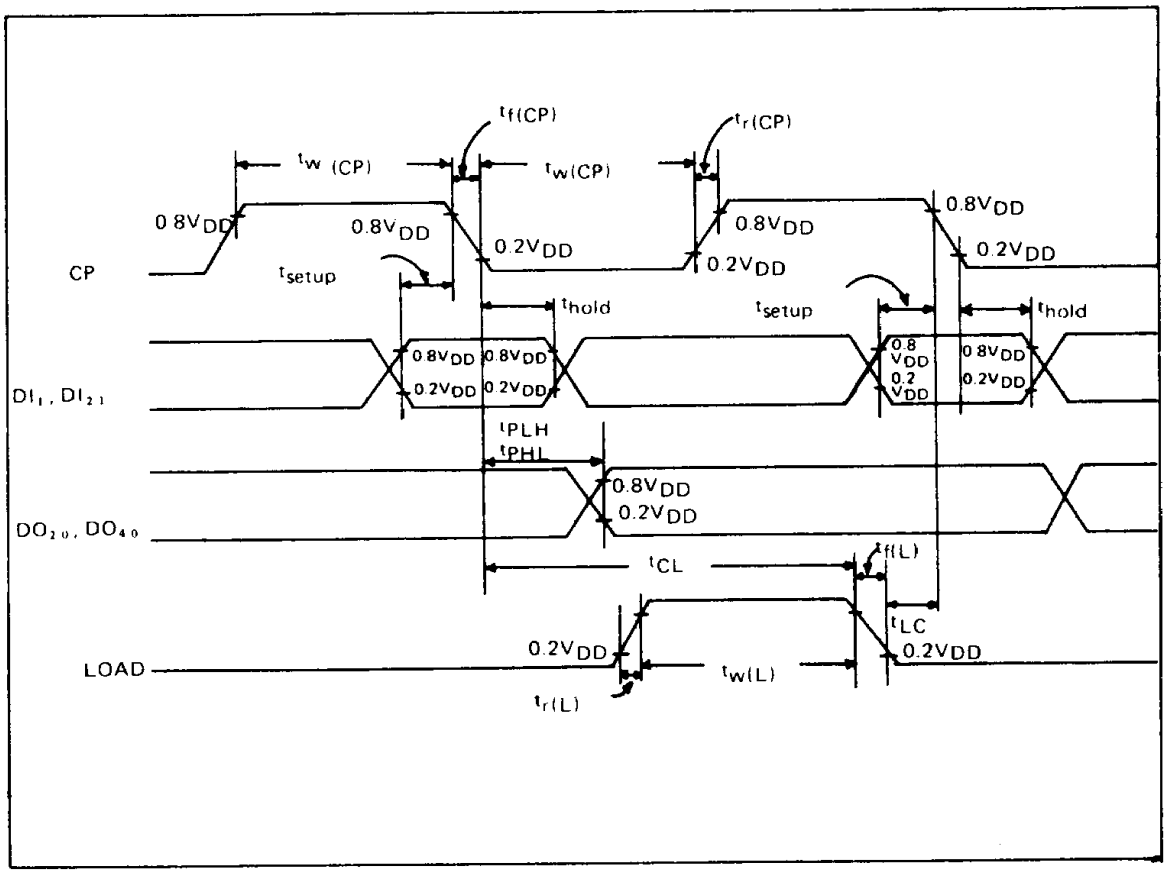
*2 : DO_{20}, DO_{40}

*3 : VN = V_{DD} ~ V_{EE}, $V_3 = \frac{8}{9}(V_{DD} - V_{EE})$, $V_2 = \frac{1}{9}(V_{DD} - V_{EE})$

*4 : Applicable to O_1 ~ O_{40}

SWITCHING CHARACTERISTICS

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
"H", "L" propagation delay time	t_{PLH} t_{PHL}	—	–	–	250	ns
Max. clock frequency	f_{CP}	DUTY = 50%	3.3	–	–	MHz
Clock pulse width	$t_{W(CP)}$	—	125	–	–	ns
LOAD pulse width	$t_{W(L)}$	—	125	–	–	ns
Data setup time DI → CP	t_{setup}	—	50	–	–	ns
CP → LOAD time	t_{CL}	—	250	–	–	ns
LOAD → CP time	t_{LC}	—	0	–	–	ns
DATA hold time DI → CP	t_{hold}	—	50	–	–	ns
CP Rising/Falling time	$t_{r(CP)}$ $t_{f(CP)}$	—	–	–	50	ns
LOAD Rising/Falling time	$t_{r(L)}$ $t_{f(L)}$	—	–	–	1	μs



PIN DESCRIPTION

- **DI_1**
  The 1st ~ 20th data from the LCD controller LSI is input to shift register from DI_1. (Positive logic)

- **CP**
  Clock pulse input pin for the two 20-bit shift register. The data is shifted in the two 20-bit shift register at the falling edge of the clock pulse. A data setup time (t_{setup}) and data hold time (t_{hold}) are required each between DI_1, DI_{21} and CP.

- **DO_{20}**
  The 20th bit of shift register contents is output from DO_{20} synchronized with the clock pulse. By connecting DO_{20} with DI_{21}, two 20-bit shift registers are connected and becomes 40-bit shift register.

- **DI_{21}**
  The 21st ~ 40th data from the LCD controller LSI is input to shift register from DI_{21}. By connecting DO_{20} with DI_{21}, two 20-bit shift registers are connected and becomes 40-bit shift register.

- **DO_{40}**
  The 40th bit of shift register contents is output from DO_{40} synchronized with the clock pulse. By connecting DO_{40} with next MSM5839BGS's DI_1, this LSI is applicable to a wide screen LCD. Refer to the sample application circuit.

- **DF**
  Alternate signal input pin for LCD driving waveform.

- **$V_{DD}(V_1)$, V_{SS}**
  Supply voltage pin. V_{DD} should be 4.5 ~ 5.5V.
  V_{SS} is a ground pin (V_{SS} = 0V).

- **V_1 (V_{DD}), V_2, V_3, V_{EE} (V_4)**
  Bias supply voltage pin to drive the LCD. Bias voltage divided by the resistance is usually used as supply voltage source.

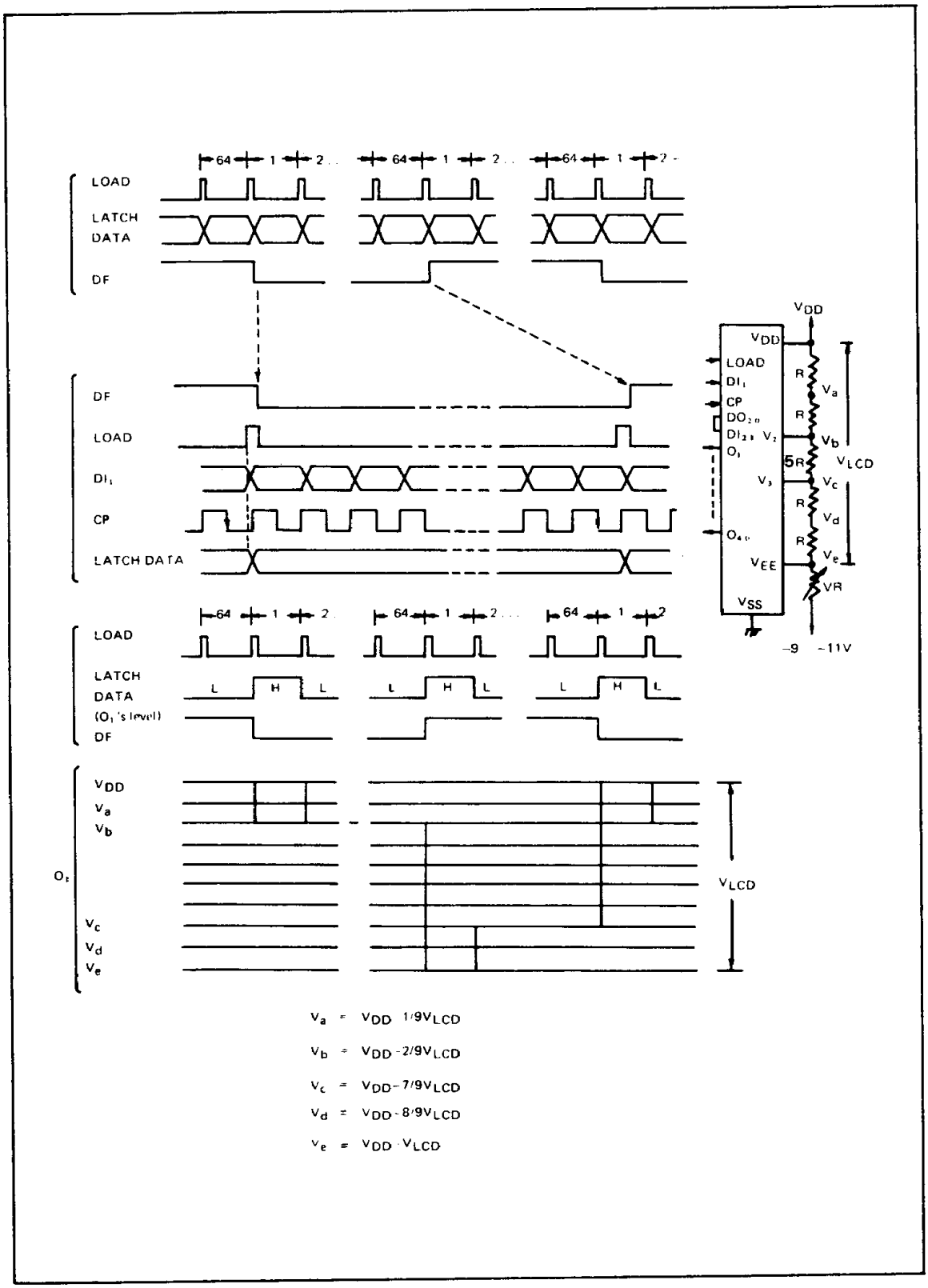
- **LOAD**
  The signal for latching the shift register contents is input from this pin.
  When LOAD pin is set at "H", the shift register contents are transferred to 40-bit 4-level driver. When LOAD pin is set at "L", the last display output data (O_1 ~ O_{40}), which was transferred when LOAD pin was at "H", is held.

- **O_1 ~ O_{40}**
  Display data output pins which correspond to each data bit in the latch.
  One of V_{DD}, V_2, V_3 or V_{EE} is selected as a display driving voltage source according to the combination of latched data level and DF signal.
  These pins should be connected to the SEGMENT side of the LCD panel. Refer to the truth table below.

Latched data	DF	Display data output level
H	H	V_{EE} (V_4)
	L	V_{DD}
L	H	V_3
	L	V_2

TIMING CHART

1/64 duty, 1/9 bias



$V_a = V_{DD} - 1/9V_{LCD}$

$V_b = V_{DD} - 2/9V_{LCD}$

$V_c = V_{DD} - 7/9V_{LCD}$

$V_d = V_{DD} - 8/9V_{LCD}$

$V_e = V_{DD} - V_{LCD}$

TYPICAL APPLICATION CIRCUIT

1/64 duty, 1/9 bias