

**Document Title**

4Bank x 2M x 16bits Synchronous DRAM

**Revision History**

| Revision No. | History                               | Draft Date | Remark |
|--------------|---------------------------------------|------------|--------|
| 1.0          | First Version Release                 | Dec. 2004  |        |
| 1.1          | 1. Corrected PIN ASSIGNMENT A12 to NC | Jan. 2005  |        |

## DESCRIPTION

The Hynix HY57V281620E(L)T(P) series is a 134,217,728bit CMOS Synchronous DRAM, ideally suited for the memory applications which require wide data I/O and high bandwidth. HY57V281620E(L)T(P) series is organized as 4banks of 2,097,152 x 16.

HY57V281620E(L)T(P) is offering fully synchronous operation referenced to a positive edge of the clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth. All input and output voltage levels are compatible with LVTTTL.

Programmable options include the length of pipeline (Read latency of 2 or 3), the number of consecutive read or write cycles initiated by a single control command (Burst length of 1,2,4,8 or full page), and the burst count sequence(sequential or interleave). A burst of read or write cycles in progress can be terminated by a burst terminate command or can be interrupted and replaced by a new burst read or write command on any cycle. (This pipelined design is not restricted by a '2N' rule)

## FEATURES

- Voltage: VDD, VDDQ 3.3V supply voltage
- All device pins are compatible with LVTTTL interface
- 54 Pin TSOPII (Lead or Lead Free Package)
- All inputs and outputs referenced to positive edge of system clock
- Data mask function by UDMQ, LDQM
- Internal four banks operation
- Auto refresh and self refresh
- 4096 Refresh cycles / 64ms
- Programmable Burst Length and Burst Type
  - 1, 2, 4, 8 or full page for Sequential Burst
  - 1, 2, 4 or 8 for Interleave Burst
- Programmable  $\overline{\text{CAS}}$  Latency; 2, 3 Clocks
- Burst Read Single Write operation

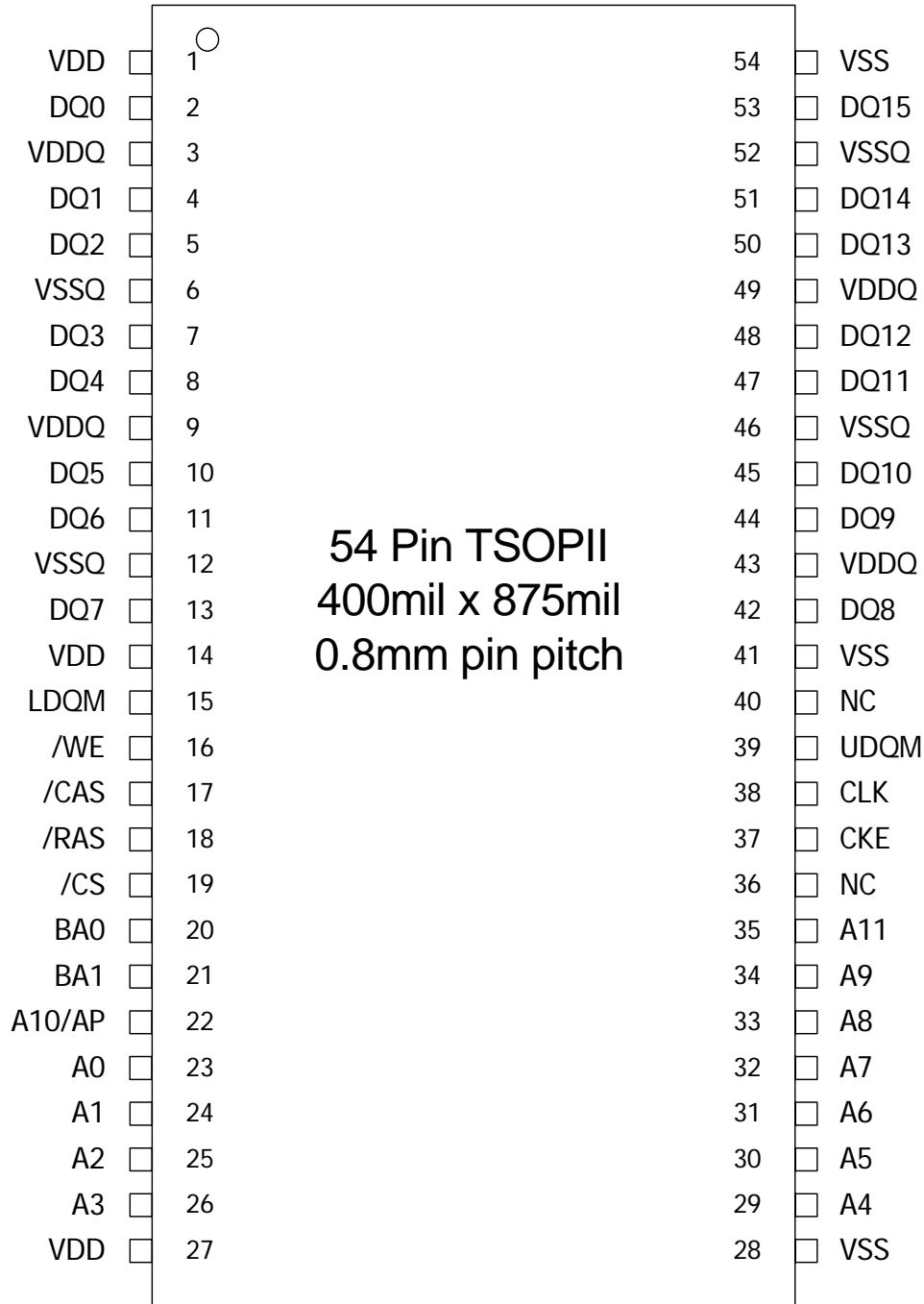
## ORDERING INFORMATION

| Part No.              | Clock Frequency | Organization        | Interface | Package       |
|-----------------------|-----------------|---------------------|-----------|---------------|
| HY57V281620E(L)T(P)-5 | 200MHz          | 4Banks x 2Mbits x16 | LVTTTL    | 54 Pin TSOPII |
| HY57V281620E(L)T(P)-6 | 166MHz          |                     |           |               |
| HY57V281620E(L)T(P)-7 | 143MHz          |                     |           |               |
| HY57V281620E(L)T(P)-H | 133MHz          |                     |           |               |

Note:

1. HY57V281620ET Series: Normal power, Leaded.
2. HY57V281620ELT Series: Low power, Leaded.
3. HY57V281620ETP Series: Normal power, Lead Free.
4. HY57V281620ELTP Series: Low power, Lead Free.

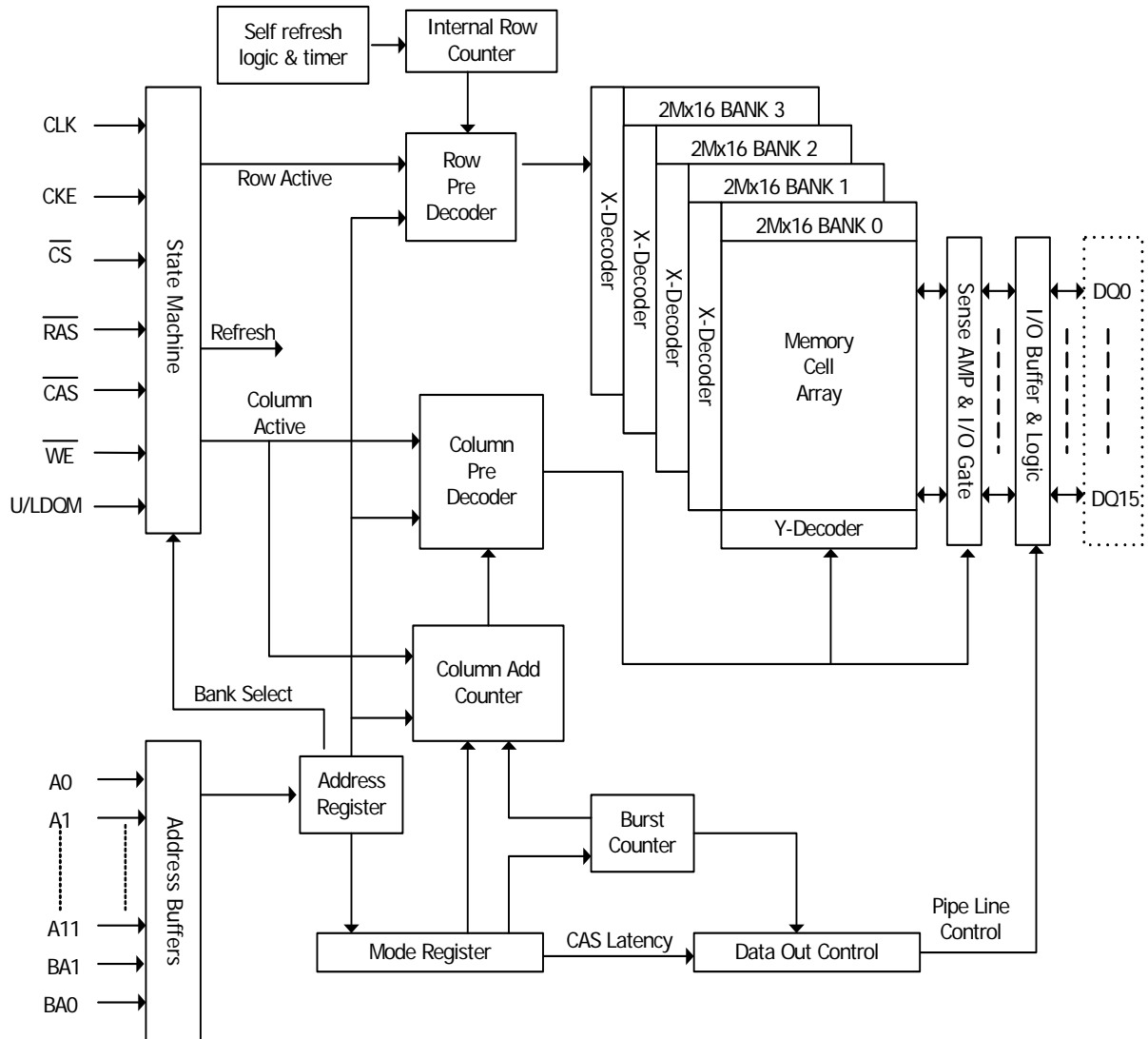
## PIN ASSIGNMENTS



## PIN DESCRIPTION

| SYMBOL  | TYPE  | DESCRIPTION  |
|---|---|--|
| CLK   | Clock   | The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK                                     |
| CKE   | Clock Enable  | Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh |
| $\overline{CS}$                                       | Chip Select   | Enables or disables all inputs except CLK, CKE, UDQM and LDQM  |
| BA0, BA1  | Bank Address  | Selects bank to be activated during $\overline{RAS}$ activity<br>Selects bank to be read/written during $\overline{CAS}$ activity  |
| A0 ~ A11  | Address   | Row Address: RA0 ~ RA11, Column Address: CA0 ~ CA8<br>Auto-precharge flag: A10   |
| $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ | Row Address Strobe,<br>Column Address Strobe,<br>Write Enable | $\overline{RAS}$ , $\overline{CAS}$ and $\overline{WE}$ define the operation<br>Refer function truth table for details             |
| UDQM, LDQM  | Data Input/Output Mask  | Controls output buffers in read mode and masks input data in write mode  |
| DQ0 ~ DQ15  | Data Input/Output   | Multiplexed data input / output pin  |
| VDD/VSS   | Power Supply/Ground   | Power supply for internal circuits and input buffers   |
| VDDQ/VSSQ   | Data Output Power/Ground                                      | Power supply for output buffers  |
| NC  | No Connection   | No connection  |

**FUNCTIONAL BLOCK DIAGRAM**  
2Mbit x 4banks x 16 I/O Synchronous DRAM



## BASIC FUNCTIONAL DESCRIPTION

### Mode Register

|     |     |     |     |         |    |    |             |    |    |    |              |    |    |
|-----|-----|-----|-----|---------|----|----|-------------|----|----|----|--------------|----|----|
| BA1 | BA0 | A11 | A10 | A9      | A8 | A7 | A6          | A5 | A4 | A3 | A2           | A1 | A0 |
| 0   | 0   | 0   | 0   | OP Code | 0  | 0  | CAS Latency |    |    | BT | Burst Length |    |    |

#### OP Code

| A9 | Write Mode                  |
|----|-----------------------------|
| 0  | Burst Read and Burst Write  |
| 1  | Burst Read and Single Write |

#### Burst Type

| A3 | Burst Type |
|----|------------|
| 0  | Sequential |
| 1  | Interleave |

#### CAS Latency

| A6 | A5 | A4 | CAS Latency |
|----|----|----|-------------|
| 0  | 0  | 0  | Reserved    |
| 0  | 0  | 1  | 1           |
| 0  | 1  | 0  | 2           |
| 0  | 1  | 1  | 3           |
| 1  | 0  | 0  | Reserved    |
| 1  | 0  | 1  | Reserved    |
| 1  | 1  | 0  | Reserved    |
| 1  | 1  | 1  | Reserved    |

#### Burst Length

| A2 | A1 | A0 | Burst Length |          |
|----|----|----|--------------|----------|
|    |    |    | A3 = 0       | A3 = 1   |
| 0  | 0  | 0  | 1            | 1        |
| 0  | 0  | 1  | 2            | 2        |
| 0  | 1  | 0  | 4            | 4        |
| 0  | 1  | 1  | 8            | 8        |
| 1  | 0  | 0  | Reserved     | Reserved |
| 1  | 0  | 1  | Reserved     | Reserved |
| 1  | 1  | 0  | Reserved     | Reserved |
| 1  | 1  | 1  | Full Page    | Reserved |

## ABSOLUTE MAXIMUM RATING

| Parameter                          | Symbol    | Rating     | Unit     |
|------------------------------------|-----------|------------|----------|
| Ambient Temperature                | TA        | 0 ~ 70     | °C       |
| Storage Temperature                | TSTG      | -55 ~ 125  | °C       |
| Voltage on Any Pin relative to VSS | VIN, VOUT | -1.0 ~ 4.6 | V        |
| Voltage on VDD relative to VSS     | VDD, VDDQ | -1.0 ~ 4.6 | V        |
| Short Circuit Output Current       | IOS       | 50         | mA       |
| Power Dissipation                  | PD        | 1          | W        |
| Soldering Temperature / Time       | TSOLDER   | 260 / 10   | °C / Sec |

## DC OPERATING CONDITION (TA= 0 to 70°C)

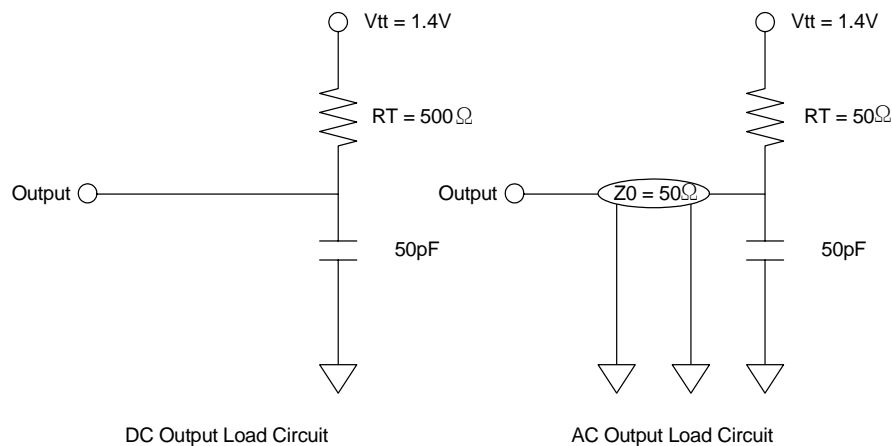
| Parameter            | Symbol    | Min. | Typ | Max        | Unit | Note |
|----------------------|-----------|------|-----|------------|------|------|
| Power Supply Voltage | VDD, VDDQ | 3.0  | 3.3 | 3.6        | V    | 1    |
| Input High Voltage   | VIH       | 2.0  | 3.0 | VDDQ + 0.3 | V    | 1, 2 |
| Input Low Voltage    | VIL       | -0.3 | -   | 0.8        | V    | 1, 3 |

- Note: 1. All voltages are referenced to VSS = 0V  
 2. VIH(max) is acceptable 5.6V AC pulse width with <=3ns of duration.  
 3. VIL(min) is acceptable -2.0V AC pulse width with <=3ns of duration

## AC OPERATING TEST CONDITION (TA= 0 to 70 °C, VDD=3.3±0.3V, VSS=0V)

| Parameter   | Symbol    | Value     | Unit | Note |
|---|-----------|-----------|------|------|
| AC Input High / Low Level Voltage                   | VIH / VIL | 2.4 / 0.4 | V    |      |
| Input Timing Measurement Reference Level Voltage    | Vtrip     | 1.4       | V    |      |
| Input Rise / Fall Time                              | tR / tF   | 1         | ns   |      |
| Output Timing Measurement Reference Level Voltage   | Voutref   | 1.4       | V    |      |
| Output Load Capacitance for Access Time Measurement | CL        | 50        | pF   | 1    |

Note 1.



**CAPACITANCE** (TA= 0 to 70 °C, f=1MHz, VDD=3.3V)

| Parameter                       | Pin  | Symbol | Min | Max | Unit |
|---------------------------------|--|--------|-----|-----|------|
| Input capacitance               | CLK  | CI1    | 2.0 | 4.0 | pF   |
|                                 | A0 ~ A11, BA0, BA1, CKE, $\overline{CS}$ , $\overline{RAS}$ , $\overline{CAS}$ ,<br>$\overline{WE}$ , LDQM, UDQM | CI2    | 2.5 | 5.0 | pF   |
| Data input / output capacitance | DQ0 ~ DQ15   | CI/O   | 3.0 | 5.5 | pF   |

**DC CHARACTERISTICS I** (TA= 0 to 70°C)

| Parameter              | Symbol | Min | Max | Unit | Note       |
|------------------------|--------|-----|-----|------|------------|
| Input Leakage Current  | ILI    | -1  | 1   | uA   | 1          |
| Output Leakage Current | ILO    | -1  | 1   | uA   | 2          |
| Output High Voltage    | VOH    | 2.4 | -   | V    | IOH = -2mA |
| Output Low Voltage     | VOL    | -   | 0.4 | V    | IOL = +2mA |

Note:

- VIN = 0 to 3.3V, All other balls are not tested under VIN =0V
- DOUT is disabled, VOUT=0 to 3.6



**DC CHARACTERISTICS II** (TA= 0 to 70°C)

| Parameter  | Symbol | Test Condition   | Speed     |     |     |     | Unit | Note |   |
|--|--------|--|-----------|-----|-----|-----|------|------|---|
|  |        |  | 5         | 6   | 7   | H   |      |      |   |
| Operating Current                                | IDD1   | Burst length=1, One bank active<br>t <sub>RC</sub> ≥ t <sub>RC</sub> (min), I <sub>OL</sub> =0mA   | 120       | 110 | 100 | 100 | mA   | 1    |   |
| Precharge Standby Current in Power Down Mode     | IDD2P  | CKE ≤ V <sub>IL</sub> (max), t <sub>CK</sub> = 15ns  | 2         |     |     |     | mA   |      |   |
|  | IDD2PS | CKE ≤ V <sub>IL</sub> (max), t <sub>CK</sub> = ∞   | 2         |     |     |     | mA   |      |   |
| Precharge Standby Current in Non Power Down Mode | IDD2N  | CKE ≥ V <sub>IH</sub> (min), $\overline{CS}$ ≥ V <sub>IH</sub> (min), t <sub>CK</sub> = 15ns<br>Input signals are changed one time during 2clks.<br>All other pins ≥ V <sub>DD</sub> -0.2V or ≤ 0.2V | 18        |     |     |     | mA   |      |   |
|  | IDD2NS | CKE ≥ V <sub>IH</sub> (min), t <sub>CK</sub> = ∞<br>Input signals are stable.  | 15        |     |     |     |      |      |   |
| Active Standby Current in Power Down Mode        | IDD3P  | CKE ≤ V <sub>IL</sub> (max), t <sub>CK</sub> = 15ns  | 3         |     |     |     | mA   |      |   |
|  | IDD3PS | CKE ≤ V <sub>IL</sub> (max), t <sub>CK</sub> = ∞   | 3         |     |     |     |      |      |   |
| Active Standby Current in Non Power Down Mode    | IDD3N  | CKE ≥ V <sub>IH</sub> (min), $\overline{CS}$ ≥ V <sub>IH</sub> (min), t <sub>CK</sub> = 15ns<br>Input signals are changed one time during 2clks.<br>All other pins ≥ V <sub>DD</sub> -0.2V or ≤ 0.2V | 40        |     |     |     | mA   |      |   |
|  | IDD3NS | CKE ≥ V <sub>IH</sub> (min), t <sub>CK</sub> = ∞<br>Input signals are stable.  | 35        |     |     |     |      |      |   |
| Burst Mode Operating Current                     | IDD4   | t <sub>CK</sub> ≥ t <sub>CK</sub> (min), I <sub>OL</sub> =0mA<br>All banks active  | 120       | 110 | 100 | 100 | mA   | 1    |   |
| Auto Refresh Current                             | IDD5   | t <sub>RC</sub> ≥ t <sub>RC</sub> (min), All banks active  | 210       | 200 | 190 | 190 | mA   | 2    |   |
| Self Refresh Current                             | IDD6   | CKE ≤ 0.2V   | Normal    | 2   |     |     |      | mA   | 3 |
|  |        |  | Low power | 800 |     |     |      | uA   |   |

**Note:** 1. IDD1 and IDD4 depend on output loading and cycle rates. Specified values are measured with the output open  
2. Min. of t<sub>RRC</sub> (Refresh  $\overline{RAS}$  cycle time) is shown at AC CHARACTERISTICS II  
3. HY57V281620ET(P) Series: Normal Power  
HY57V281620ELT(P) Series: Low Power

**AC CHARACTERISTICS I** (AC operating conditions unless otherwise noted)

| Parameter                               |                                      | Sym-<br>bol | 5    |      | 6   |      | 7   |      | H   |      | Unit | Note |
|---|--------------------------------------|-------------|------|------|-----|------|-----|------|-----|------|------|------|
|   |                                      |             | Min  | Max  | Min | Max  | Min | Max  | Min | Max  |      |      |
| System Clock<br>Cycle Time              | $\overline{\text{CAS}}$<br>Latency=3 | tCK3        | 5.0  | 1000 | 6.0 | 1000 | 7.0 | 1000 | 7.5 | 1000 | ns   |      |
|   | $\overline{\text{CAS}}$<br>Latency=2 | tCK2        | 10   |      | 10  |      | 10  |      | 10  |      | ns   |      |
| Clock High Pulse Width                  |                                      | tCHW        | 1.75 | -    | 2.0 | -    | 2.0 | -    | 2.5 | -    | ns   | 1    |
| Clock Low Pulse Width                   |                                      | tCLW        | 1.75 | -    | 2.0 | -    | 2.0 | -    | 2.5 | -    | ns   | 1    |
| Access Time<br>From Clock               | $\overline{\text{CAS}}$<br>Latency=3 | tAC3        | -    | 4.5  | -   | 5.4  | -   | 5.4  | -   | 5.4  | ns   | 2    |
|   | $\overline{\text{CAS}}$<br>Latency=2 | tAC2        | -    | 6.0  | -   | 6.0  | -   | 6.0  | -   | 6.0  | ns   |      |
| Data-out Hold Time                      |                                      | tOH         | 2.0  | -    | 2.0 | -    | 2.5 | -    | 2.5 | -    | ns   |      |
| Data-Input Setup Time                   |                                      | tDS         | 1.5  | -    | 1.5 | -    | 1.5 | -    | 1.5 | -    | ns   | 1    |
| Data-Input Hold Time                    |                                      | tDH         | 0.8  | -    | 0.8 | -    | 0.8 | -    | 0.8 | -    | ns   | 1    |
| Address Setup Time                      |                                      | tAS         | 1.5  | -    | 1.5 | -    | 1.5 | -    | 1.5 | -    | ns   | 1    |
| Address Hold Time                       |                                      | tAH         | 0.8  | -    | 0.8 | -    | 0.8 | -    | 0.8 | -    | ns   | 1    |
| CKE Setup Time                          |                                      | tCKS        | 1.5  | -    | 1.5 | -    | 1.5 | -    | 1.5 | -    | ns   | 1    |
| CKE Hold Time                           |                                      | tCKH        | 0.8  | -    | 0.8 | -    | 0.8 | -    | 0.8 | -    | ns   | 1    |
| Command Setup Time                      |                                      | tCS         | 1.5  | -    | 1.5 | -    | 1.5 | -    | 1.5 | -    | ns   | 1    |
| Command Hold Time                       |                                      | tCH         | 0.8  | -    | 0.8 | -    | 0.8 | -    | 0.8 | -    | ns   | 1    |
| CLK to Data Output in Low-Z Time        |                                      | tOLZ        | 1.0  | -    | 1.0 | -    | 1.5 | -    | 1.5 | -    | ns   |      |
| CLK to<br>Data Output<br>in High-Z Time | $\overline{\text{CAS}}$<br>Latency=3 | tOHZ3       | -    | 4.5  | -   | 5.4  | -   | 5.4  | -   | 5.4  | ns   |      |
|   | $\overline{\text{CAS}}$<br>Latency=2 | tOHZ2       | -    | 6.0  | -   | 6.0  | -   | 6.0  | -   | 6.0  | ns   |      |

Note:

1. Assume  $t_R$  /  $t_F$  (input rise and fall time) is 1ns. If  $t_R$  &  $t_F$  > 1ns, then  $[(t_R+t_F)/2-1]$ ns should be added to the parameter.
2. Access time to be measured with input signals of 1V/ns edge rate, from 0.8V to 0.2V. If  $t_R$  > 1ns, then  $(t_R/2-0.5)$ ns should be added to the parameter.

**AC CHARACTERISTICS II** (AC operating conditions unless otherwise noted)

| Parameter                       |               | Symbol | 5          |      | 6   |      | 7   |      | H   |      | Unit | Note |
|---------------------------------|---------------|--------|------------|------|-----|------|-----|------|-----|------|------|------|
|                                 |               |        | Min        | Max  | Min | Max  | Min | Max  | Min | Max  |      |      |
| RAS Cycle Time                  | Operation     | tRC    | 55         | -    | 60  | -    | 63  | -    | 63  | -    | ns   |      |
| RAS Cycle Time                  | Auto Refresh  | tRRC   | 55         | -    | 60  | -    | 63  | -    | 63  | -    | ns   |      |
| RAS to CAS Delay                |               | tRCD   | 15         | -    | 18  | -    | 20  | -    | 20  | -    | ns   |      |
| RAS Active Time                 |               | tRAS   | 38.7       | 100K | 42  | 100K | 42  | 100K | 42  | 120K | ns   |      |
| RAS Precharge Time              |               | tRP    | 15         | -    | 18  | -    | 20  | -    | 20  | -    | ns   |      |
| RAS to RAS Bank Active Delay    |               | tRRD   | 10         | -    | 12  | -    | 14  | -    | 15  | -    | ns   |      |
| CAS to CAS Delay                |               | tCCD   | 1          | -    | 1   | -    | 1   | -    | 1   | -    | CLK  |      |
| Write Command to Data-In Delay  |               | tWTL   | 0          | -    | 0   | -    | 0   | -    | 0   | -    | CLK  |      |
| Data-in to Precharge Command    |               | tDPL   | 2          | -    | 2   | -    | 2   | -    | 2   | -    | CLK  |      |
| Data-In to Active Command       |               | tDAL   | tDPL + tRP |      |     |      |     |      |     |      |      |      |
| DQM to Data-Out Hi-Z            |               | tDOZ   | 2          | -    | 2   | -    | 2   | -    | 2   | -    | CLK  |      |
| DQM to Data-In Mask             |               | tDQM   | 0          | -    | 0   | -    | 0   | -    | 0   | -    | CLK  |      |
| MRS to New Command              |               | tMRD   | 2          | -    | 2   | -    | 2   | -    | 2   | -    | CLK  |      |
| Precharge to Data Output High-Z | CAS Latency=3 | tPROZ3 | 3          | -    | 3   | -    | 3   | -    | 3   | -    | CLK  |      |
|                                 | CAS Latency=2 | tPROZ2 | 2          | -    | 2   | -    | 2   | -    | 2   | -    | CLK  |      |
| Power Down Exit Time            |               | tDPE   | 1          | -    | 1   | -    | 1   | -    | 1   | -    | CLK  |      |
| Self Refresh Exit Time          |               | tSRE   | 1          | -    | 1   | -    | 1   | -    | 1   | -    | CLK  | 1    |
| Refresh Time                    |               | tREF   | -          | 64   | -   | 64   | -   | 64   | -   | 64   | ms   |      |

Note: 1. A new command can be given tRRC after self refresh exit.

**COMMAND TRUTH TABLE**

| Command                   | CKEn-1 | CKEn | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | DQM | ADDR                                  | A10/AP | BA | Note     |  |
|---------------------------|--------|------|-----------------|------------------|------------------|-----------------|-----|---------------------------------------|--------|----|----------|--|
| Mode Register Set         | H      | X    | L               | L                | L                | L               | X   | OP code                               |        |    |          |  |
| No Operation              | H      | X    | H               | X                | X                | X               | X   | X                                     |        |    |          |  |
|                           |        |      | L               | H                | H                | H               |     |                                       |        |    |          |  |
| Bank Active               | H      | X    | L               | L                | H                | H               | X   | RA                                    |        | V  |          |  |
| Read                      | H      | X    | L               | H                | L                | H               | X   | CA                                    | L      | V  |          |  |
| Read with Autoprecharge   |        |      |                 |                  |                  |                 |     |                                       | H      |    |          |  |
| Write                     | H      | X    | L               | H                | L                | L               | X   | CA                                    | L      | V  |          |  |
| Write with Autoprecharge  |        |      |                 |                  |                  |                 |     |                                       | H      |    |          |  |
| Precharge All Banks       | H      | X    | L               | L                | H                | L               | X   | X                                     | H      | X  |          |  |
| Precharge selected Bank   |        |      |                 |                  |                  |                 |     |                                       | L      | V  |          |  |
| Burst Stop                | H      | X    | L               | H                | H                | L               | X   | X                                     |        |    |          |  |
| DQM                       | H      | X    |                 |                  |                  |                 | V   | X                                     |        |    |          |  |
| Auto Refresh              | H      | H    | L               | L                | L                | H               | X   | X                                     |        |    |          |  |
| Burst-Read-Single-WRITE   | H      | X    | L               | L                | L                | L               | X   | A9 ball High<br>(Other balls OP code) |        |    | MRS Mode |  |
| Self Refresh <sup>1</sup> | Entry  | H    | L               | L                | L                | L               | H   | X                                     | X      |    |          |  |
|                           | Exit   | L    | H               | H                | H                | H               | H   | X                                     |        |    |          |  |
| Precharge power down      | Entry  | H    | L               | H                | X                | X               | X   | X                                     | X      |    |          |  |
|                           |        |      |                 | L                | H                | H               | H   |                                       |        |    |          |  |
|                           | Exit   | L    | H               | H                | X                | X               | X   | X                                     |        |    |          |  |
|                           |        |      |                 | L                | H                | H               | H   |                                       |        |    |          |  |
| Clock Suspend             | Entry  | H    | L               | H                | X                | X               | X   | X                                     | X      |    |          |  |
|                           |        |      |                 | L                | V                | V               | V   |                                       |        |    |          |  |
|                           | Exit   | L    | H               | X                |                  |                 |     | X                                     |        |    |          |  |

### PACKAGE INFORMATION

400mil 54pin Thin Small Outline Package

