



# 3.3V Single LVDS Driver/Receiver

MAX9164

## General Description

The MAX9164 high-speed LVDS driver/receiver is designed specifically for low-power point-to-point applications. The MAX9164 operates from a single 3.3V power supply, and is pin compatible with DS90LV019. The device features an independent differential driver and receiver.

The MAX9164 driver output uses a current-steering configuration to generate a 3.1mA drive current. The driver accepts a single-ended input and translates it to LVDS signals at speeds up to 200Mbps over controlled-impedance media of approximately 100Ω. The transmission media may be printed circuit board traces or cables. The enable logic input, DE, is used to enable or disable the driver.

The MAX9164 receiver detects a differential input as low as 100mV and translates it to single-ended output at speeds up to 200Mbps. The enable logic input, RE, is used to enable or disable the receiver.

Inputs and outputs conform to the ANSI TIA/EIA-644 LVDS standard. The MAX9164 is offered in 14-lead SO and TSSOP packages, and is specified for operation from -40°C to +85°C.

## Applications

- Cell-Phone Base Stations      Network Switches/Routers
- Add/Drop Muxes                Backplane Interconnect
- Digital Cross-Connects        Clock Distribution
- DSLAMs

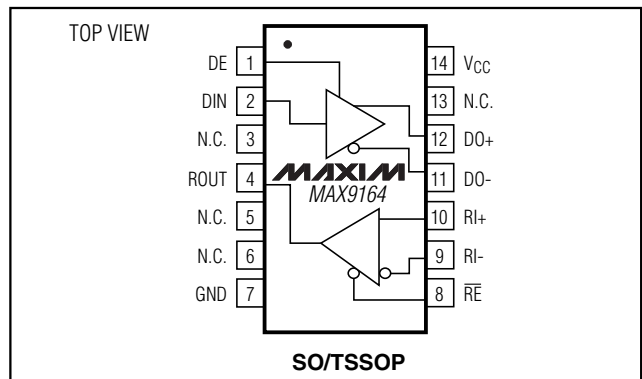
## Features

- ◆ 3.3V Operation
- ◆ 35% Lower Power than DS90LV019
- ◆ 200Mbps Data Signaling Rate
- ◆ ±1V Common-Mode Range
- ◆ ±100mV Receiver Sensitivity
- ◆ Flow-Through Pinout
- ◆ Receiver Output High for Open Input

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9164ESD	-40°C to +85°C	14 SO
MAX9164EUD	-40°C to +85°C	14 TSSOP

## Pin Configuration



## Typical Application Circuit

**TABLE 1. DRIVER FUNCTION TABLE**

INPUTS		OUTPUTS	
DE	DIN	DO+	DO-
H	L ( $\leq 0.8V$ )	L	H
H	H ( $\geq 2.0V$ )	H	L
H	(> 0.8V and < 2.0V)	Undefined	Undefined
L	X	Z	Z

X: High or low  
Z: High impedance

**TABLE 2. RECEIVER FUNCTION TABLE**

INPUTS		OUTPUT
RE	RI+ - RI-	ROUT
L	L ( $\leq -100mV$ )	L
L	H ( $\geq 100mV$ )	H
L	(> -100mV and < 100mV)	Undefined
L	Open	H
H	X	Z

X: High or low  
Z: High impedance

## 3.3V Single LVDS Driver/Receiver

### ABSOLUTE MAXIMUM RATINGS

V <sub>CC</sub> to GND	-0.3V to +4.0V	Operating Temperature Range	-40°C to +85°C
DO+, DO-, RI+, RI- to GND	-0.3V to +4.0V	Junction Temperature	+150°C
DIN, ROUT, DE, RE to GND	-0.3V to (V <sub>CC</sub> + 0.3V)	Storage Temperature Range	-65°C to +150°C
Driver Short-Circuit Current	Continuous	ESD Protection	HBM (1.5kΩ, 100pF), DO+, DO-, RI+, RI-, DE, RE, DIN, ROUT > ±2kV
Continuous Power Dissipation (T <sub>A</sub> = +70°C)		Lead Temperature (soldering, 10s)	+300°C
14-Pin SO (derate 8.3mW/°C above +70°C)	667mW		
14-Pin TSSOP (derate 9.1mW/°C above +70°C)	727mW		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### DC ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = 3.0V to 3.6V, |V<sub>ID</sub>| = 0.1V to 2.4V, common-mode input voltage (V<sub>CM</sub>) = |V<sub>ID</sub>|/2 to 2.4V - |V<sub>ID</sub>|/2, R<sub>L</sub> = 100Ω ±1%, T<sub>A</sub> = -40°C to +85°C. Typical values are at V<sub>CC</sub> = 3.3V, |V<sub>ID</sub>| = 0.2V, V<sub>CM</sub> = 1.2V, T<sub>A</sub> = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>SINGLE-ENDED INPUTS (DIN, DE, RE)</b>						
Input High Voltage	V <sub>IH</sub>		2.0		V <sub>CC</sub>	V
Input Low Voltage	V <sub>IL</sub>		0		0.8	V
Input Current	I <sub>IN</sub>	RE, DE, DIN = high or low	-10		+10	μA
Input Diode Clamp Voltage	V <sub>CL</sub>	I <sub>CLAMP</sub> = -18mA	-1.5			V
<b>DRIVER OUTPUT (DO+, DO-)</b>						
Differential Output Voltage	V <sub>OD</sub>	Figure 1	250	310	450	mV
Change in Magnitude of V <sub>OD</sub> Between Complementary Output States	ΔV <sub>OD</sub>	Figure 1		0.02	25	mV
Offset Voltage	V <sub>OS</sub>	Figure 1	1.0	1.29	1.7	V
Change in Magnitude of V <sub>OS</sub> Between Complementary Output States	ΔV <sub>OS</sub>	Figure 1		0.8	25	mV
High-Impedance Leakage Current	I <sub>OZD</sub>	DE = 0; DO+, DO- = V <sub>CC</sub> or 0	-1		+1	μA
Power-Off Leakage Current	I <sub>OXD</sub>	DO+, DO- = 3.6V or 0; V <sub>CC</sub> = 0	-1		+1	μA
Output Short-Circuit Current	I <sub>OSD</sub>	DO+ = 0 at DIN = V <sub>CC</sub>		-3	-10	mA
		DO- = 0 at DIN = 0		-3	-10	
Output Capacitance	C <sub>DO</sub>	Capacitance from DO+ or DO- to 0		3.7		pF
<b>RECEIVER INPUT (RI+, RI-)</b>						
Differential Input High Threshold	V <sub>TH</sub>				100	mV
Differential Input Low Threshold	V <sub>TL</sub>		-100			mV
Input Current	I <sub>IN</sub>	V <sub>CC</sub> = 3.6V or 0; RI+, RI- = 2.4V or 0	-10		+10	μA
Input Capacitance	C <sub>RI</sub>	RI+ or RI- to 0		5		pF
<b>RECEIVER OUTPUT (ROUT)</b>						
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -400μA	V <sub>ID</sub> = 100mV	2.9	3.28	V
			RI+, RI- open			
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = +2.0mA, V <sub>ID</sub> = -100mV		0.025	0.4	V
Output Short-Circuit Current	I <sub>OS</sub>	V <sub>ID</sub> = +100mV, ROUT = 0	-20	-28	-75	mA

## 3.3V Single LVDS Driver/Receiver

### DC ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = 3.0V$  to  $3.6V$ ,  $|V_{ID}| = 0.1V$  to  $2.4V$ , common-mode input voltage ( $V_{CM}$ ) =  $|V_{ID}|/2$  to  $2.4V - |V_{ID}|/2$ ,  $R_L = 100\Omega \pm 1\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ . Typical values are at  $V_{CC} = 3.3V$ ,  $|V_{ID}| = 0.2V$ ,  $V_{CM} = 1.2V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>SUPPLY CURRENT</b>						
Supply Current	$I_{CC}$	$DE = V_{CC}$ , $\overline{RE} = 0$		7.4	12.5	mA
Driver Supply Current	$I_{CCD}$	$DE = \overline{RE} = V_{CC}$		7.4	12.5	mA
Receiver Supply Current	$I_{CCR}$	$DE = \overline{RE} = 0$		4.4	7.0	mA
Disable Supply Current	$I_{CCZ}$	$DE = 0$ , $\overline{RE} = V_{CC}$		4.4	7.0	mA

### AC ELECTRICAL CHARACTERISTICS

( $V_{CC} = 3.0V$  to  $3.6V$ ,  $|V_{ID}| = 0.2V$ ,  $V_{CM} = 1.2V$ ,  $R_L = 100\Omega \pm 1\%$ ,  $C_L = 10pF$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ . Typical values are at  $V_{CC} = 3.3V$ ,  $|V_{ID}| = 0.2V$ ,  $V_{CM} = 1.2V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.) (Notes 3, 4, 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DRIVER</b>						
Differential High-to-Low Propagation Delay	$t_{PHLD}$	Figure 2	2.0	4.4	6.5	ns
Differential Low-to-High Propagation Delay	$t_{PLHD}$	Figure 2	1.0	4.2	7.0	ns
Differential Skew   $t_{PHLD} - t_{PLHD}$	$t_{SKD}$	Figure 2		0.2	1.0	ns
Rise Time	$t_{TLHD}$	Figure 2	0.2	0.9	3.0	ns
Fall Time	$t_{THLD}$	Figure 2	0.2	0.8	3.0	ns
Disable Time High to Z	$t_{PHZ}$	Figure 3	1.5	6.0	8.0	ns
Disable Time Low to Z	$t_{PLZ}$	Figure 3	2.5	5.5	9.0	ns
Enable Time Z to High	$t_{PZH}$	Figure 3	4.0	5.5	8.0	ns
Enable Time Z to Low	$t_{PZL}$	Figure 3	3.8	5.0	8.0	ns
<b>RECEIVER</b>						
Differential High-to-Low Propagation Delay	$t_{PHL}$	Figure 4	3.0	5.4	7.0	ns
Differential Low-to-High Propagation Delay	$t_{PLH}$	Figure 4	3.0	5.3	9.0	ns
Differential Skew   $t_{PHL} - t_{PLH}$	$t_{SK}$	Figure 4		0.14	1.5	ns
Rise Time	$t_{TLH}$	Figure 4	0.15	0.8	3.0	ns
Fall Time	$t_{THL}$	Figure 4	0.15	0.4	3.0	ns
Disable Time High to Z	$t_{PHZ}$	Figure 5	3.0	5.4	6.0	ns
Disable Time Low to Z	$t_{PLZ}$	Figure 5	3.0	5.1	6.0	ns
Enable Time Z to High	$t_{PZH}$	Figure 5	3.0	5.4	8.0	ns
Enable Time Z to Low	$t_{PZL}$	Figure 5	3.0	5.1	8.0	ns

**Note 1:** Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are 100% tested at  $T_A = +25^\circ C$ .

**Note 2:** Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to device ground except  $V_{TH}$ ,  $V_{TL}$ ,  $V_{ID}$ ,  $V_{OD}$ , and  $\Delta V_{OD}$ .

**Note 3:**  $C_L$  includes probe and jig capacitance.

**Note 4:** AC parameters are guaranteed by design and characterization.

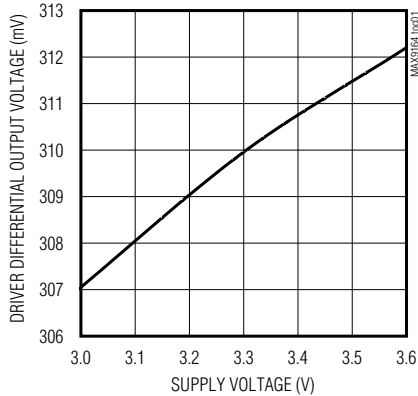
**Note 5:** Generator waveforms for all tests unless otherwise specified:  $f = 100MHz$ ,  $Z_0 = 50\Omega$ ,  $t_R = t_F = 6.0ns$  (0 to 3V, 0% to 100%) for DE and  $\overline{RE}$ ,  $t_R = t_F = 3.0ns$  (0 to 3V, 0% to 100%) for DIN, and  $t_R = t_F = 1.0ns$  ( $|V_{ID}| = 0.2V$ , 20% to 80%) for RI+/RI- inputs.

# 3.3V Single LVDS Driver/Receiver

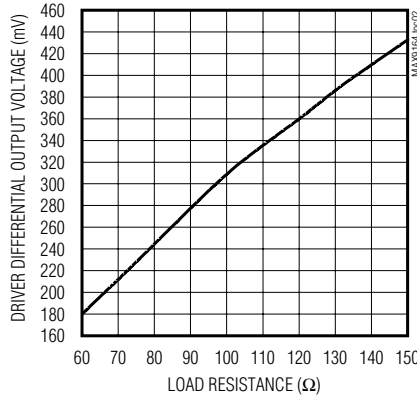
## Typical Operating Characteristics

( $V_{CC} = 3.3V$ ,  $I_{VID} = 0.2V$ ,  $V_{CM} = 1.2V$ ,  $R_L = 100\Omega \pm 1\%$ ,  $FREQ = 100MHz$ ,  $C_L = 10pF$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

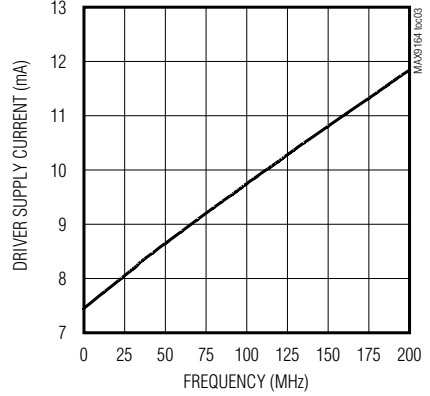
**DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. SUPPLY VOLTAGE**



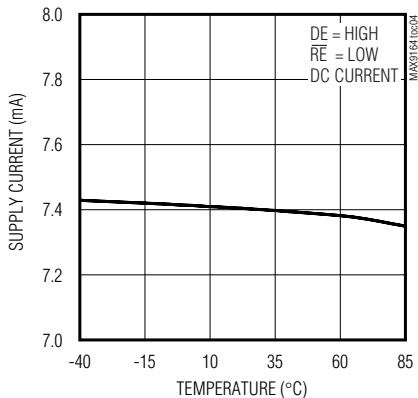
**DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. LOAD RESISTANCE**



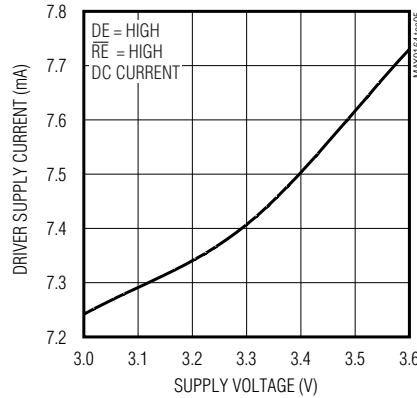
**DRIVER SUPPLY CURRENT vs. FREQUENCY**



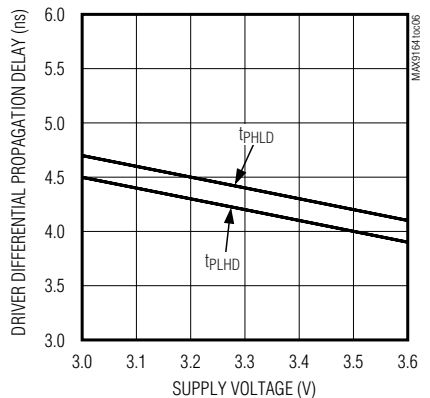
**SUPPLY CURRENT (I<sub>CC</sub>) vs. TEMPERATURE**



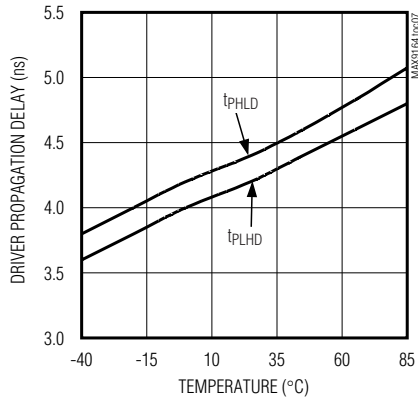
**DRIVER SUPPLY CURRENT (I<sub>CC</sub>) vs. SUPPLY VOLTAGE**



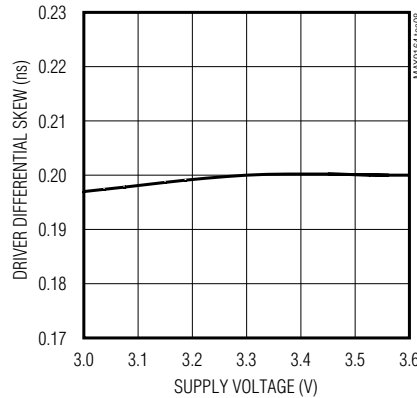
**DRIVER DIFFERENTIAL PROPAGATION DELAY vs. SUPPLY VOLTAGE**



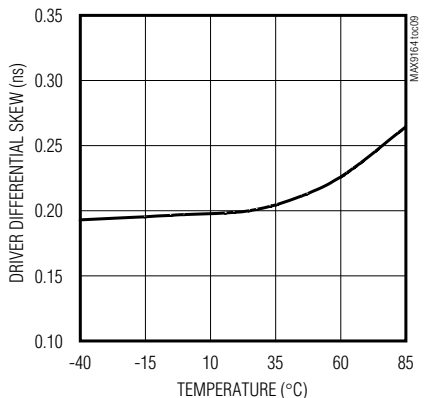
**DRIVER DIFFERENTIAL PROPAGATION DELAY vs. TEMPERATURE**



**DRIVER DIFFERENTIAL SKEW vs. SUPPLY VOLTAGE**



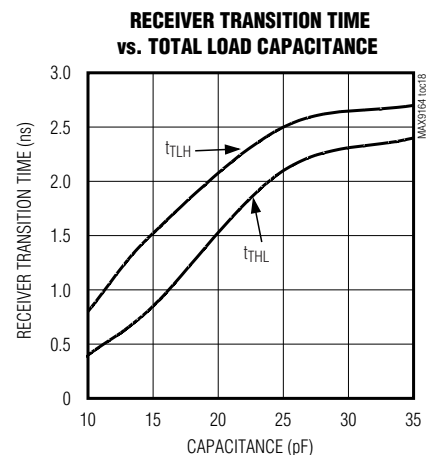
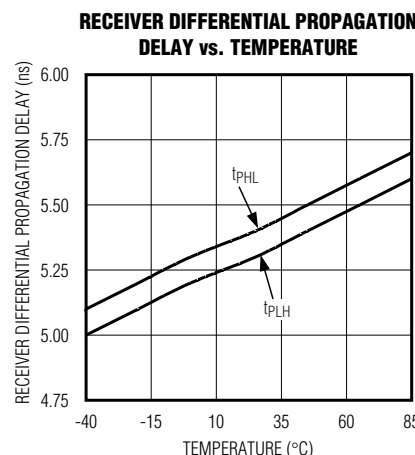
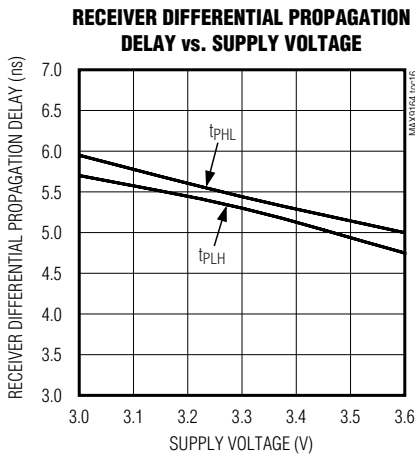
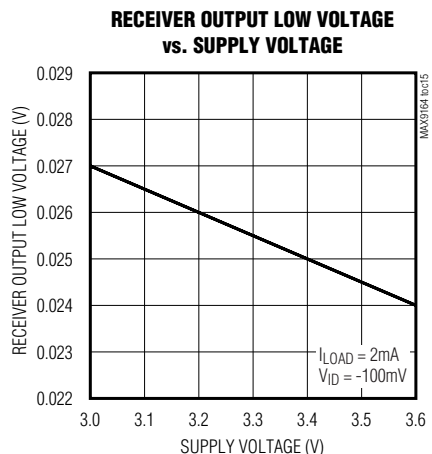
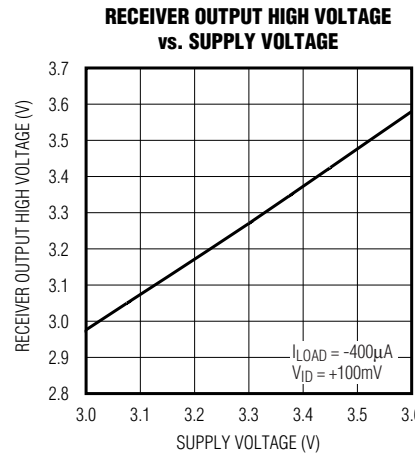
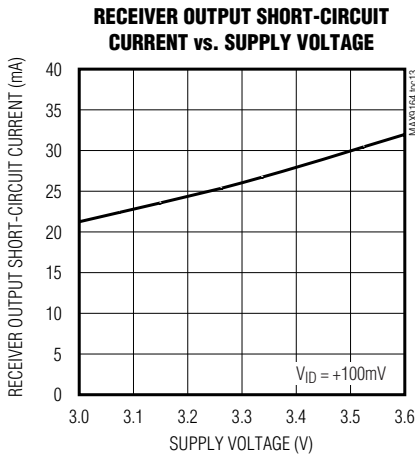
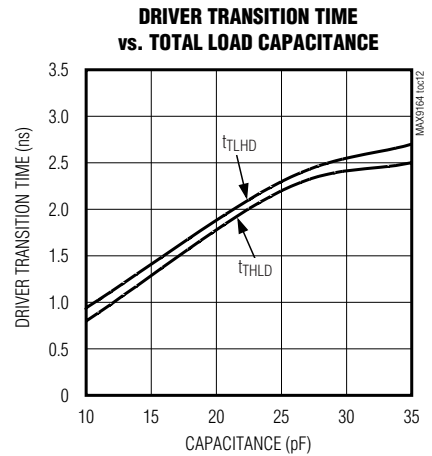
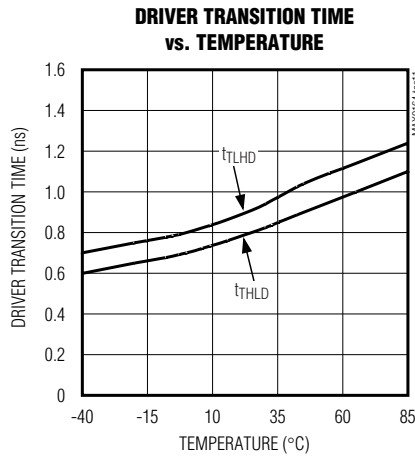
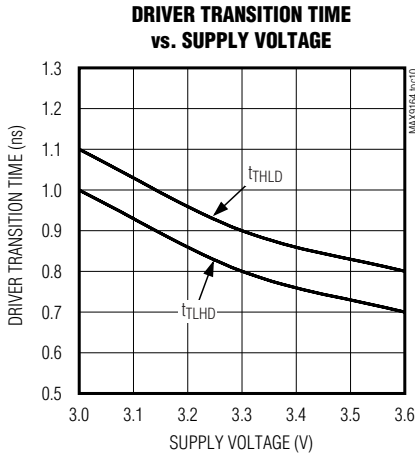
**DRIVER DIFFERENTIAL SKEW vs. TEMPERATURE**



## 3.3V Single LVDS Driver/Receiver

### Typical Operating Characteristics (continued)

( $V_{CC} = 3.3V$ ,  $I_{VID} = 0.2V$ ,  $V_{CM} = 1.2V$ ,  $R_L = 100\Omega \pm 1\%$ ,  $FREQ = 100MHz$ ,  $C_L = 10pF$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



## 3.3V Single LVDS Driver/Receiver

### Pin Description

PIN	NAME	FUNCTION
1	DE	LVTTTL/LVCMOS Driver Enable Input. The driver is enabled when DE is high. When DE is low, the driver outputs, DO+ and DO-, are disabled and are high impedance.
2	DIN	LVTTTL/LVCMOS Driver Input
3, 5, 6, 13	N.C.	No Connection. Not internally connected.
4	ROUT	LVTTTL/LVCMOS Receiver Output
7	GND	Ground
8	$\overline{RE}$	LVTTTL/LVCMOS Receiver Enable Input. The receiver is enabled when $\overline{RE}$ is low. When $\overline{RE}$ is high, the receiver output is disabled and is high impedance.
9	RI-	Inverting LVDS Receiver Input. RI- has an integrated pulldown to GND.
10	RI+	Noninverting LVDS Receiver Input. RI+ has an integrated pullup to $V_{CC}$ .
11	DO-	Inverting LVDS Driver Output
12	DO+	Noninverting LVDS Driver Output
14	$V_{CC}$	Power-Supply Input. Bypass $V_{CC}$ to GND with 0.1 $\mu$ F and 0.001 $\mu$ F ceramic capacitors.

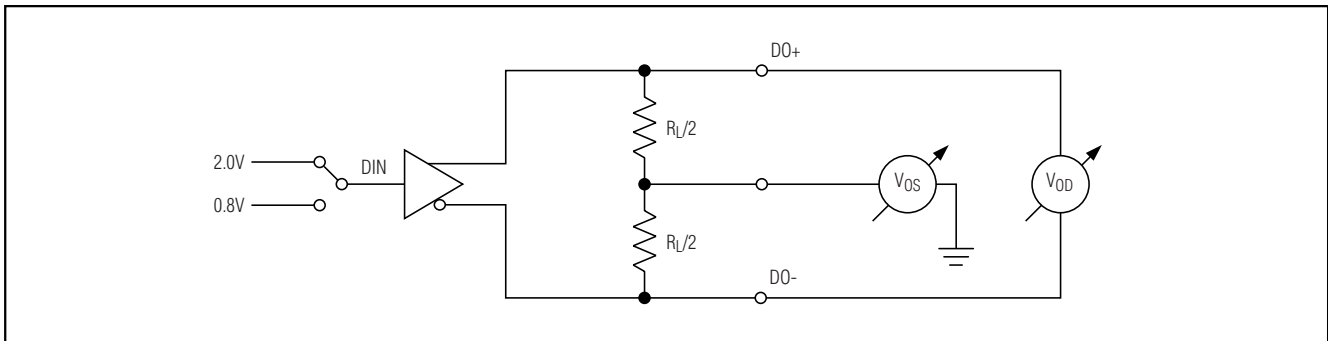


Figure 1. Differential Driver DC Test Circuit

# 3.3V Single LVDS Driver/Receiver

MAX9164

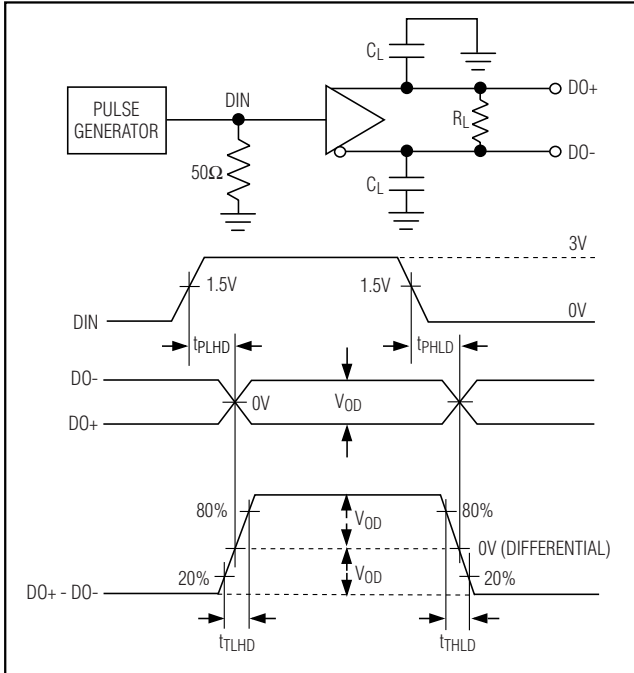


Figure 2. Driver Differential Propagation Delay and Transition Time Test Circuit and Waveforms

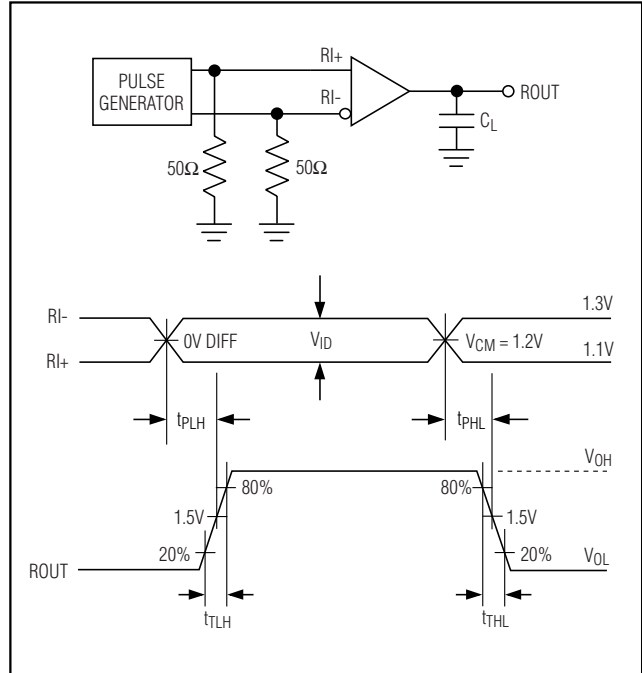


Figure 4. Receiver Propagation Delay and Transition Time Test Circuit and Waveforms

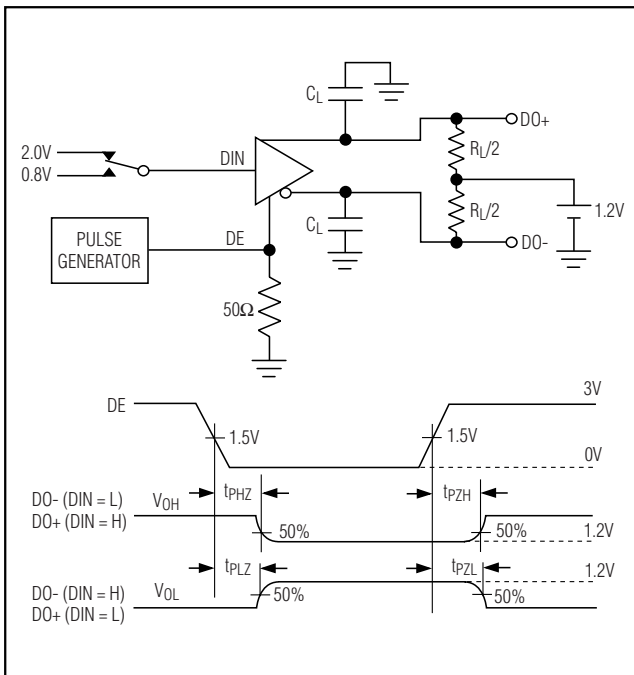


Figure 3. Driver High-Impedance Delay Test Circuit and Waveforms

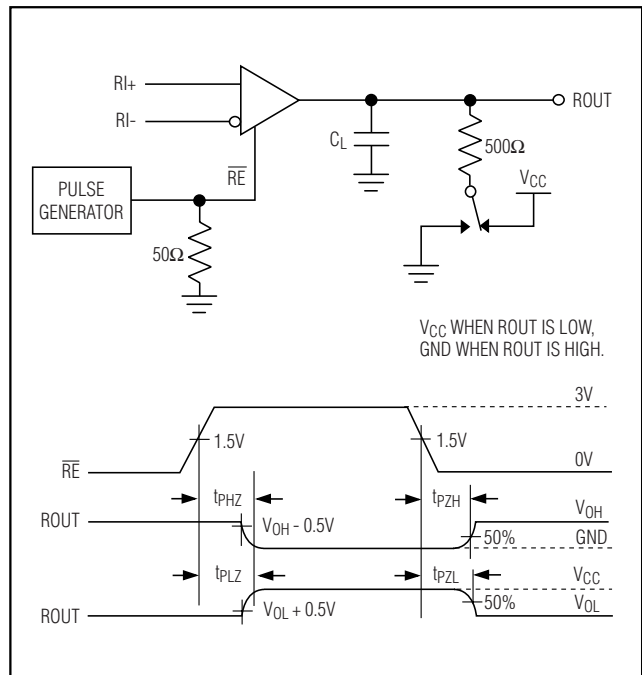


Figure 5. Receiver High-Impedance Delay Test Circuit and Waveforms

## 3.3V Single LVDS Driver/Receiver

### Detailed Description

The MAX9164 high-speed LVDS driver/receiver is designed specifically for low-power point-to-point applications. The MAX9164 operates from a single 3.3V power supply, and is pin compatible with the DS90LV019. The device features an independent differential driver and receiver.

The MAX9164 driver outputs use a current-steering configuration to generate a 3.1mA (typ) output current. This current-steering approach induces less ground bounce and no shoot-through current, enhancing noise margin and system speed performance. The outputs are short-circuit current limited. The MAX9164 output requires a resistive load to terminate the signal and complete the transmission loop. With a typical 3.1mA output current, the MAX9164 produces a 310mV output voltage when driving a bus terminated with a 100Ω resistor ( $3.1\text{mA} \times 100\Omega = 310\text{mV}$ ).

The MAX9164 receiver detects a differential input as low as 100mV and translates it to single-ended output. The device features input biasing that drives the output high if the inputs are left open.

### Power-On Reset

The power-on reset voltage of the MAX9164 is typically 2.2V. When the supply falls below this voltage, the device is disabled and the outputs (DO+, DO-, and ROUT) are high impedance.

### Applications Information

#### Power-Supply Bypassing

Bypass  $V_{CC}$  with high-frequency, surface-mount ceramic 0.1μF and 0.001μF capacitors in parallel as close to the device as possible, with the smaller valued capacitor closest to  $V_{CC}$ .

#### Termination

The MAX9164 requires an external termination resistor at the differential input. This termination resistor should match the differential impedance of the input transmission line.

The differential output requires a termination resistor at the far end of the transmission line. This termination resistor should match the differential impedance of the output transmission line.

These termination resistors are typically 100Ω. Minimize the distance between the input termination resistor and the MAX9164 receiver input.

### Traces, Cables, and Connectors

The characteristics of differential input and output connections affect the performance of the device. Use controlled-impedance traces, cables, and connectors with matched characteristic impedance.

Ensure that noise couples as common mode by running the traces of a differential pair close together. Reduce within-pair skew by matching the electrical length of the conductors within a differential pair. Excessive skew can result in a degradation of magnetic field cancellation.

Maintain the distance between conductors within a differential pair to avoid discontinuities in differential impedance. Minimize the number of vias to further prevent impedance discontinuities.

### Board Layout

For LVDS applications, a four-layer PC board with separate power, ground, LVDS, and logic signal layers is recommended. Separate the LVTTTL/LVCMOS and LVDS signals to prevent coupling.

### Chip Information

TRANSISTOR COUNT: 901

PROCESS: CMOS



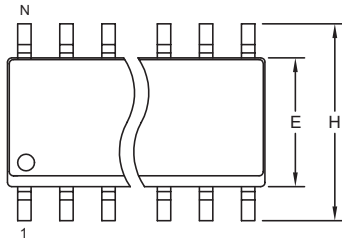
# 3.3V Single LVDS Driver/Receiver

## Package Information

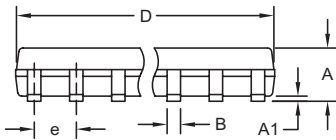
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

**MAX9164**

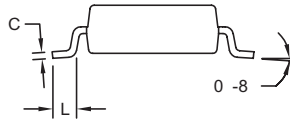
SOICN .150" EPS



TOP VIEW



FRONT VIEW



SIDE VIEW

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

VARIATIONS:

DIM	INCHES		MILLIMETERS		N	MS012
	MIN	MAX	MIN	MAX		
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC

**NOTES:**

1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

<small>PROPRIETARY INFORMATION</small>		
TITLE: <b>PACKAGE OUTLINE, .150" SOIC</b>		
APPROVAL	DOCUMENT CONTROL NO. 21-0041	REV. B 1/1

# 3.3V Single LVDS Driver/Receiver

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	—	1.10	—	.043
A <sub>t</sub>	0.05	0.15	.002	.006
A <sub>e</sub>	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b <sub>1</sub>	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c <sub>1</sub>	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC		N	VARIATIONS			
			MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

**NOTES:**

- DIMENSIONS D AND E DO NOT INCLUDE FLASH
- MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
- CONTROLLING DIMENSION: MILLIMETER
- MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
- \*N\* REFERS TO NUMBER OF LEADS
- THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [C-] IN THE DIRECTION INDICATED

TSSOP4.40mm.EPS

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<b>DALLAS SEMICONDUCTOR</b>		<b>MAXIM</b>	
PROPRIETARY INFORMATION			
TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY			
APPROVAL	DOCUMENT CONTROL NO. 21-0066	REV. F	1/1