PRELIMINARY - October 3, 2000 TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com

DESCRIPTION

The SC1153 is a low-cost, full featured, synchronous voltage-mode controller designed for use in single ended power supply applications where efficiency is of primary concern. Synchronous operation allows for the elimination of heat sinks in many applications. The SC1153 is ideal for implementing DC/DC converters needed to power advanced microprocessors, such as Pentium® III, in both single and multiple processor configurations. Internal level-shift, high-side drive circuitry, and preset shoot-thru control, allows for use of inexpensive n-channel power switches.

SC1153 features include an integrated 5-bit VID DAC, temperature compensated voltage reference, triangle wave oscillator, current limit comparator, frequency shift over-current protection, and an accessible, internally compensated error amplifier. Power good signaling, logic compatible shutdown, and over voltage protection are also provided.

The SC1153 operates at a fixed 200KHz, providing an optimum compromise between efficiency, external component size, and cost.

FEATURES

- Low cost / full featured
- Synchronous operation
- 5 Bit VID programmable output
- On-chip power good and OVP functions
- Designed to meet Intel VRM 8.4 (Pentium® III)
- 1.3V to 3.5V Range, 1% tolerance

APPLICATIONS

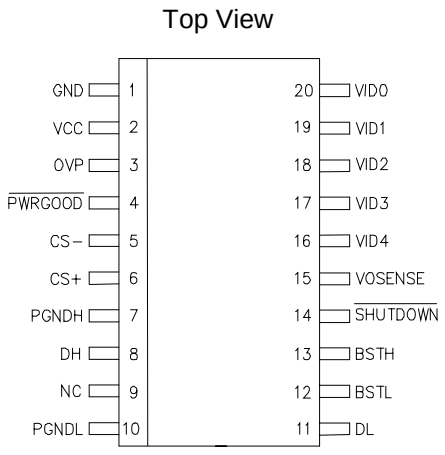
- Pentium® III Core Supply
- Multiple Microprocessor Supplies
- Voltage Regulator Modules (VRM)
- Programmable Power Supplies
- High Efficiency DC/DC Conversion

ORDERING INFORMATION

DEVICE(1)	PACKAGE	TEMP. RANGE (T_J)
SC1153CSW.TR	SO-20	0 - 125°C

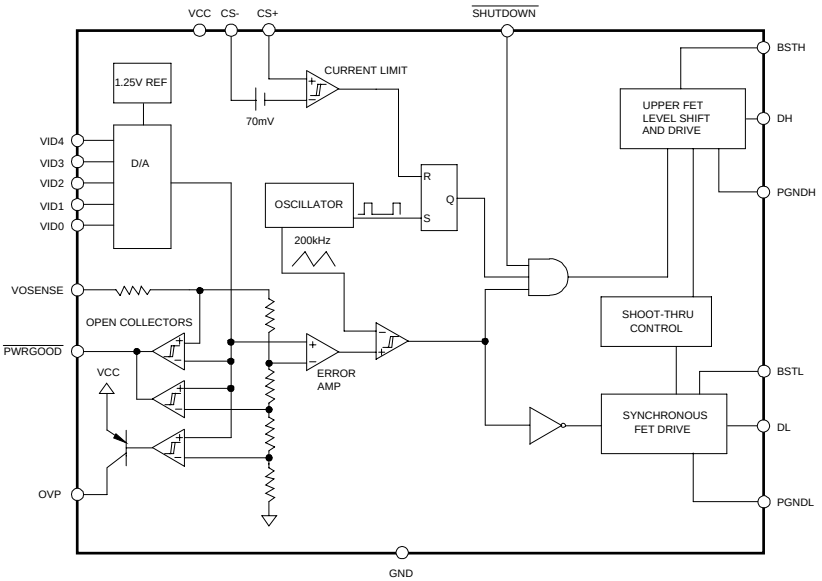
Note:
(1) Only available in tape and reel packaging. A reel contains 1000 devices.

PIN CONFIGURATION



(20-Pin SOIC)

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Maximum	Units
V_{CC} to GND	V_{IN}	-0.3 to 7	V
PGND to GND		± 1	V
BST to GND		-0.3 to 15	V
Thermal Resistance Junction to Case	θ_{JC}	30	°C/W
Thermal Resistance Junction to Ambient	θ_{JA}	90	°C/W
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 sec	T_{LEAD}	300	°C

ELECTRICAL CHARACTERISTICS

Unless specified: V_{CC} = 4.75V to 5.25V; GND = PGND = 0V; FB = V_O; 0mV < (CS(+) - CS(-)) < 60mV; T_J = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	I_O = 2A(1)	See Output Voltage Table.			
Supply Voltage	V_{CC}	4.2		7	V
Supply Current	V_{CC} = 5.0		5		mA
Load Regulation	I_O = 0.3A to 15A(1)		1		%
Line Regulation	All VID codes(1)		0.5		%
Gain (A_{OL})	V_{OSENSE} to V_O		35		dB
Current Limit Voltage		60	70	80	mV
Oscillator Frequency		180	200	220	kHz
Oscillator Max Duty Cycle		90	95		%
DH Sink/Source Current	BST_H - DH = 4.5V, DH - $PGND_H$ = 2V	1			A
DL Sink/Source Current	BST_L - DL = 4.5V, DL - $PGND_L$ = 2V	1			A
OVP Threshold Voltage			120		%
OVP Source Current	V_{OVP} = 3V	10			mA
Power Good Threshold Voltage		90		110	%
Dead Time		50	100		ns

NOTE:

(1) Specification refers to application circuit (Figure 1.).

(2) This part is ESD sensitive. Use of standard ESD handling precautions is required.

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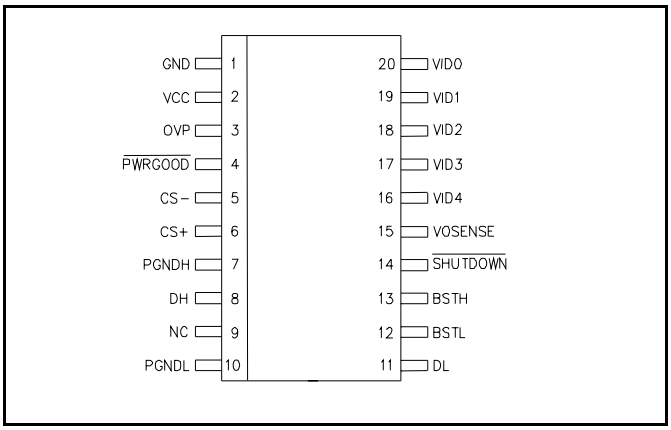
PIN DESCRIPTION

Pin #	Pin Name	Pin Function
1	GND	Small Signal Analog and Digital Ground
2	VCC	Chip Supply Voltage
3	OVP	High Signal Out if V_O > Setpoint + 20%
4	$\overline{\text{PWRGOOD}}$(1)	Open collector logic output, high if V_O within 10% of setpoint
5	CS(-)	Current Sense Input (negative)
6	CS(+)	Current Sense Input (positive)
7	PGNDH	Power Ground for High Side Switch
8	DH	High Side Driver Output
9	NC	Not Connected
10	PGNDL	Power Ground for Low Side Switch
11	DL	Low Side Driver Output
12	BSTL	Vcc for Low Side Driver (Boost)
13	BSTH	Vcc for High Side Driver (Boost)
14	$\overline{\text{SHUTDOWN}}$(1)	Logic Low shuts down the converter
15	VOSENSE	Top end of internal feedback chain
16	VID4(1)	Programming Input (MSB)
17	VID3(1)	Programming Input
18	VID2(1)	Programming Input
19	VID1(1)	Programming Input
20	VID0(1)	Programming Input (LSB)

NOTE:

(1) All logic level inputs and outputs are open collector TTL compatible.

PIN CONFIGURATION



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APPLICATION CIRCUIT

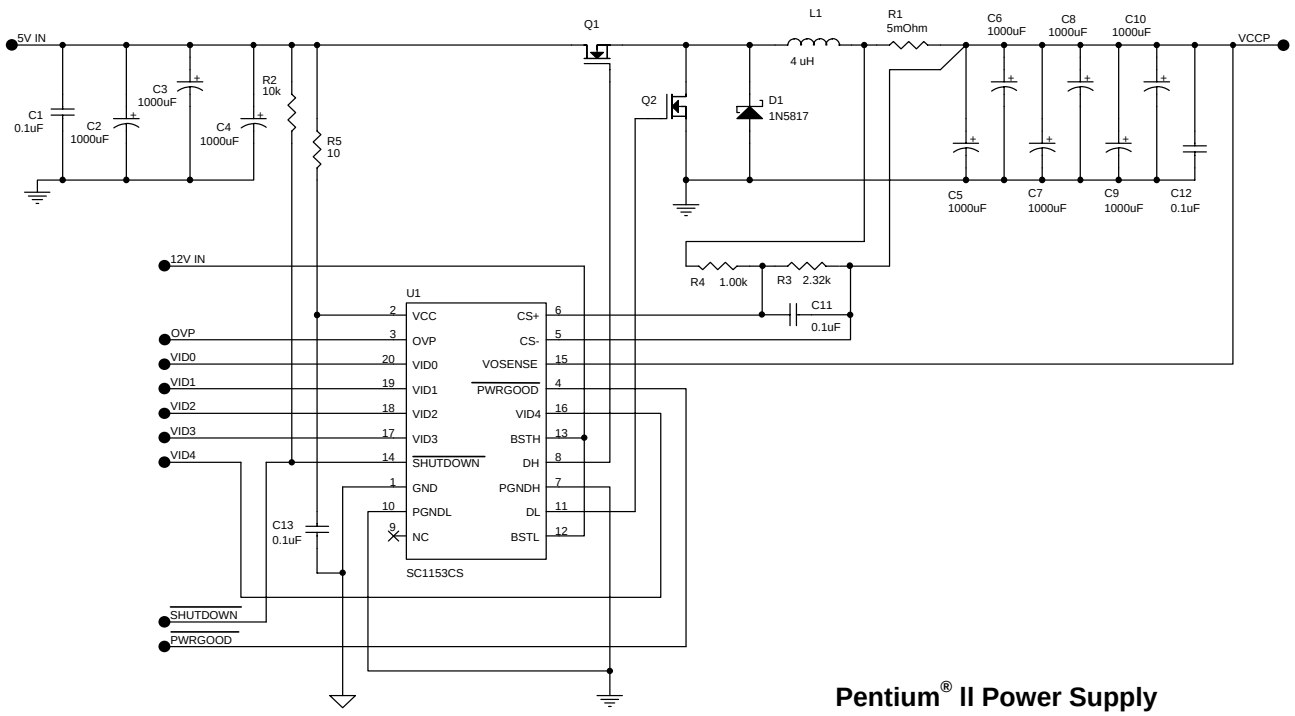

Figure 1.

MATERIALS LIST

Quantity	Reference	Part/Description	Vendor	Notes
4	C1,C11-C13	0.1µF Ceramic	Various	
9	C2-C10	1000µF/6.3V	SANYO	MV-GX or equiv. Low ESR
1	D1	1N5817	Various	
1	L1	4µH		8 Turns 16AWG on MICROMETALS T50-52D core
2	Q1, Q2	See notes	See notes	FET selection requires trade-off between efficiency and cost. Absolute maximum $R_{DS(ON)}$ = 22 mΩ
1	R1	5mΩ	IRC	OAR-1 Series
1	R2	10kΩ, 5%, 1/8W	Various	
1	R3	2.32kΩ, 1%, 1/8W	Various	
1	R4	1kΩ, 1%, 1/8W	Various	
1	R5	10Ω, 5%, 1/8W	Various	
1	U1	SC1153CS	SEMTECH	

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OUTPUT VOLTAGE TABLE

Unless specified: V_{CC} = 5.00V; GND = PGND = 0V; FB = V_O; 0mV < (CS(+) - CS(-)) < 60mV; T_J = 25°C

PARAMETER	CONDITIONS	VID 43210	MIN	TYP	MAX	UNITS
Output Voltage	I_O = 2A in Application Circuit (Figure 1)	01111	1.287	1.300	1.313	V
		01110	1.336	1.350	1.364	
		01101	1.386	1.400	1.414	
		01100	1.435	1.450	1.465	
		01011	1.485	1.500	1.515	
		01010	1.534	1.550	1.566	
		01001	1.584	1.600	1.616	
		01000	1.633	1.650	1.667	
		00111	1.683	1.700	1.717	
		00110	1.732	1.750	1.768	
		00101	1.782	1.800	1.818	
		00100	1.832	1.850	1.868	
		00011	1.881	1.900	1.919	
		00010	1.931	1.950	1.969	
		00001	1.980	2.000	2.020	
		00000	2.030	2.050	2.070	
		11111	1.980	2.000	2.020	
		11110	2.079	2.100	2.121	
		11101	2.178	2.200	2.222	
		11100	2.277	2.300	2.323	
		11011	2.376	2.400	2.424	
		11010	2.475	2.500	2.525	
		11001	2.574	2.600	2.626	
		11000	2.673	2.700	2.727	
		10111	2.772	2.800	2.828	
		10110	2.871	2.900	2.929	
		10101	2.970	3.000	3.030	
		10100	3.069	3.100	3.131	
		10011	3.168	3.200	3.232	
		10010	3.267	3.300	3.333	
		10001	3.366	3.400	3.434	
		10000	3.465	3.500	3.535	

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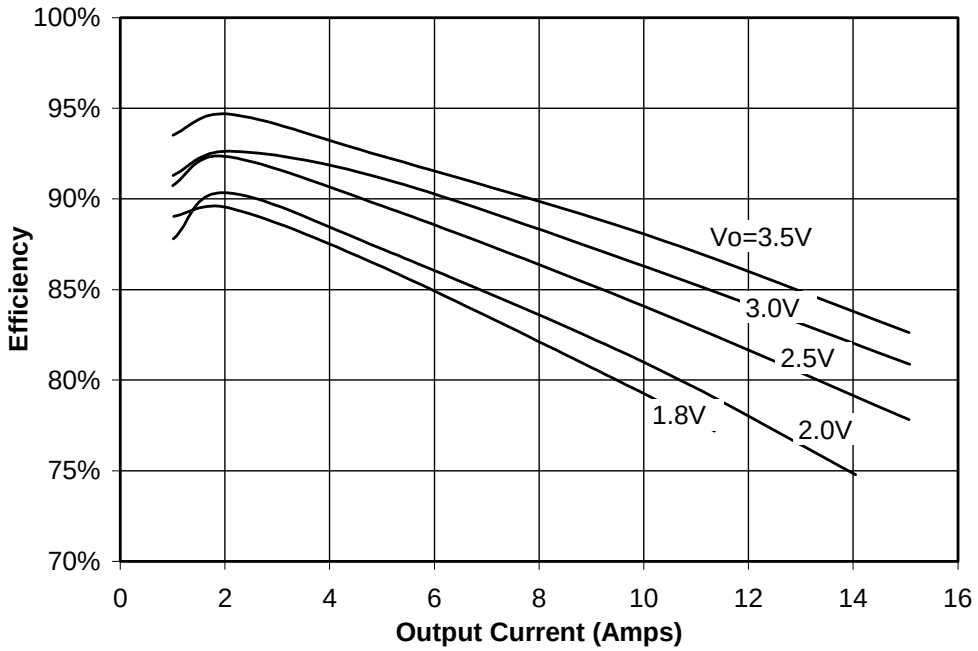
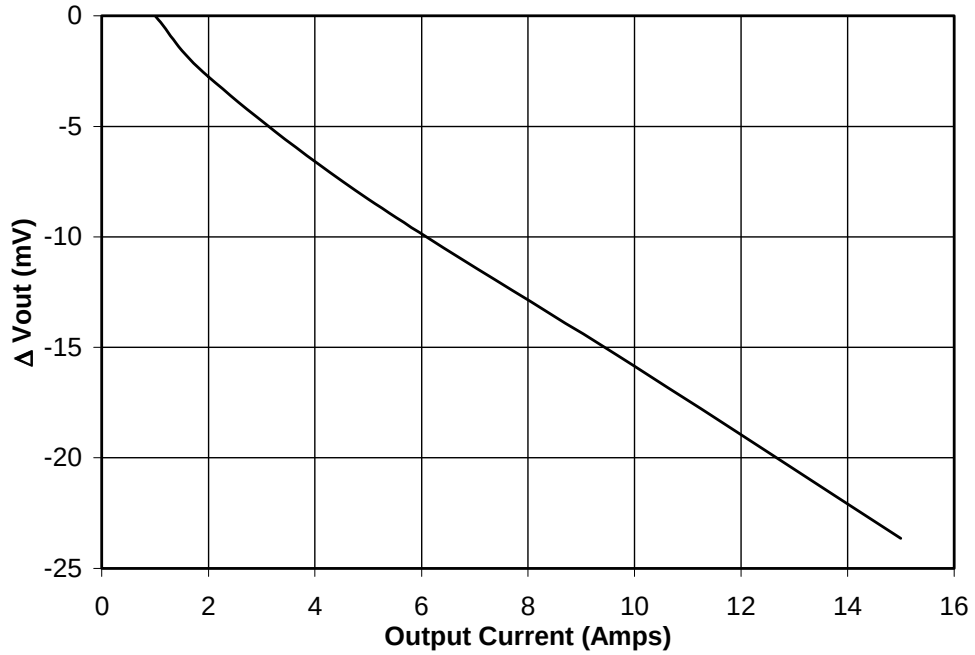
CHARACTERISTIC CURVES

SC1153 Efficiency in Application Circuit (Figure 1).



SC1153 Regulation in Application Circuit (Figure 1).



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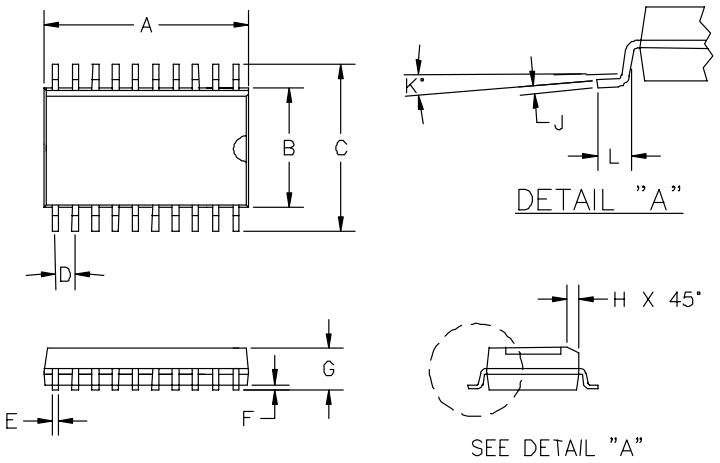
OUTLINE DRAWING SO-20



DIMENSIONS (1)					
DIMN	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.496	.512	12.6	13.0	(2)
B	.291	.299	7.40	7.60	(2)
C	.394	.419	10.0	10.65	–
D	.050	BSC	1.27	BSC	–
E	.013	.020	0.33	0.51	–
F	.004	.012	.10	.30	–
G	.092	.104	2.35	2.65	–
H	.010	.030	.25	.75	–
J	.009	.013	.23	.32	–
K	0°	8°	0°	8°	–
L	.016	.050	.40	1.27	–

(2) DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTUSIONS
(1) CONTROLLING DIMENSION : MILLIMETERS.

Ref. MS-013AC

THEORY OF OPERATION

The voltage at the VOSENSE pin is applied, through the internal precision resistor feedback chain, to the inverting input of the error amplifier. The non-inverting input of the error amplifier is supplied with a DC voltage derived by the DAC from the internal trimmed bandgap voltage reference. The output of the error amplifier is compared to the triangular output of the internal oscillator to generate a fixed frequency, variable duty cycle pulse train. The internal oscillator uses an on-chip capacitor and precision trimmed current sources to set the frequency to 200kHz.

The generated pulse train is gated with the output of the current limit latch and the inhibit signal to produce a drive signal for the upper FET. It is also inverted to produce a drive signal for the lower FET. These FET drive signals are modified by the “shoot-through control” circuitry so that the top FET turn-on is delayed until the bottom FET has turned off, and visa-versa.

The current limit latch is set (ending the upper FET drive pulse early) if the current limit comparator indicates an overcurrent condition. The latch is reset at the start of each oscillator period.

The $\overline{\text{PWRGOOD}}$ and OVP signals are derived from the voltage at the VOSENSE pin by comparators fed from the internal feedback chain.

ECN00-1346