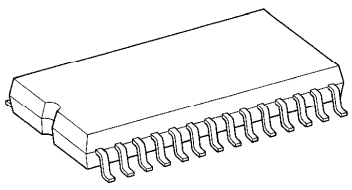
TENTATIVE TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9271F, TC9271N

MODULATION / TRANSMISSION IC FOR DIGITAL AUDIO INTERFACE

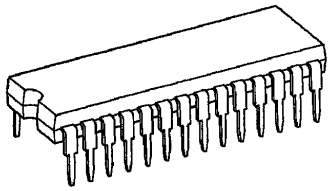
TC9271F and TC9271N are modulation / transmission ICs for digital audio interface based on EIAJ CP-1201 standards.

TC9271F



SOP28-P-450-1.27

TC9271N



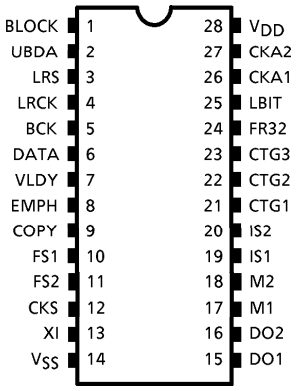
SDIP28-P-400-1.78

Weight
SOP28-P-450-1.27 : 0.8g (Typ.)
SDIP28-P-400-1.78 : 2.2g (Typ.)

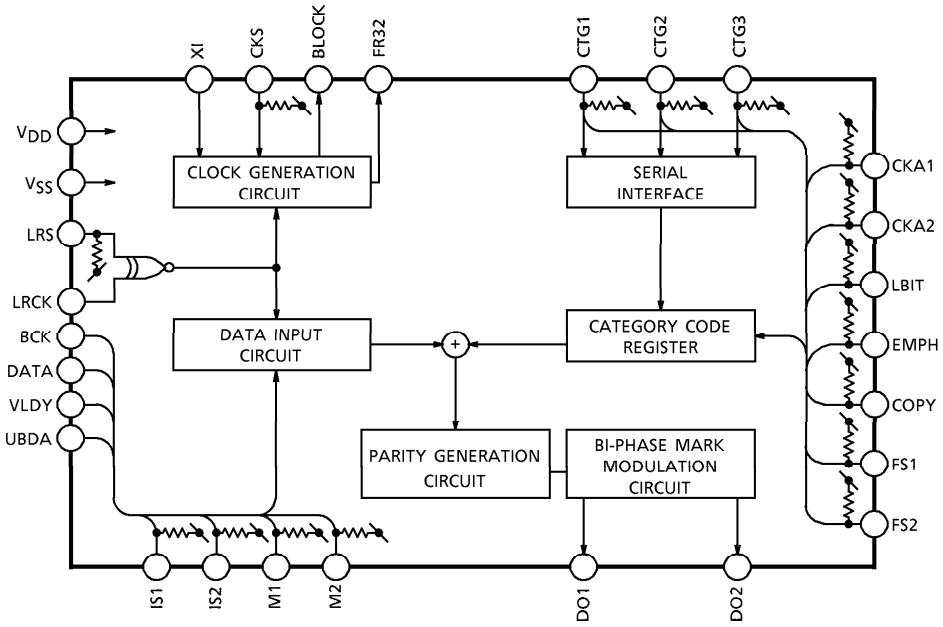
FEATURES

- Based on EIAJ CP-1201 standards.
- Data input format selectable between MSB first or LSB first. Data length is 24bit max.
- Two modes : 2 channel and 4 channel
- Channel status data easily set with external pins. The data can be input serially by microcontroller.
- User data can be transmitted.
- Double-speed operation
- Selectable LRCK polarity
- Two packages : 28-pin flat package, 28-pin shrink DIP package

PIN CONNECTION



BLOCK DIAGRAM



PIN FUNCTION

PIN No.	SYMBOL	I / O	FUNCTION	REMARKS
1	BLOCK	O	Block top position output pin	
2	UBDA	I	User bit data input pin	
3	LRS	I	LRCK polarity selection pin LRS: L level → R channel data / L channel data; H level → L channel data / R channel data	With pull-up resistor
4	LRCK	I	LR clock input pin	
5	BCK	I	Bit clock input pin	
6	DATA	I	2ch: Data input pin / 4ch: Data input pin 1	
7	VLDY	I	2ch: Correction flag input pin / 4ch: Data input pin 1	
8	EMPH	I	Emphasis flag setting pin	With pull-up resistor
9	COPY	I	P: Copy flag setting pin / S: Fixes to high.	With pull-up resistor
10	FS1	I	Sampling frequency setting pin 1	With pull-up resistor
11	FS2	I	Sampling frequency setting pin 2	With pull-up resistor
12	CKS	I	Clock divider selection pin	With pull-up resistor
13	XI	I	Clock input pin	
14	V_{SS}	—	Ground pin	
15	DO1	O	Digital data output pin 1	
16	DO2	O	Digital data output pin 2	
17	M1	I	Channel mode setting pin 1 / Select 2ch or 4ch mode.	With pull-up resistor
18	M2	I	Channel mode setting pin 2	With pull-up resistor
19	IS1	I	Data input mode setting pin 1	With pull-up resistor
20	IS2	I	Data input mode setting pin 2	With pull-up resistor
21	CTG1	I	P: Category code setting pin 1 / S: Data input pin	With pull-up resistor
22	CTG2	I	P: Category code setting pin 2 / S: Clock input pin	With pull-up resistor
23	CTG3	I	P: Category code setting pin 3 / S: Latch pulse input	With pull-up resistor
24	FR32	O	FR32 output pin	
25	LBIT	I	P: LBIT input pin / S: 32 / 192bit switching pin	With pull-up resistor
26	CKA1	I	P: Clock accuracy setting pin 1 / S: Fixes to high.	With pull-up resistor
27	CKA2	I	P: Clock accuracy setting pin 2 / S: Prohibits output at high level.	With pull-up resistor
28	V_{DD}	—	Power supply pin	

(Note) In the above pin description, "2ch" indicates 2 channel mode; "4ch", 4 channel mode. "P" indicates parallel mode; "S", serial mode. For mode settings, use FS1 (pin 10) and FS2 (pin 11).

OPERATIONAL DESCRIPTION

1. Internal mode setting

1-1. 2ch mode and 4ch mode setting

To switch between 2ch mode and 4ch mode, use both the M1 and M2 pins.
The 4ch mode is further divided into two modes. In one mode, data are output from two channels from both output pins, DO1 and DO2. In the other mode, data are output from four channels from one output pin (DO1 output = DO2 output).
Two modes are also supported for inputting data. In the first mode, two channels of data are input from two input pins, DATA and VLDY. In the second mode, four channels of data are input from one input pin.

Table 1 2 Channel and 4 Channel Mode Setting

MODE SETTING		INPUT SIGNAL				OUTPUT SIGNAL		Comment
M2 PIN	M1 PIN	LRCK PIN	BCK PIN	DATA PIN	VLDY PIN	DO2 PIN	DO1 PIN	
L	L	Lrck	Bck	Din1	Valid	Din1	Din1	2ch mode
L	H	Lrck	Bck	Din1	Din2	Din2	Din1	
H	L	Lrck	Bck	Din1	Din2	Din1 + 2	Din1 + 2	
H	H	Frck	Bck	Din1 + 2	Wdck	Din1 + 2	Din1 + 2	

(Note) Adding validity flag
A validity flag can be added in 2 channel mode. However, in 4 channel mode, the flag is fixed to low, as VLDY (pin 7) functions as a data or clock input pin in this mode.

The signals in Table 1 are as follows.

Lrck	:	Left channel and right channel selection clock
Bck	:	Bit clock
Frck	:	Frame clock (4 channel mode)
Valid	:	Validity flag
Wdck	:	Word clock (4 channel mode)
Din1, Din2	:	2 channel multiplexed input data
Din1 + 2	:	4 channel multiplexed input data
Dit1, Dit2	:	2 channel multiplexed output data
Dit1 + 2	:	4 channel multiplexed output data

1-2. Data input mode setting

Two data input modes are supported : LSB-first mode and MSB-first mode. Effective data are assumed to be before the change point of LRCK. However, MSB-first mode supports three input data bit length settings.
Table 2 shows the data input modes. In modes where up to 24bit can be input, input the unused bits fixed to 0.

Table 2 Data Input Modes

SELECTION SIGNAL		INPUT FORMAT			
IS2 PIN	IS1 PIN	INPUT FORMAT	DATA POSITION	NUMBER OF BITS	NUMBER OF BCK
L	L	LSB first	A	24 max.	At least 24 clocks / ch
L	H	MSB first	B	24 max.	32 clocks / ch
H	L		A	20	At least 20 clocks / ch
H	H		A	16	At least 16 clocks / ch

A : Effective data before the change point of LRCK .
B : Effective data after the change point of LRCK .

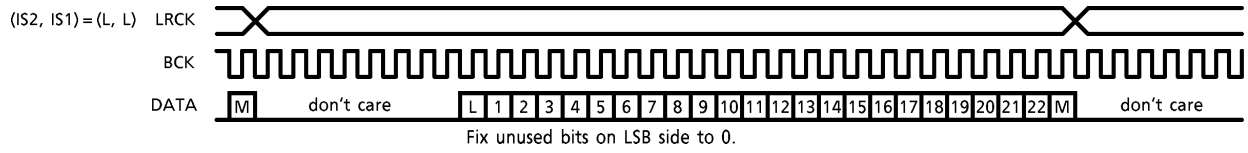


Figure 1a Data Input Format Example 1
((IS2, IS1) = (L, L); effective data before the change point of LRCK, 24bit / ch max.)

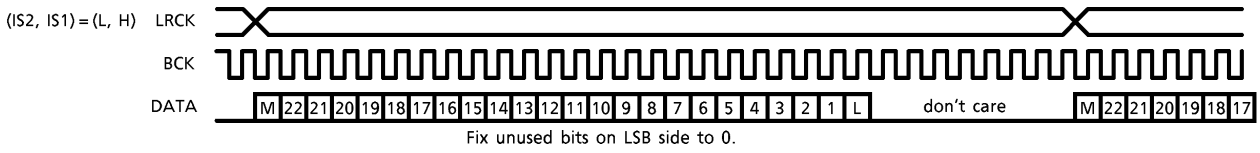


Figure 1b Data Input Format Example 2
((IS2, IS1) = (L, H); effective data after the change point of LRCK, 24bit / ch max.)

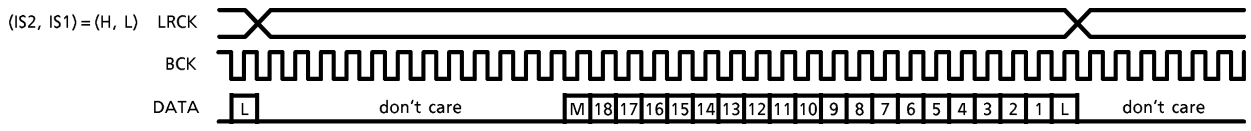


Figure 1c Data Input Format Example 3
((IS2, IS1) = (H, L); effective data before the change point of LRCK, 20bit / ch)

Figure 1d Data Input Format Example 4
((IS2, IS1) = (H, H); effective data before the change point of LRCK, 16bit / ch)

1-3. User bits and validity flag input format

Synchronize the user bits and validity flag with the audio data. Because the validity input pin (VLDY) is used as a data or word clock input pin in other than 2 channel mode, the output data validity flag is fixed to 0.
Figure 2 shows the input timings.

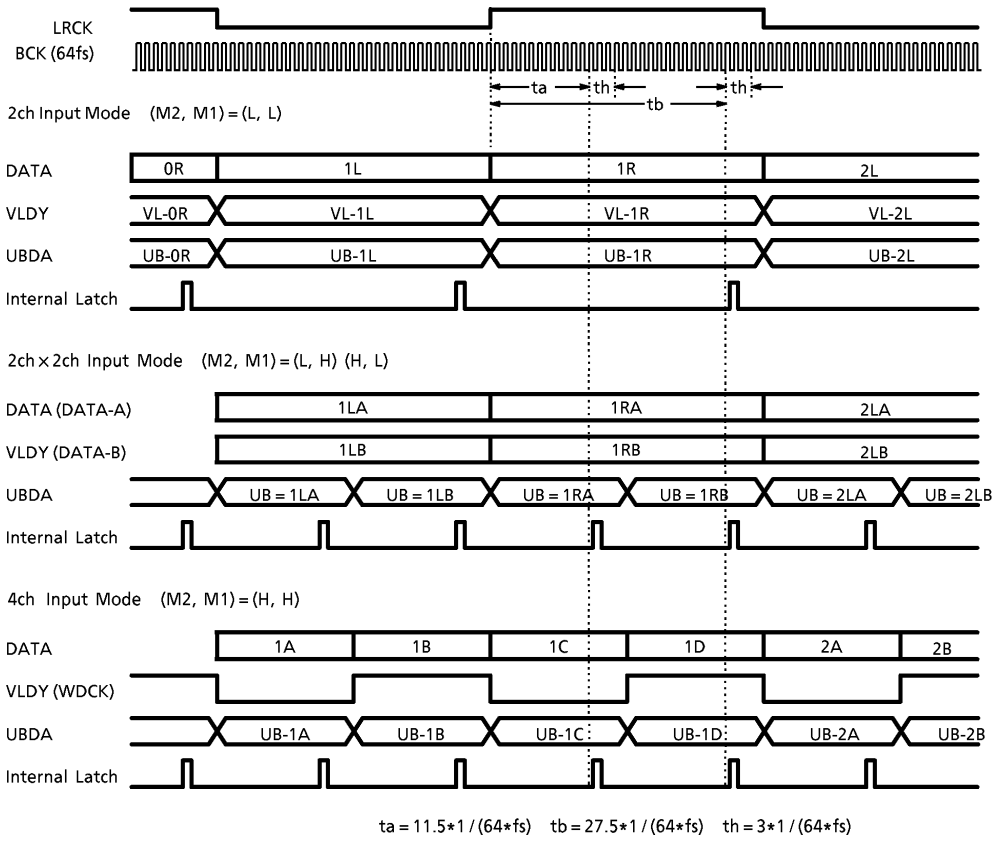


Figure 2 V and U Bit Input Timing Chart

1-4. LR clock polarity setting

The LRCK input polarity can be switched using the LRS pin. In 4 channel mode, when the LRCK polarity is reversed, the Frck (frame clock) and Wdck (word clock) polarities are also reversed, as in Figure 3b.

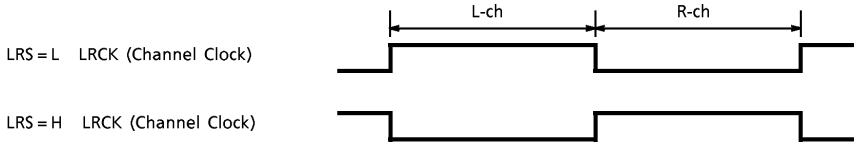


Figure 3a LRCK Polarity Setting Example in 2ch Mode

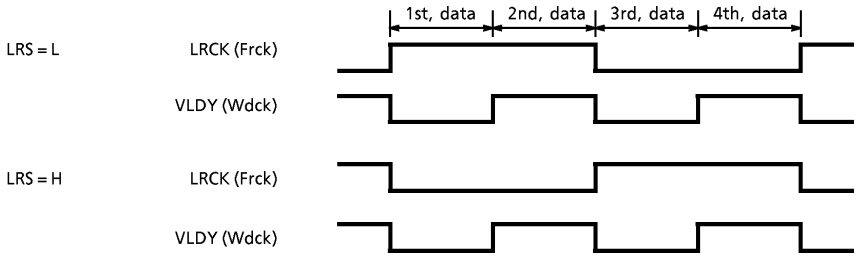


Figure 3b LRCK Polarity Setting Example in 4ch Mode

1-5. System clock setting

The CKS pin is used to divide the clock input from XI by two is set. It is possible to compare the phase of the clock input to LRCK with the phase of the internal divided clock to automatically determine whether the clock input from the XI pin is a 256fs- or a 384fs-type clock.

Table 4 Clock Divider Setting

CKS PIN	CLOCK INPUT FROM XI PIN
L	256fs / 384fs
H	512fs / 768fs

(Note) "fs" is the sampling frequency.
When the 384fs-type clock is input with CKS = low, the duty cycle must be controlled.

1-6. Data input / output formats

When LRS = high, the input / output formats depending on mode are as follows.

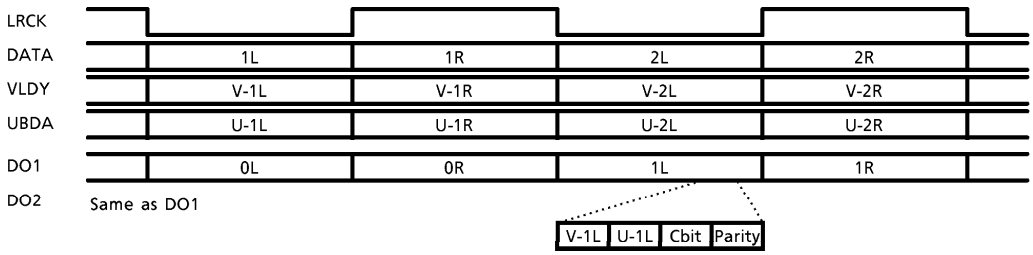


Figure 4a Data Input / Output Format Example 1 ((M2, M1) = (L, L) ; 2ch input, 2ch output mode)

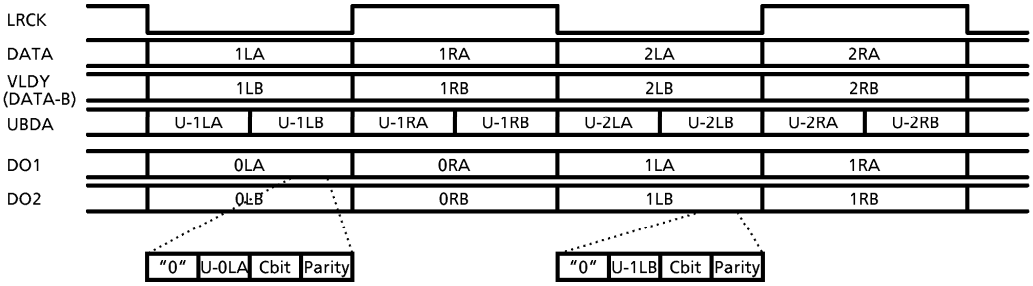


Figure 4b Data Input / Output Format Example 2 ((M2, M1) = (L, H) ; 2ch × 2 input, 2ch × 2 output mode)

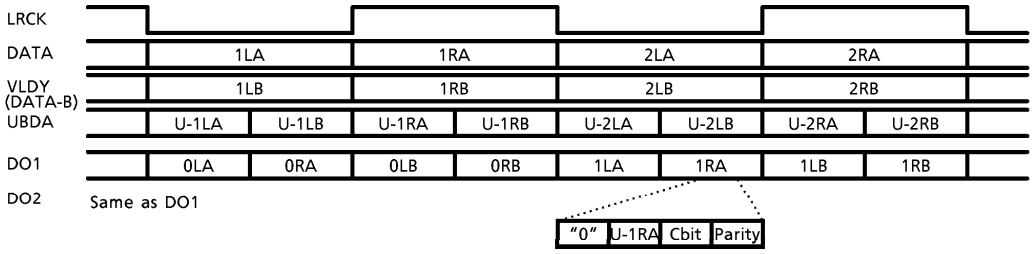


Figure 4c Data Input / Output Format Example 3 ((M2, M1) = (H, L) ; 2ch × 2 input, 4ch output mode)

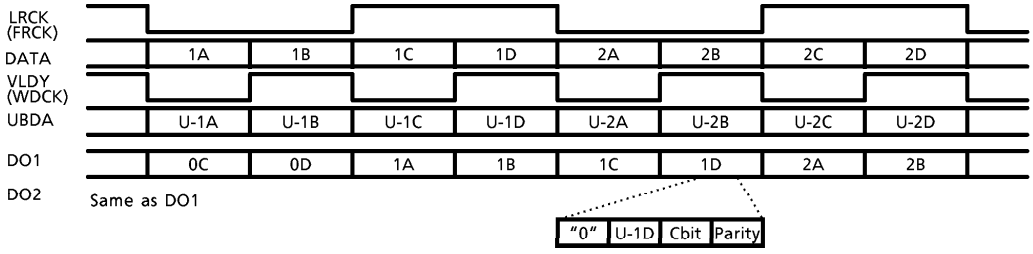


Figure 4d Data Input / Output Format Example 4 ((M2, M1) = (H, H) ; 4ch input, 4ch output mode)

2. Channel status setting

The channel status can be set by two methods. The first method is parallel DC setting. The second method is serial setting using a microcontroller. (Table 7)
The EMPH flag in channel status is set to the OR of the parallel data and the serial data in serial mode.

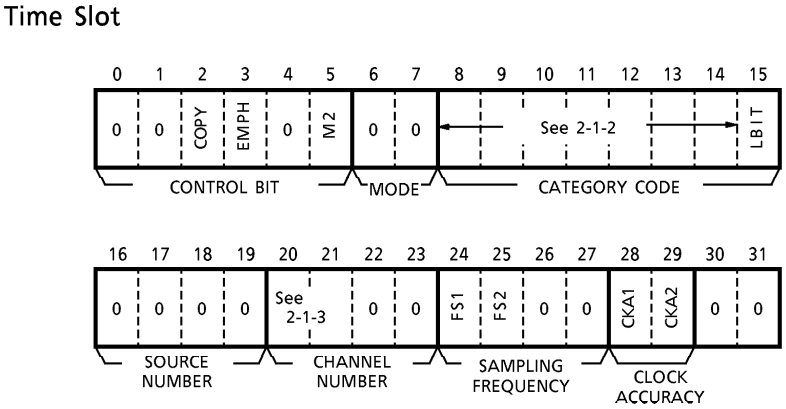


Figure 5 Channel Status Bit Correspondence

2-1. Parallel mode

This mode is used to make parallel DC setting of the channel status.
Figure 5 shows the bits which can be set. In Figure 5, "0" indicates that the bit is fixed to 0. Accordingly, in home digital audio equipment, the mode is fixed to 00 and the source number to 0000.

2-1-1. Control bit setting ;

Fixing three of the six control bits to 0 results in the following limitations.

(a) Time Slot 0 = 0 ; Only for home equipment
(b) Time Slot 1 = 0 ; Only for audio data
(c) Time Slot 4 = 0 ; Only for fixing emphasis to 50 / 15μs

Bits other than these can be DC-set directly from the pin.

(a) Time Slot 2 = COPY ; When COPY pin = H, no copy protection
When COPY pin = L, copy protection (Copying inhibited)
(b) Time Slot 3 = EMPH ; When EMPH pin = H, emphasis is 50 / 15
When EMPH pin = L, no emphasis
(c) Time Slot 5 = M2 ; For 2 channel output per output pin, set to two channels
For 4 channel output per output pin, set to four channels

2-1-2. Category code setting ;

The category code is set using pins CTG1~3.
The category bits shown in Table 5 as "L" can be freely set using the LBIT pin. For details, refer to the EIAJ CP-1201 standards.

Table 5 Category Code Setting

CTG			CATEGORY	
3	2	1		
0	0	0	General format	[000 00000]
		1	Digital mixer	[010 0100L]
	1	1	Sample rate converter	[010 1100L]
		0	Digital sampler	[010 0010L]
1	0	1	ADC (no copy right)	[011 0000L]
		0	ADC (copy right)	[011 0100L]
	1	0	Synthesizer	[101 0000L]
		1	Microphone	[101 1000L]

2-1-3. Channel number setting ;

In 2 channel mode, the channel number is added automatically. In 4 channel mode, all the bits are fixed to 0.
Table 6 shows the specific details.

Table 6 Channel Number Addition Correspondence

PIN NAME			CHANNEL NUMBER	
M2	M1	LRCK	LRS = H	LRS = L
L	L	L	[1000]	[0100]
		H	[0100]	[1000]
L	H	L	[1000]	[0100]
		H	[0100]	[1000]
Other combinations			[0000]	

2-1-4. Sampling frequency setting ;

Pins FS1 and FS2 are used for setting the sampling frequency.

Table 7 Sampling Frequency Setting

PIN INPUT		SETTING DATA		SETTING MODE (PINS CTG1~3, LBIT, CKA1~2)
FS1	FS2	SAMPLING FREQUENCY	[TS24-27]	
L	L	44.1kHz	[0000]	Parallel mode
L	H	48kHz	[0100]	
H	H	32kHz	[1100]	
H	L	Setting by serial data transfer		Serial mode

(Note) When FS1 = high and FS2 = low, serial mode is set. Thus, the mode becomes momentarily serial mode when the sampling frequency switches, momentarily disturbing clocks and data.

2-1-5. Clock accuracy bit setting ;

Use the CKA1 and CKA2 pins to set the clock accuracy. The following describes the modes.

(a) Standard mode (level Ⅱ) ;
When setting to output disable mode, change CKA1 and CKA2 from low to high.

(b) Variable pitch mode (level Ⅲ) ;
When setting to output disable mode, change CKA1 only from low to high and keep CKA2 high.

(c) Accuracy mode (level Ⅰ) ;
When setting to output disable mode, change CKA2 only from low to high and keep CKA1 high.

Table 8 Clock Accuracy Setting

PIN INPUT		SETTING DATA		DO1, DO2 OUTPUT STATUS
CKA1	CKA2	CLOCK ACCURACY	[TS28, 29]	
L	L	Level Ⅱ	[00]	Normal output
L	H	Level Ⅲ	[01]	
H	L	Level Ⅰ	[10]	
H	H	DO1 and DO2 output fixed to low (output disable mode)		

(Note) When (CKA1, CKA2) = (H, H), output disable mode for digital data is entered, and DO1 and DO2 output is fixed to low.

2-2. Serial mode

This mode is used to serially set data for the channel status using a microcontroller.
As Table 9 shows, in serial mode some pin functions differ from those in parallel mode.

Table 9 Pin Functions in Serial Mode

PIN NAME	FUNCTION	REMARKS	
EMPH	EMPH flag input	The flag is set based on the OR of EMPH and serial data.	
COPY	— (Fixed to high)		
FS1	— (Fixed to high)	Set for serial mode	
FS2	— (Fixed to low)		
CTG1	Data input		Channel status processing
CTG2	Clock input		
CTG3	Latch pulse input		
LBIT	32 / 192bit switching	Set to low for 192bit mode	
CKA1	— (Fixed to high)		
CKA2	DO1 / 2 output setting	Set to high to disable DO1 and DO2 pin output.	

(Note 1) As channel status data, the EMPH flag uses the OR of the parallel data and serial data.

(Note 2) The channel number (TIME SLOT 20 and 21 in Figure 5) is automatically set. (Effective only in 2 channel mode. (M2 pin = low))

(Note 3) The serial setting register consists of 32bit. To reset (clear) this register at power on, set to parallel mode. That is, fixing FS2 to low, set the FS1 pin to low at power on then to high.

2-2-1. Channel status input ;

The 32 and 192bit input modes are supported to serially input the channel status.

(1) 32bit input ; (LBIT = high)

This mode is used to input only 32bit from the start of the channel status.
The timing of the data is conditioned to make them effective from the next block.

(2) 192bit input ; (LBIT = low)

This mode is used to input all 192 channel status bits.
Input 192bit (32 × 6) data in sync with the FR32 and BLOCK signals. Because the internal register consists of 32bit, input 32bit data before the FR32 falling edge.
In this mode, 0~31 frames of input data are input while BLOCK output is high. Figure 6 is an input timing example.

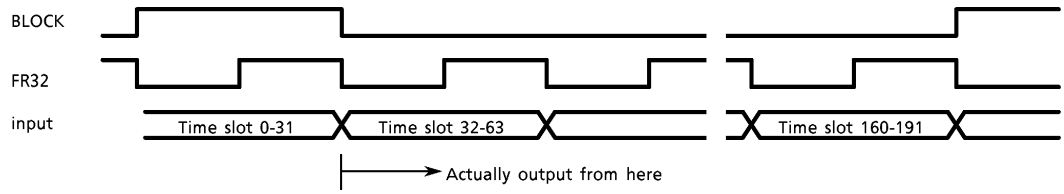


Figure 6 192Bit Input Timing Example

2-2-2. Serial Interface

The serial interface processes data, clocks, and latch signals. Figure 7 shows an example of serial interface timing.

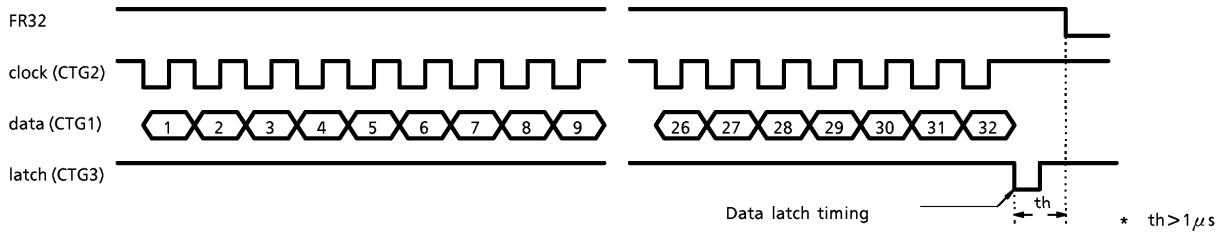


Figure 7 Serial Interface Timing Example

Data are latched at the clock rising edge.
In 192bit input mode, data are latched to the internal registers at each falling edge of FR32. Accordingly, input the data between the FR32 falling edge and the next falling edge. An interval of at least 1μs is required between the latch signal and the FR32 falling edge.

MAXIMUM RATINGS (Ta = 25°C)

ITEM		SYMBOL	RATING	UNIT
Power Supply Voltage		V_{DD}	−0.3~7.0	V
Input Voltage		V_{in}	−0.3~V_{DD} + 0.3	V
Power Dissipation	TC9271F	P_D	600	mW
	TC9271N		800	
Operating Temperature		T_{opr}	−35~85	°C
Storage Temperature		T_{stg}	−55~150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = 25°C, V_{DD} = 5V)
DC characteristics

ITEM		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Power Supply Voltage		V_{DD}	—	Ta = −35~85°C	4.5	5.0	5.5	V
Current Consumption		I_{DD}	—	XI = 16.9MHz CKS = low level	—	5	15	mA
Input Voltage	"H" Level	V_{IH}	—	(*1)	V_{DD} × 0.8	—	V_{DD}	V
	"L" Level	V_{IL}	—	(*1)	0.0	—	V_{DD} × 0.2	
Input Current	"H" Level	I_{IH}	—	(*1), $V_{IN} = V_{DD}$	—	—	1.0	μA
	"L" Level	I_{IL}	—	(*2), V_{IN} = 0V	−1.0	—	—	
Output Current	"H" Level	I_{OH}	—	(*3), V_{OH} = 4.5V	—	—	−1.6	mA
	"L" Level	I_{OL}	—	(*3), V_{OL} = 0.5V	3.0	—	—	
Pull-up Resistance		RUP	—	(*4)	—	100	—	kΩ

(*1) All input pins
(*2) All input pins other than (*4)
(*3) All output pins
(*4) All pins with pull-up resistor

AC characteristics

ITEM	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Frequency	f_{opr}	—		7.5	16.9	40.0	MHz
Input Frequency	f_{LR}	—	LRCK duty cycle = 50%	30.0	44.1	100.0	kHz
	f_{BCK}		BCK duty cycle = 50%	0.96	1.41	6.40	MHz
Rising Time	t_r	—	Pins LRCK, BCK, DATA, and XI	—	—	15	ns
Falling Time	t_f		(10~90%)	—	—	15	
Delay Time	t_d	—	BCK falling edge →LRCK, DATA	—	—	40	

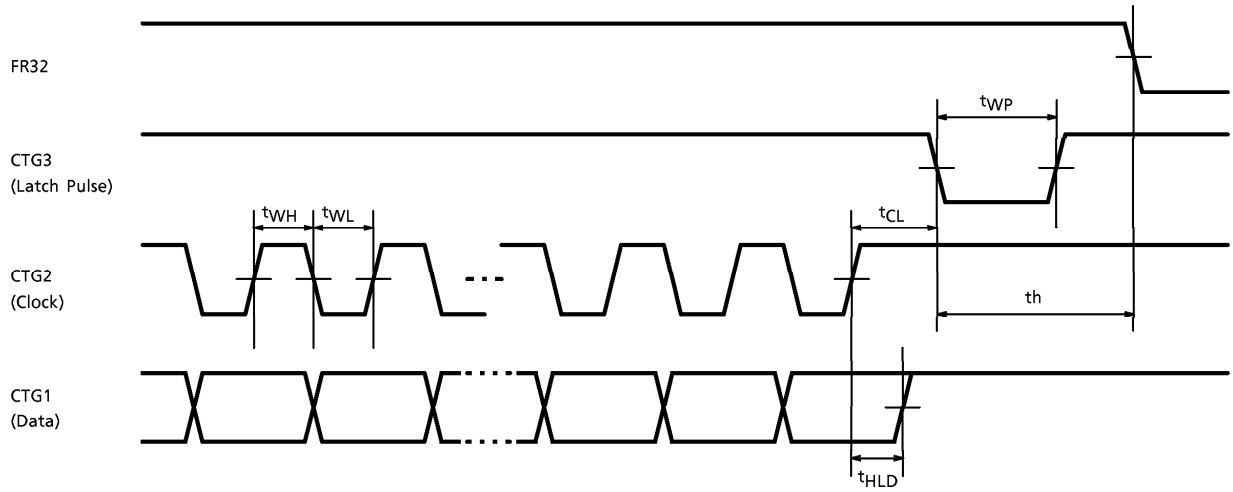
(1) Clock and data output timings

ITEM	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rising Time	t_{or}	—	Pins BLOCK, DO1, DO2, and FR32 (10~90%)	—	—	20	ns
Output Falling Time	t_{of}			—	—	20	

(2) Microcontroller interface timing (in serial mode)

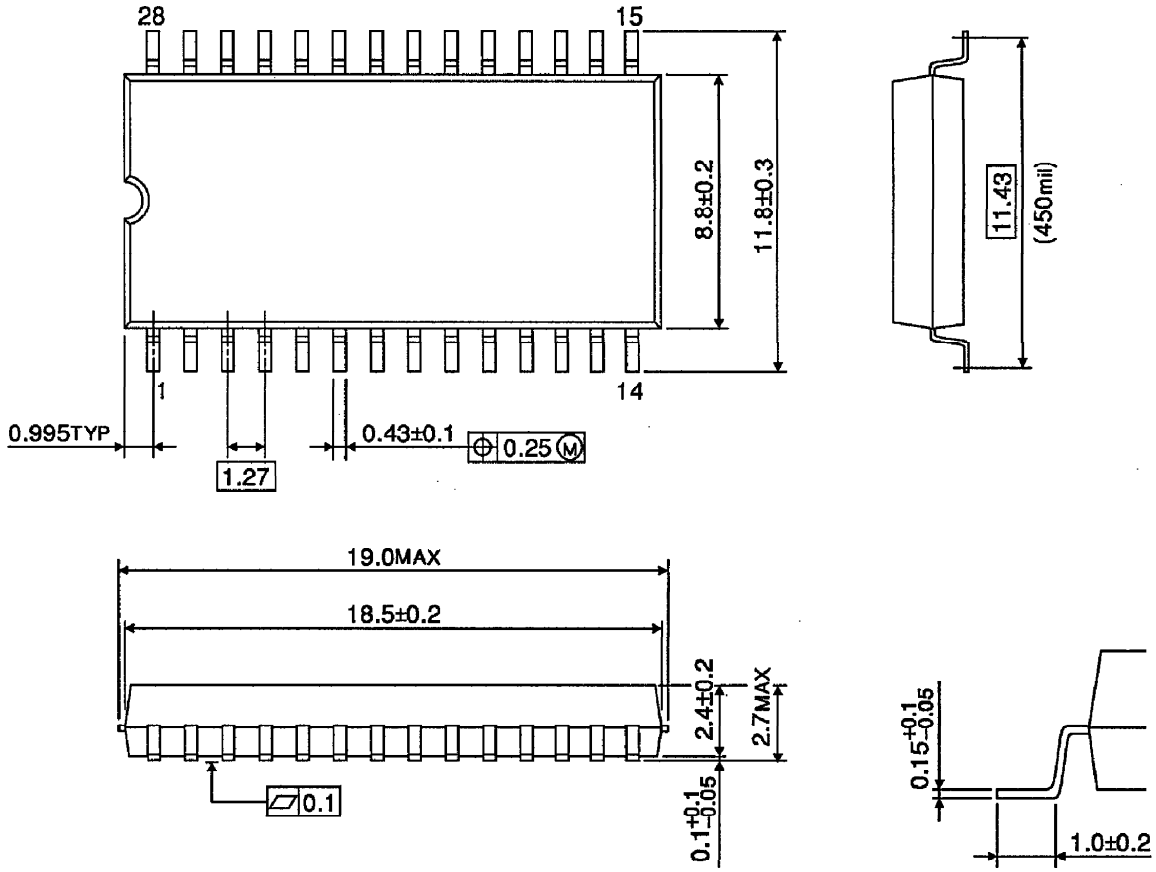
ITEM		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Strobe Pulse Width		t_{WP}	—	CTG3	0.5	—	—	μs
Clock Pulse Width	"H" Level	t_{WH}	—	CTG2	1.0	—	—	
	"L" Level	t_{WL}	—	CTG2	1.0	—	—	
Hold Time		t_{HLD}	—	CTG1→CTG2	0.5	—	—	
Delay Time		t_{CL}	—	CTG2→CTG3	0.5	—	—	

(*5) In 192bit serial input mode, set th > 1μs.
(*6) Input data in sync with the clock falling edge.
Data are loaded internally at the clock rising edge.



OUTLINE DRAWING

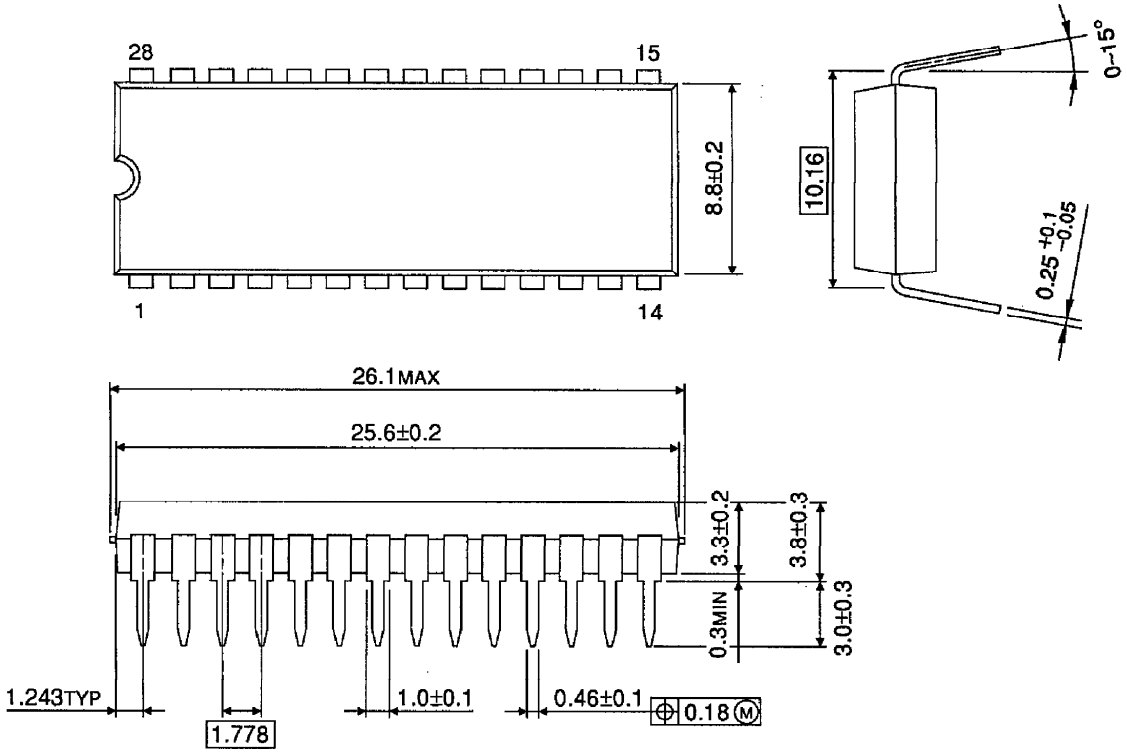
SOP28-P-450-1.27 Unit : mm



Weight : 0.8g (Typ.)

OUTLINE DRAWING

SDIP28-P-400-1.78 Unit : mm



Weight : 2.2g (Typ.)