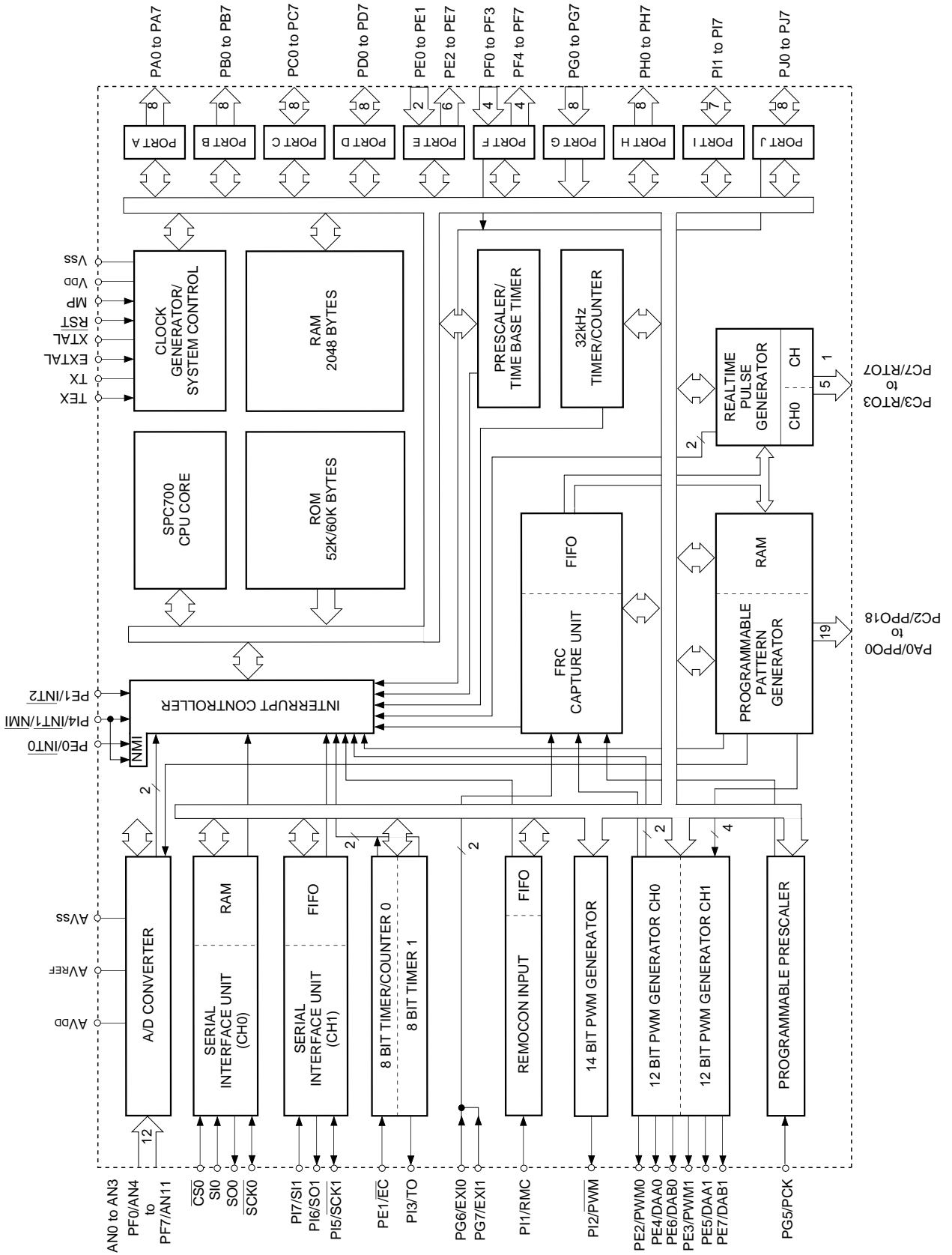
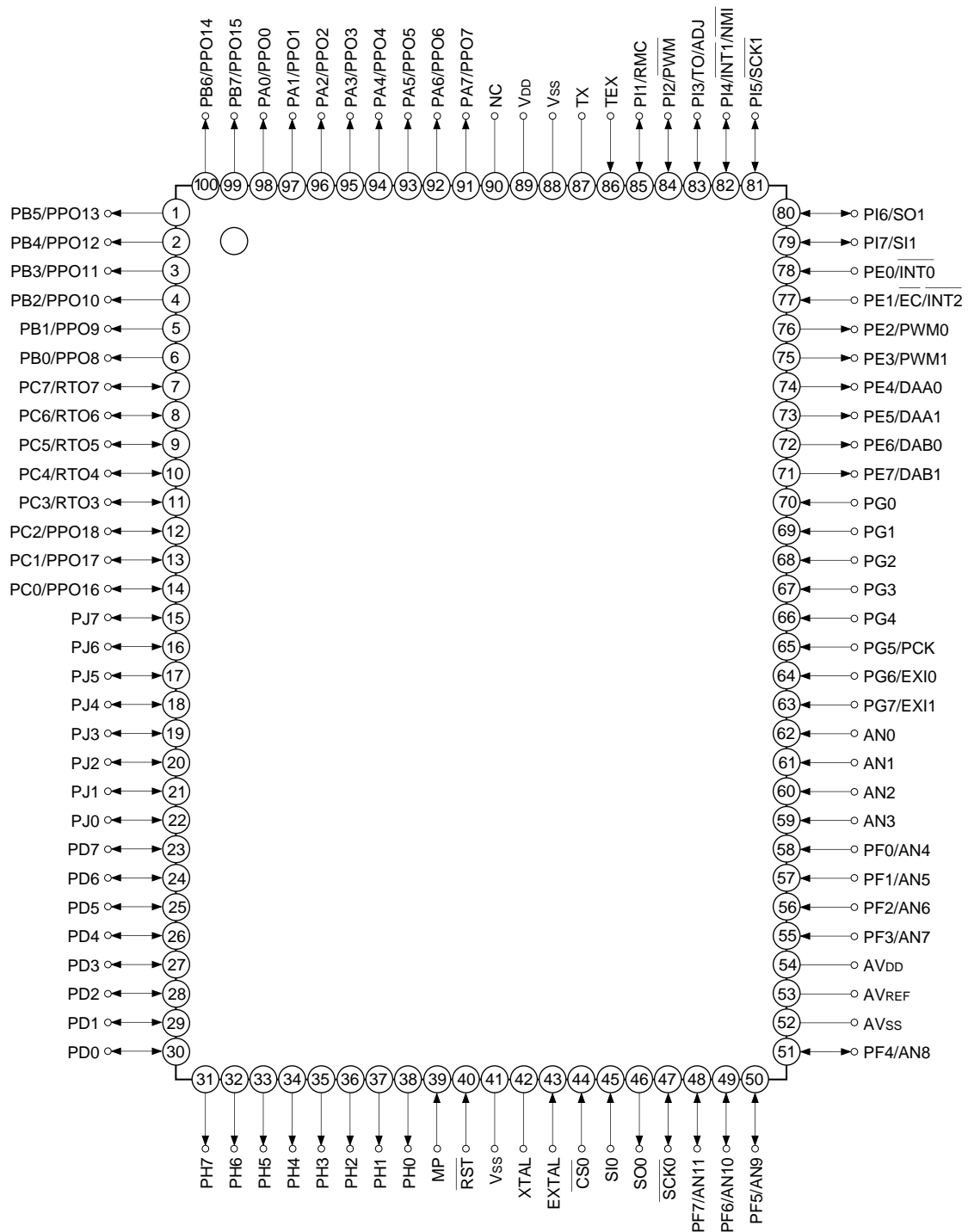


Block Diagram

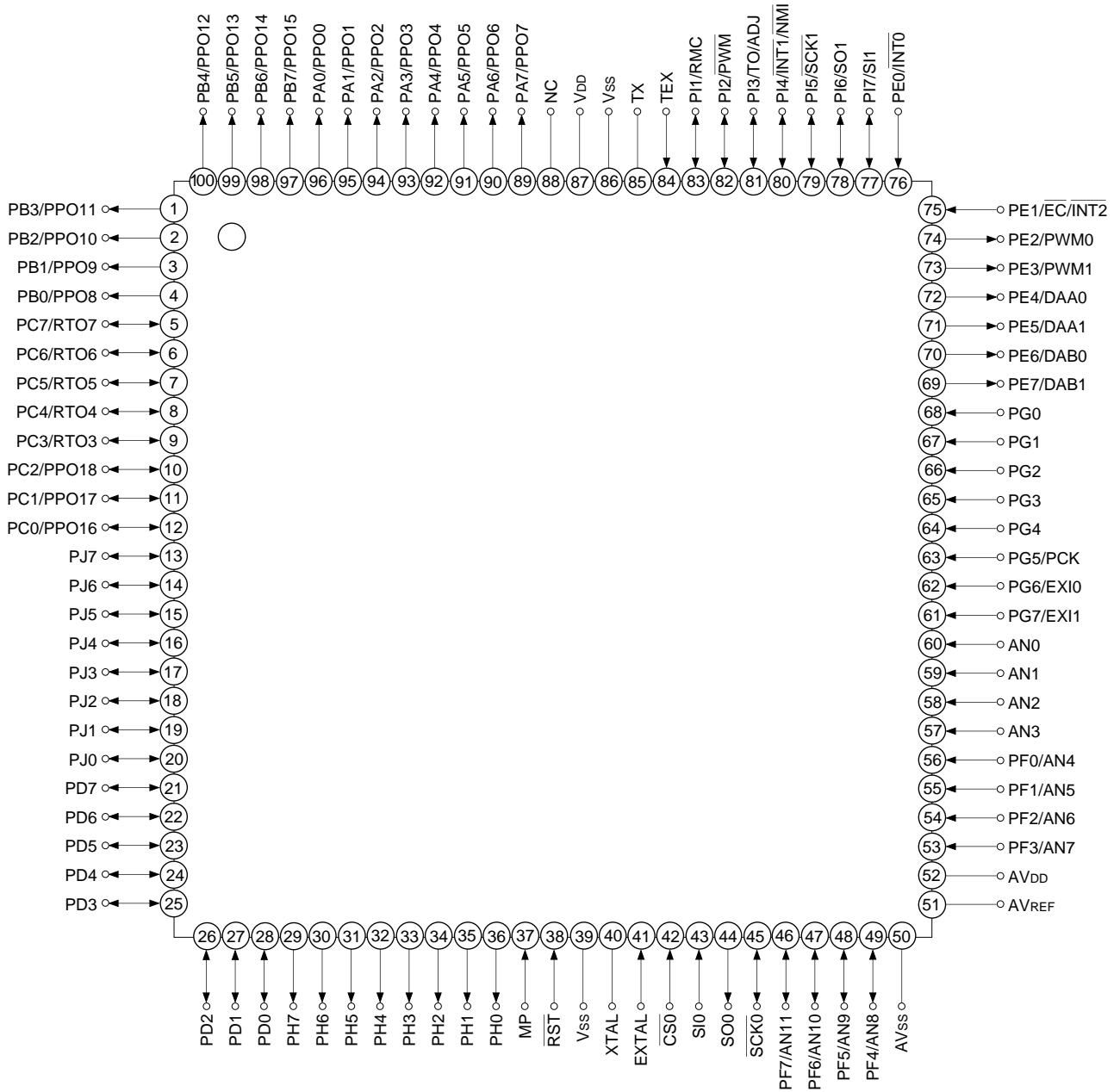


Pin Configuration 1 (Top View) 100-pin QFP package



- Note** 1. NC (Pin 90) is always connected to VDD.
 2. Vss (Pins 41 and 88) are both connected to GND.

Pin Configuration 2 (Top View) 100-pin LQFP package



- Note** 1. NC (Pin 88) is always connected to V_{DD}.
- 2. V_{SS} (Pins 39 and 86) are both connected to GND.

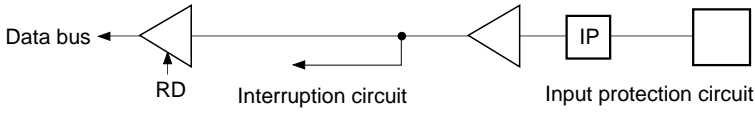
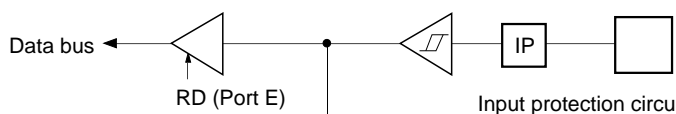
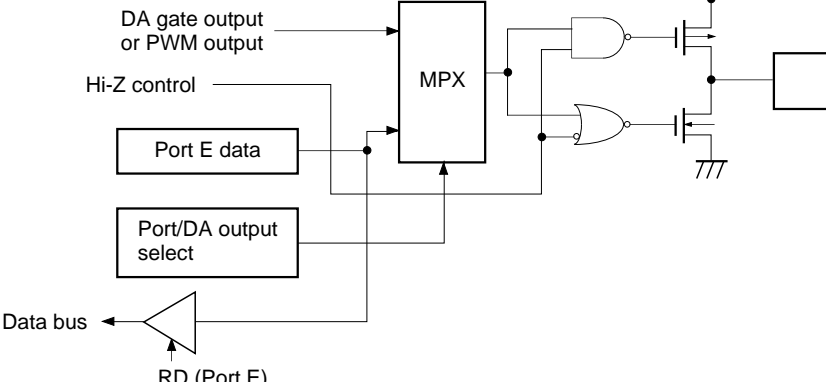
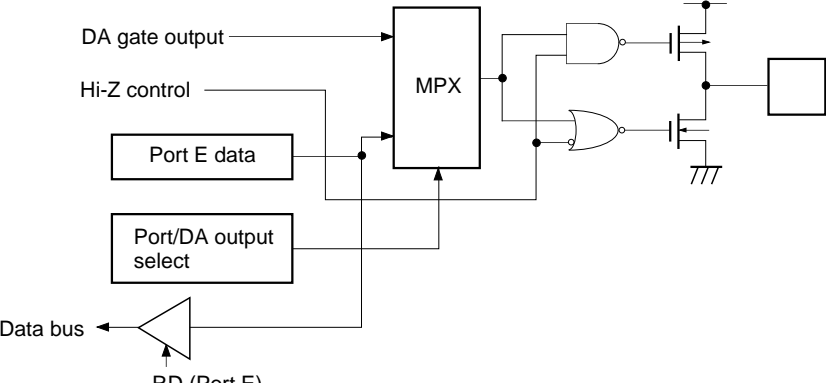
Pin Description

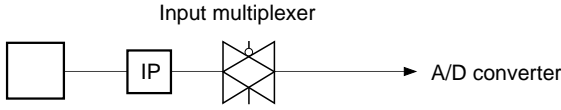
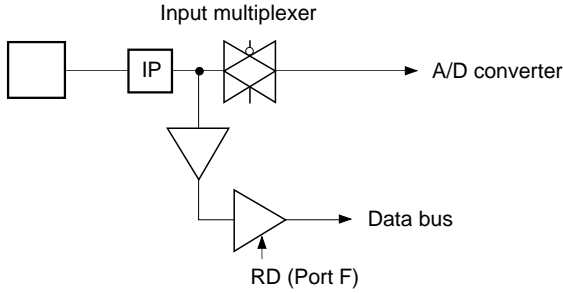
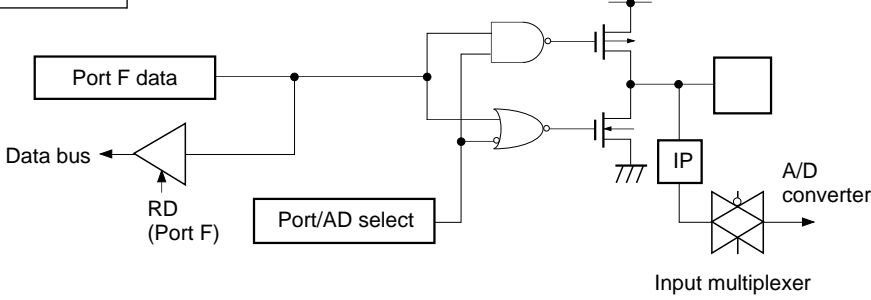
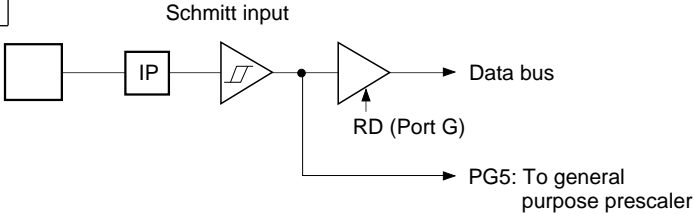
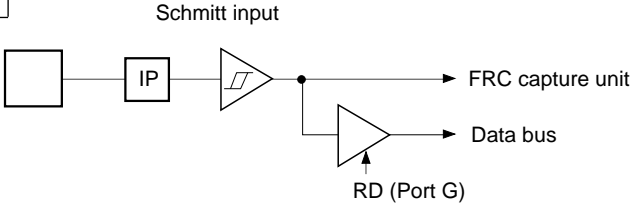
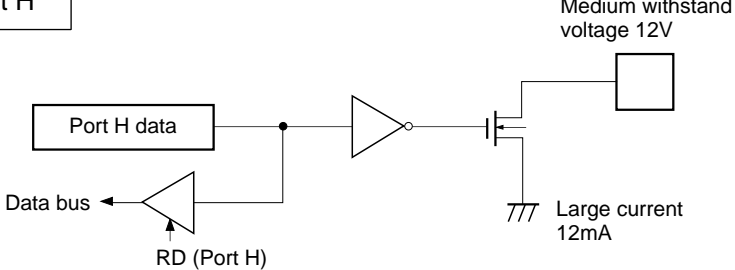
Symbol	I/O	Description		
PA0/PPO0 to PA7/PPO7	Output/ Real time output	(Port A) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)	Programmable pattern generator (PPG) output. Functions as high precision real time pulse output port. (19 pins)	
PB0/PPO8 to PB7/PPO15	Output/ Real time output	(Port B) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)		
PC0/PPO16 to PC2/PPO18	I/O/ Real time output	(Port C) 8-bit I/O port, enables to specify I/O by bit unit. Data is gated with PPO or RTO contents by OR-gate and they are output. (8 pins)		
PC3/RTO3 to PC7/RTO7	I/O/ Real time output		Real time pulse generator (RTG) output. Functions as high precision real time pulse output port. (5 pins)	
PD0 to PD7	I/O	(Port D) 8-bit I/O port. Enable to specify I/O by 4-bit unit. Enables to drive 12mA sink current. (8 pins)		
PE0/ $\overline{\text{INT0}}$	Input/Input	(Port E) 8-bit port. Lower 2 bits are input pins and upper 6 bits are output pins. (8 pins)	Input pin to request external interruption. Active when falling edge.	
PE1/ $\overline{\text{EC}}/\overline{\text{INT2}}$	Input/Input/Input		External event input pin for timer/counter.	Input pin to request external interruption. Active when falling edge.
PE2/PWM0	Output/Output		Pulse width modulation (PWM) output pins. (2 pins)	
PE3/PWM1	Output/Output			
PE4/DAA0	Output/Output			DA gate pulse output pins. (4 pins)
PE5/DAA1	Output/Output			
PE6/DAB0	Output/Output			
PE7/DAB1	Output/Output			
AN0 to AN3	Input	Analog input pins to A/D converter. (12 pins)		
PF0/AN4 to PF3/AN7	Input/Input	(Port F) Lower 4 bits are input port and upper 4 bits are output port. Lower 4 bits also serve as standby release input pin. (8 pins)		
PF4/AN8 to PF7/AN11	Output/Input			
$\overline{\text{SCK0}}$	I/O	Serial clock (CH0) I/O pin.		
SO0	Output	Serial data (CH0) output pin.		
SI0	Input	Serial data (CH0) input pin.		
$\overline{\text{CS0}}$	Input	Serial chip select (CH0) input pin.		

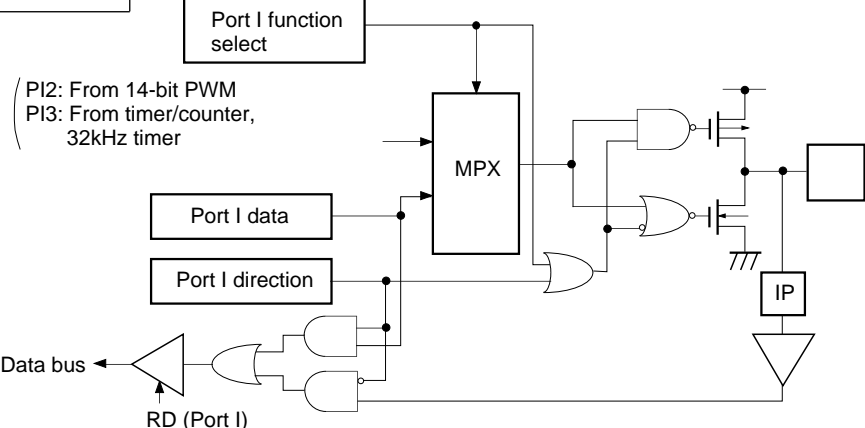
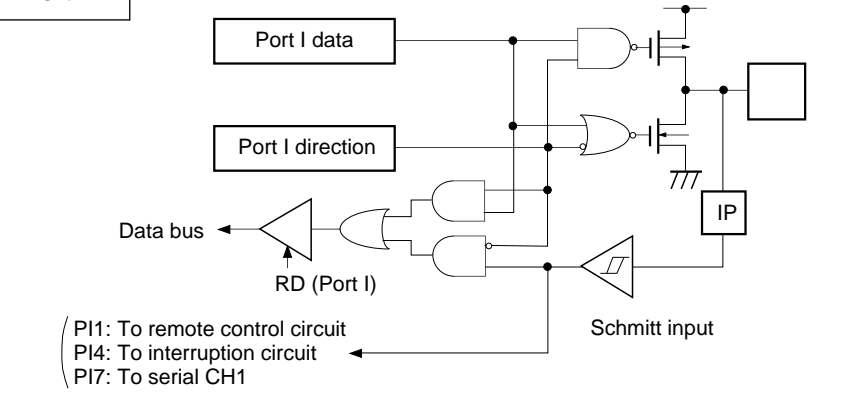
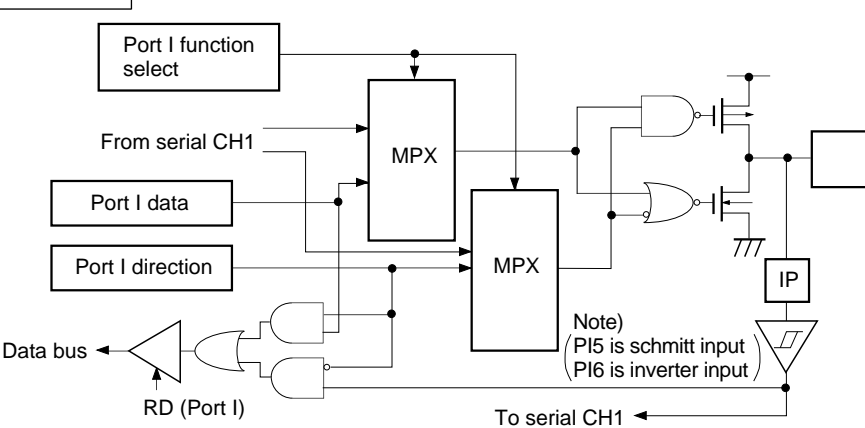
Symbol	I/O	Description	
PG0 to PG4	Input	(Port G) 8-bit input port. (8 pins)	7 bit general purpose prescaler input pin.
PG5/PCK			External input pin to FRC capture unit.
PG6/EXI0			
PG7/EXI1			
PH0 to PH7	Output	(Port H) 8-bit output port ; Medium withstand voltage (12V) and high current (12mA), N-ch open drain output. (8 pins)	
PI1/RMC	I/O/Input	(Port I) 7-bit I/O port. I/O port can be specified by bit unit. (7 pins)	Remote control receiving circuit input pin.
PI2/PWM	I/O/Output		14-bit PWM output pin.
PI3/TO/ADJ	I/O/Output/Output		Timer/counter, 32kHz oscillation adjustment output pin.
PI4/ $\overline{\text{INT1}}$ / NMI	I/O/Input/Input		Input pin to request external interruption and non-maskable interruption. Active when falling edge.
PI5/SCK1	I/O/I/O		Serial clock (CH1) I/O pin.
PI6/SO1	I/O/Output		Serial data (CH1) output pin.
PI7/SI1	I/O/Input		Serial data (CH1) input pin.
PJ0 to PJ7	I/O		(Port J) 8-bit I/O port. Function as standby release input can be specified by bit unit. I/O can be specified by bit unit.
EXTAL	Input	Connecting pin of crystal oscillator for system clock. When supplying the external clock, input the external clock to EXTAL pin and input opposite phase clock to XTAL pin.	
XTAL	Output		
TEX	Input	Connecting pin of crystal oscillator for 32kHz timer clock. When used as event counter, input to TEX pin and leave TX pin open. (Feedback resistor is not removed.)	
TX	Output		
$\overline{\text{RST}}$	Input	System reset pin of active "L" level.	
MP	Input	Microprocessor mode input pin. Always connect to GND.	
AV _{DD}		Positive power supply pin of A/D converter.	
AV _{REF}	Input	Reference voltage input pin of A/D converter.	
AV _{SS}		GND pin of A/D converter.	
V _{DD}		Positive power supply pin.	
V _{SS}		GND pin. Connect both V _{SS} pins to GND.	

Input/Output Circuit Formats for Pins

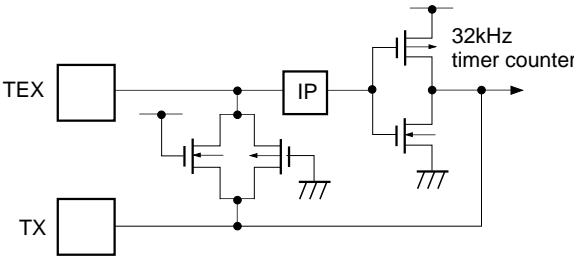
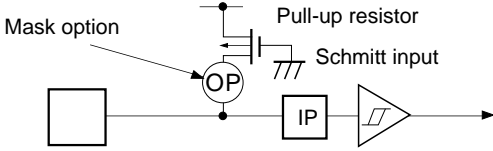
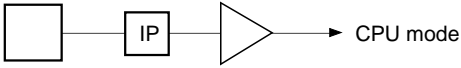
Pin	Circuit format	When reset
<p>Port A Port B</p> <p>PA0/PPO0 to PA7/PPO7 PB0/PPO8 to PB7/PPO15</p> <p>16 pins</p>	<p>PPO data</p> <p>Port A or Port B</p> <p>Data bus</p> <p>RD</p> <p>Output becomes active from high impedance by data writing to port register.</p>	<p>Hi-Z</p>
<p>Port C</p> <p>PC0/PPO16 to PC2/PPO18 PC3/RTO3 to PC7/RTO7</p> <p>8 pins</p>	<p>PPO, RTO data</p> <p>Port C data</p> <p>Port C direction</p> <p>Data bus</p> <p>RD (Port C)</p> <p>(Every bit)</p> <p>Input protection circuit</p> <p>IP</p>	<p>Hi-Z</p>
<p>Port D</p> <p>PD0 to PD7</p> <p>8 pins</p>	<p>Port D data</p> <p>Port D direction</p> <p>Data bus</p> <p>RD (Port D)</p> <p>(Every 4 bits) (PD0 to 3) (PD4 to 7)</p> <p>High current 12mA</p> <p>IP</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
<p>PE0/$\overline{\text{INT0}}$</p> <p>1 pin</p>	<p>Port E</p>  <p>Data bus</p> <p>RD</p> <p>Interruption circuit</p> <p>Input protection circuit</p>	<p>Hi-Z</p>
<p>PE1/$\overline{\text{EC}}/\overline{\text{INT2}}$</p> <p>1 pin</p>	<p>Port E</p>  <p>Data bus</p> <p>RD (Port E)</p> <p>Interruption circuit/ event counter</p> <p>Input protection circuit</p>	<p>Hi-Z</p>
<p>PE2/PWM0 PE3/PWM1 PE4/DAA0 PE5/DAA1</p> <p>4 pins</p>	<p>Port E</p>  <p>DA gate output or PWM output</p> <p>Hi-Z control</p> <p>Port E data</p> <p>Port/DA output select</p> <p>Data bus</p> <p>RD (Port E)</p> <p>MPX</p>	<p>Hi-Z</p>
<p>PE6/DAB0 PE7/DAB1</p> <p>2 pins</p>	<p>Port E</p>  <p>DA gate output</p> <p>Hi-Z control</p> <p>Port E data</p> <p>Port/DA output select</p> <p>Data bus</p> <p>RD (Port E)</p> <p>MPX</p>	<p>H level</p>

Pin	Circuit format	When reset
AN0 to AN3 4 pins		Hi-Z
PF0/AN4 to PF3/AN7 4 pins		Hi-Z
PF4/AN8 to PF7/AN11 4 pins		Hi-Z
PG0 to PG4 PG5/PCK 6 pins		Hi-Z
PG6/EXI0 PG7/EXI1 2 pins		Hi-Z
PH0 to PH7 8 pins		Hi-Z

Pin	Circuit format	When reset
<p>PI2/$\overline{\text{PWM}}$ PI3/$\overline{\text{TO/ADJ}}$</p> <p>2 pins</p>	<p>Port I</p>  <p>(PI2: From 14-bit PWM PI3: From timer/counter, 32kHz timer)</p> <p>Port I function select</p> <p>Port I data</p> <p>Port I direction</p> <p>Data bus</p> <p>RD (Port I)</p> <p>IP</p>	<p>Hi-Z</p>
<p>PI1/$\overline{\text{RMC}}$ PI4/$\overline{\text{INT1/NMI}}$ PI7/$\overline{\text{SI1}}$</p> <p>3 pins</p>	<p>Port I</p>  <p>Port I data</p> <p>Port I direction</p> <p>Data bus</p> <p>RD (Port I)</p> <p>Schmitt input</p> <p>IP</p> <p>(PI1: To remote control circuit PI4: To interruption circuit PI7: To serial CH1)</p>	<p>Hi-Z</p>
<p>PI5/$\overline{\text{SCK1}}$ PI6/$\overline{\text{SO1}}$</p> <p>2 pins</p>	<p>Port I</p>  <p>Port I function select</p> <p>From serial CH1</p> <p>Port I data</p> <p>Port I direction</p> <p>Data bus</p> <p>RD (Port I)</p> <p>IP</p> <p>Note) (PI5 is schmitt input PI6 is inverter input)</p> <p>To serial CH1</p>	<p>Hi-Z</p>

Pin	Circuit format	When reset
PJ0 to PJ7 8 pins		Hi-Z
$\overline{\text{CS0}}$ SIO 2 pins		Hi-Z
SO0 1 pin		Hi-Z
$\overline{\text{SCK0}}$ 1 pin		Hi-Z
EXTAL XTAL 2 pins	<ul style="list-style-type: none"> • Shows the circuit composition during oscillation. • Feedback resistor is removed during stop. 	Oscillation

Pin	Circuit format	When reset
<p>TEX TX</p> <p>2 pins</p>	 <ul style="list-style-type: none"> • Shows the circuit composition during oscillation. • Feedback resistor is removed during 32kHz oscillation circuit stop by software. At this time TEX pin outputs "L" level and TX pin outputs "H" level. 	<p>Oscillation</p>
<p>$\overline{\text{RST}}$</p> <p>1 pin</p>		<p>L level</p>
<p>MP</p> <p>1 pin</p>		<p>Hi-Z</p>

Absolute Maximum Ratings

(V_{SS} = 0V)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V _{DD}	-0.3 to +7.0	V	
	AV _{DD}	AV _{SS} to +7.0* ¹	V	
	AV _{SS}	-0.3 to +0.3	V	
Input voltage	V _{IN}	-0.3 to +7.0* ²	V	
Output voltage	V _{OUT}	-0.3 to +7.0* ²	V	
Medium withstand output voltage	V _{OUTP}	-0.3 to +15.0	V	PH pin
High level output current	I _{OH}	-5	mA	
High level total output current	∑I _{OH}	-50	mA	Total of output pins
Low level output current	I _{OL}	15	mA	Other than large current output pins: per pin
	I _{OLC}	20	mA	Large current port pin* ³ : per pin
Low level total output current	∑I _{OL}	130	mA	Total of output pins
Operating temperature	T _{opr}	-20 to +75	°C	
Storage temperature	T _{stg}	-55 to +150	°C	
Allowable power dissipation	P _D	600	mW	QFP package type
		380		LQFP package type

*1 AV_{DD} and V_{DD} should be set to a same voltage.

*2 V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.

*3 The large current operation transistors are the N-CH transistors of the PD and PH ports.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	3.0	5.5	V	Guaranteed range during high speed mode (1/2 dividing clock) operation
		2.7	5.5	V	Guaranteed range during low speed mode (1/16 dividing clock) operation
		2.7	5.5	V	Guaranteed operation range by TEX clock
		2.0	5.5	V	Guaranteed data hold operation range during STOP
Analog power supply	AV _{DD}	3.0	5.5	V	*1
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	*2
	V _{IHS}	0.8V _{DD}	V _{DD}	V	CMOS schmitt input*3 and PE0/ $\overline{\text{INT0}}$ pin
			5.5	V	CMOS schmitt input*6
	V _{IHEX}	V _{DD} - 0.4	V _{DD} + 0.3	V	EXTAL pin*4, *7 and TEX pin*5, *7
			V _{DD} + 0.2	V	EXTAL pin*4, *8 and TEX pin*5, *8
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	*2, *7
		0	0.2V _{DD}	V	*2, *8
	V _{ILS}	0	0.2V _{DD}	V	CMOS schmitt input*3 and PE0/ $\overline{\text{INT0}}$ pin
	V _{ILEX}	-0.3	0.4	V	EXTAL pin*4, *7 and TEX pin*5, *7
			0.2	V	EXTAL pin*4, *8 and TEX pin*5, *8
Operating temperature	Topr	-20	+75	°C	

*1 AV_{DD} and V_{DD} should be set to a same voltage.

*2 Normal input port (each pin of PC, PD, PF0 to PF3, PG, PI and PJ), MP pin.

*3 Each pin of $\overline{\text{SCK0}}$, $\overline{\text{RST}}$, PE1/ $\overline{\text{EC}}$ / $\overline{\text{INT2}}$, PI1/RMC, PI4/ $\overline{\text{INT1}}$ / $\overline{\text{NMI}}$, PI5/ $\overline{\text{SCK1}}$ and PI7/SI1.

*4 It specifies only when the external clock is input.

*5 It specifies only when the external event count clock is input.

*6 Each pin of $\overline{\text{CS0}}$, SI0, and PG.

*7 In case of 4.5 to 5.5V supply voltage (V_{DD}).

*8 In case of 3.0 to 3.6V supply voltage (V_{DD}).

Electrical Characteristics

DC Characteristics ($V_{DD} = 4.5$ to $5.5V$)

($T_a = -20$ to $+75^\circ C$, $V_{SS} = 0V$)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE2 to PE7, PF4 to PF7, PH (V_{OL} only)	$V_{DD} = 4.5V$, $I_{OH} = -0.5mA$	4.0			V
			$V_{DD} = 4.5V$, $I_{OH} = -1.2mA$	3.5			V
Low level output voltage	V_{OL}	PI1 to PI7, PJ, SO0, SCK0	$V_{DD} = 4.5V$, $I_{OL} = 1.8mA$			0.4	V
			$V_{DD} = 4.5V$, $I_{OL} = 3.6mA$			0.6	V
		PD, PH	$V_{DD} = 4.5V$, $I_{OL} = 12.0mA$			1.5	V
Input current	I_{IHE}	EXTAL	$V_{DD} = 5.5V$, $V_{IH} = 5.5V$	0.5		40	μA
	I_{ILE}		$V_{DD} = 5.5V$, $V_{IL} = 0.4V$	-0.5		-40	μA
	I_{IHT}	TEX	$V_{DD} = 5.5V$, $V_{IH} = 5.5V$	0.1		10	μA
	I_{ILT}		$V_{DD} = 5.5V$, $V_{IL} = 0.4V$	-0.1		-10	μA
	I_{ILR}		\overline{RST}^{*1}	$V_{DD} = 5.5V$, $V_{IL} = 0.4V$	-1.5		-400
I/O leakage current	I_{IZ}	PA to PG, PI, PJ, MP, AN0 to AN3, CS0, SI0, SO0, SCK0, \overline{RST}^{*1}	$V_{DD} = 5.5V$, $V_I = 0, 5.5V$			± 10	μA
Open drain output leakage current (N-CH Tr OFF in state)	I_{LOH}	PH	$V_{DD} = 5.5V$, $V_{OH} = 12V$			50	μA
Supply current*2	I_{DD1}	V_{DD}	16MHz crystal oscillation ($C_1 = C_2 = 15pF$)		31	50	mA
			$V_{DD} = 5V \pm 0.5V^{*3}$				
	I_{DDS1}		SLEEP mode		2.0	8	mA
			$V_{DD} = 5V \pm 0.5V$				
	I_{DD2}		32kHz crystal oscillation ($C_1 = C_2 = 47pF$)		46	110	μA
			$V_{DD} = 3V \pm 0.3V$				
I_{DDS2}	SLEEP mode		9	35	μA		
	$V_{DD} = 3V \pm 0.3V$						
I_{DDS3}	STOP mode (EXTAL and TEX pins oscillation stop)				10	μA	
	$V_{DD} = 5V \pm 0.5V$						
Input capacity	C_{IN}	Other than V_{DD} , V_{SS} , AV_{DD} , and AV_{SS}	Clock 1MHz 0V other than the measured pins		10	20	pF

*1 \overline{RST} pin specifies the input current when the pull-up resistor is selected, and specifies leakage current when non-resistor is selected.

*2 When entire output pins are open.

*3 When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 00FEH) to "00" and operating in high speed mode (1/2 dividing clock).

DC Characteristics (V_{DD} = 3.0 to 3.6V)

(T_a = -20 to +75°C, V_{SS} = 0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V _{OH}	PA to PD, PE2 to PE7, PF4 to PF7, PH (V _{OL} only), PI1 to PI7	V _{DD} = 3.0V, I _{OH} = -0.15mA	2.7			V
			V _{DD} = 3.0V, I _{OH} = 0.5mA	2.3			V
Low level output voltage	V _{OL}	PJ, SO0, SCK0	V _{DD} = 3.0V, I _{OL} = 1.2mA			0.3	V
			V _{DD} = 3.0V, I _{OL} = 1.6mA			0.5	V
		PD, PH	V _{DD} = 3.0V, I _{OL} = 5mA			1.0	V
Input current	I _{IHE}	EXTAL	V _{DD} = 3.6V, V _{IH} = 3.6V	0.3		20	μA
	I _{ILE}		V _{DD} = 3.6V, V _{IL} = 0.3V	-0.3		-20	μA
	I _{IHT}	TEX	V _{DD} = 3.6V, V _{IH} = 3.6V	0.1		10	μA
	I _{ILT}		V _{DD} = 3.6V, V _{IL} = 0.3V	-0.1		-10	μA
	I _{ILR}	RST*1	V _{DD} = 3.6V, V _{IL} = 0.3V	-0.9		-200	μA
I/O leakage current	I _{Iz}	PA to PG, PI, PJ, MP, AN0 to AN3, CS0, SI0, SO0, SCK0, RST*1	V _{DD} = 3.6V, V _I = 0, 3.6V			±10	μA
Open drain output leakage current	I _{LOH}	PH	V _{DD} = 3.6V, V _{OH} = 12V			50	μA
Supply current*2	I _{DD1}	V _{DD}	12MHz crystal oscillation (C ₁ = C ₂ = 15pF) V _{DD} = 3.3V ± 0.3V*3		15	30	mA
	I _{DDS1}		SLEEP mode V _{DD} = 3.3V ± 0.3V		0.8	2.5	mA
	I _{DDS3}		STOP mode (EXTAL and TEX pins oscillation stop) V _{DD} = 3.3V ± 0.3V			10	μA
Input capacity	C _{IN}	Other than V _{DD} , V _{SS} , AV _{DD} , and AV _{SS}	Clock 1MHz 0V other than the measured pins		10	20	pF

*1 RST pin specifies the input current when the pull-up resistor is selected, and specifies leakage current when non-resistor is selected.

*2 When entire output pins are open.

*3 When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 00FEH) to "00" and operating in high speed mode (1/2 dividing clock).

AC Characteristics

(1) Clock timing

(Ta = -20 to +75°C, VDD = 3.0 to 5.5V, VSS = 0V)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit	
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	VDD = 4.5 to 5.5V	1	16	MHz
					1	12	
System clock input pulse width	tXL, tXH	XTAL EXTAL	Fig. 1, Fig. 2 (External clock drive)	VDD = 4.5 to 5.5V	28		ns
					37.5		
System clock input rise and fall times	tCR, tCF	XTAL EXTAL	Fig. 1, Fig. 2 (External clock drive)		200	ns	
Event count clock input pulse width	tEH, tEL	\overline{EC}	Fig. 3	tsys × 4*		ns	
Event count clock input rise and fall times	tER, tEF	\overline{EC}	Fig. 3		20	ns	
System clock frequency	fc	TEX TX	Fig. 2 VDD = 2.7 to 5.5V (32kHz clock applied condition)	32.768		kHz	
Event count clock input pulse width	tTL, tTH	TEX	Fig. 3	10		μs	
Event count clock input rise and fall times	tTR, tTF	TEX	Fig. 3		20	ms	

* tsys indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

tsys [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Fig. 1. Clock timing

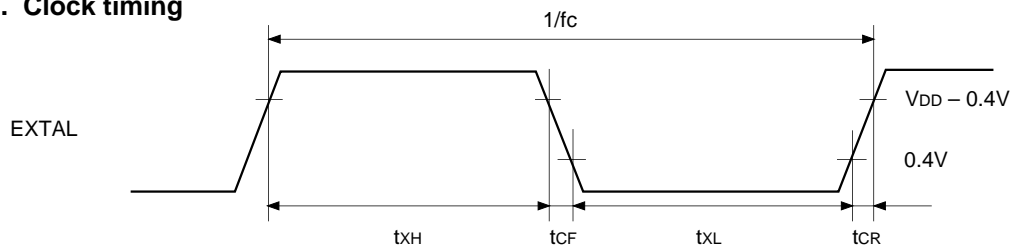


Fig. 2. Clock applied condition

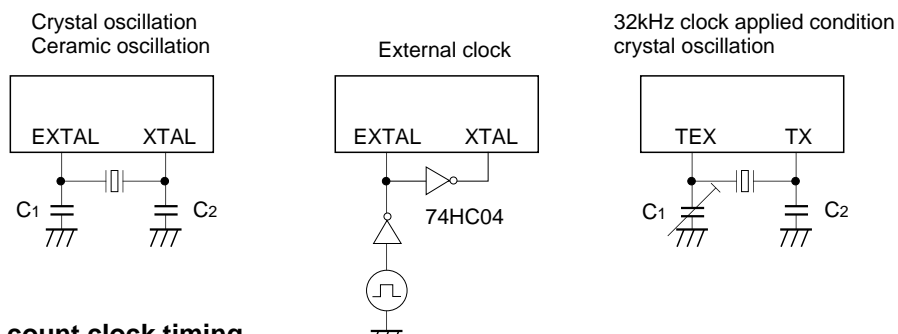
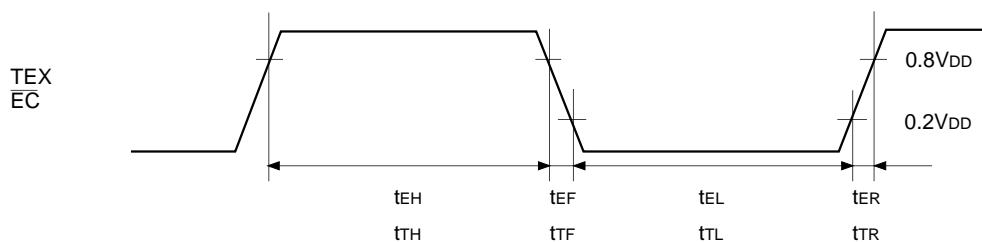


Fig. 3. Event count clock timing



(2) Serial transfer (CH0)

(Ta = -20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS} \downarrow \rightarrow \overline{SCK}$ delay time	t _{DCSK}	$\overline{SCK0}$	Chip select transfer mode (SCK = output mode)		t _{sys} + 200	ns
$\overline{CS} \uparrow \rightarrow \overline{SCK}$ floating delay time	t _{DCSKF}	$\overline{SCK0}$	Chip select transfer mode (SCK = output mode)		t _{sys} + 200	ns
$\overline{CS} \downarrow \rightarrow SO$ delay time	t _{DCSO}	SO0	Chip select transfer mode		t _{sys} + 200	ns
$\overline{CS} \downarrow \rightarrow SO$ floating delay time	t _{DCSOF}	SO0	Chip select transfer mode		t _{sys} + 200	ns
\overline{CS} high level width	t _{WHCS}	$\overline{CS0}$	Chip select transfer mode	t _{sys} + 200		ns
\overline{SCK} cycle time	t _{KCY}	$\overline{SCK0}$	Input mode	2t _{sys} + 200		ns
			Output mode	8000/fc		ns
\overline{SCK} high and low level widths	t _{KH} t _{KL}	$\overline{SCK0}$	Input mode	t _{sys} + 100		ns
			Output mode	8000/fc - 100		ns
SI input setup time (against $\overline{SCK} \uparrow$)	t _{SIK}	SI0	\overline{SCK} input mode	-t _{sys} + 100		ns
			\overline{SCK} output mode	200		ns
SI input hold time (against $\overline{SCK} \uparrow$)	t _{KSI}	SI0	\overline{SCK} input mode	2t _{sys} + 100		ns
			\overline{SCK} output mode	100		ns
$\overline{SCK} \downarrow \rightarrow SO$ delay time	t _{KSO}	SO0	\overline{SCK} input mode		2t _{sys} + 200	ns
			\overline{SCK} output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) \overline{CS} , \overline{SCK} , SI and SO means each pin of $\overline{CS} \rightarrow \overline{CS0}$, $\overline{SCK} \rightarrow \overline{SCK0}$, SI \rightarrow SI0, and SO \rightarrow SO0 respectively.

Note 3) The load of \overline{SCK} output mode and SO output delay time is 50pF + 1TTL.

Serial transfer (CH0)

(Ta = -20 to +75°C, VDD = 3.0 to 3.6V, VSS = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS} \downarrow \rightarrow \overline{SCK}$ delay time	t _{DCSK}	$\overline{SCK0}$	Chip select transfer mode (\overline{SCK} = output mode)		t _{sys} + 250	ns
$\overline{CS} \uparrow \rightarrow \overline{SCK}$ floating delay time	t _{DCSKF}	$\overline{SCK0}$	Chip select transfer mode (\overline{SCK} = output mode)		t _{sys} + 200	ns
$\overline{CS} \downarrow \rightarrow SO$ delay time	t _{DCSO}	SO0	Chip select transfer mode		t _{sys} + 250	ns
$\overline{CS} \downarrow \rightarrow SO$ floating delay time	t _{DCSOF}	SO0	Chip select transfer mode		t _{sys} + 200	ns
\overline{CS} high level width	t _{WHCS}	$\overline{CS0}$	Chip select transfer mode	t _{sys} + 200		ns
\overline{SCK} cycle time	t _{KCY}	$\overline{SCK0}$	Input mode	2t _{sys} + 200		ns
			Output mode	8000/fc		ns
\overline{SCK} high and low level widths	t _{KH} t _{KL}	$\overline{SCK0}$	Input mode	t _{sys} + 100		ns
			Output mode	8000/fc - 150		ns
SI input setup time (against $\overline{SCK} \uparrow$)	t _{SIK}	SI0	\overline{SCK} input mode	-t _{sys} +100		ns
			\overline{SCK} output mode	200		ns
SI input hold time (against $\overline{SCK} \uparrow$)	t _{KSI}	SI0	\overline{SCK} input mode	2t _{sys} +100		ns
			\overline{SCK} output mode	100		ns
$\overline{SCK} \downarrow \rightarrow SO$ delay time	t _{KSO}	SO0	\overline{SCK} input mode		2t _{sys} + 250	ns
			\overline{SCK} output mode		125	ns

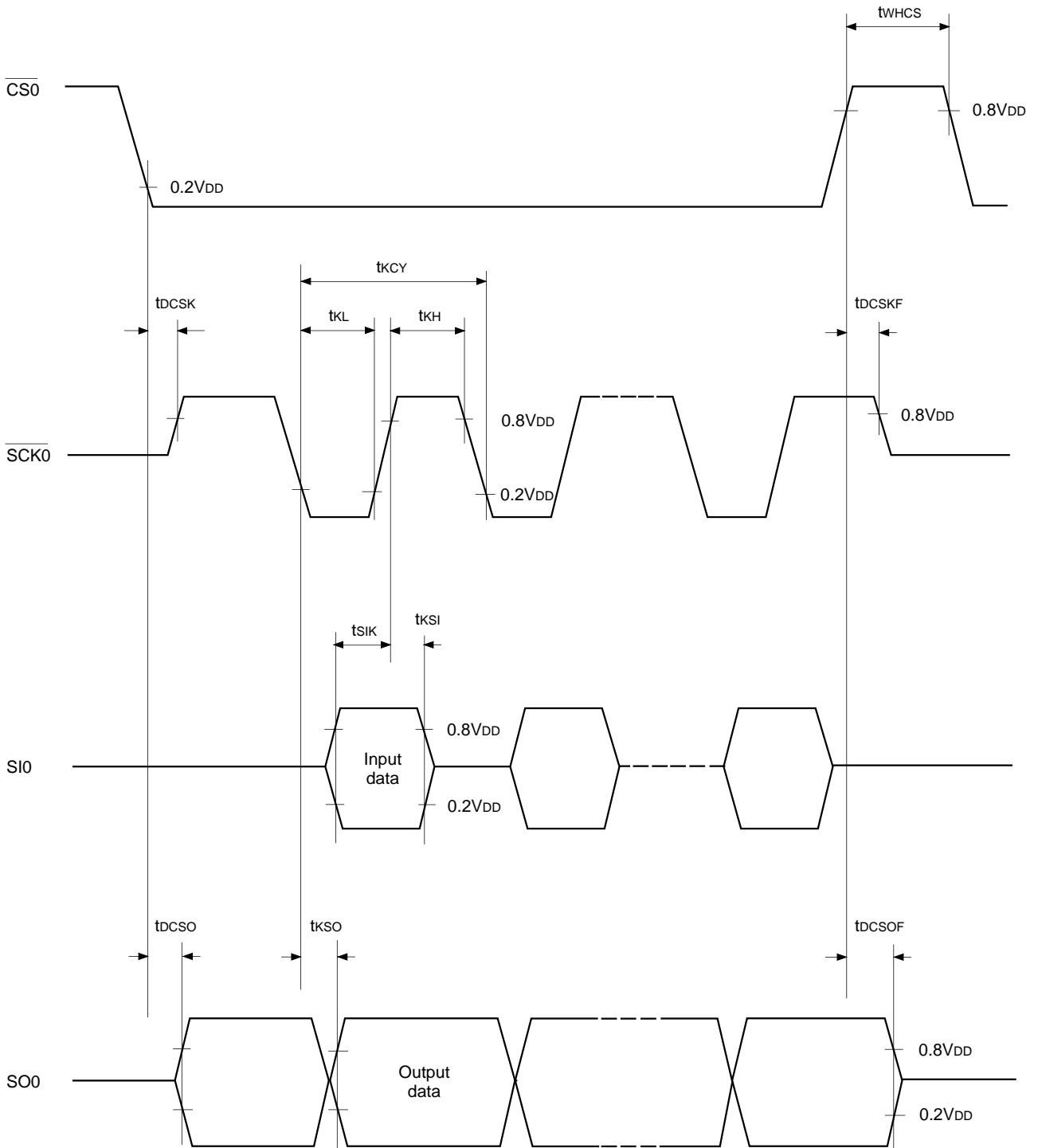
Note 1) t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) \overline{CS} , \overline{SCK} , SI and SO means each pin of $\overline{CS} \rightarrow \overline{CS0}$, $\overline{SCK} \rightarrow \overline{SCK0}$, SI \rightarrow SI0, and SO \rightarrow SO0 respectively.

Note 3) The load of \overline{SCK} output mode and SO output delay time is 50pF.

Fig. 4. Serial transfer timing (CH0)



Serial transfer (CH1)

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{CY}	$\overline{\text{SCK1}}$	Input mode	$2t_{\text{sys}} + 200$		ns
			Output mode	$8000/f_c$		ns
$\overline{\text{SCK1}}$ high and low level widths	t_{KH} t_{KL}	$\overline{\text{SCK1}}$	Input mode	$t_{\text{sys}} + 100$		ns
			Output mode	$4000/f_c - 100$		ns
SI1 input setup time (against $\overline{\text{SCK1}} \uparrow$)	t_{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (against $\overline{\text{SCK1}} \uparrow$)	t_{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	$t_{\text{sys}} + 200$		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK1}} \downarrow \rightarrow \text{SO1}$ delay time	t_{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		$t_{\text{sys}} + 200$	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/ f_c (Upper 2 bits = "00"), 4000/ f_c (Upper 2 bits = "01"), 16000/ f_c (Upper 2 bits = "11")

Note 2) The load of $\overline{\text{SCK1}}$ output mode and SO1 output delay time is 50pF + 1TTL.

Serial transfer (CH1)

(Ta = -20 to +75°C, VDD = 3.0 to 3.6V, VSS = 0V)

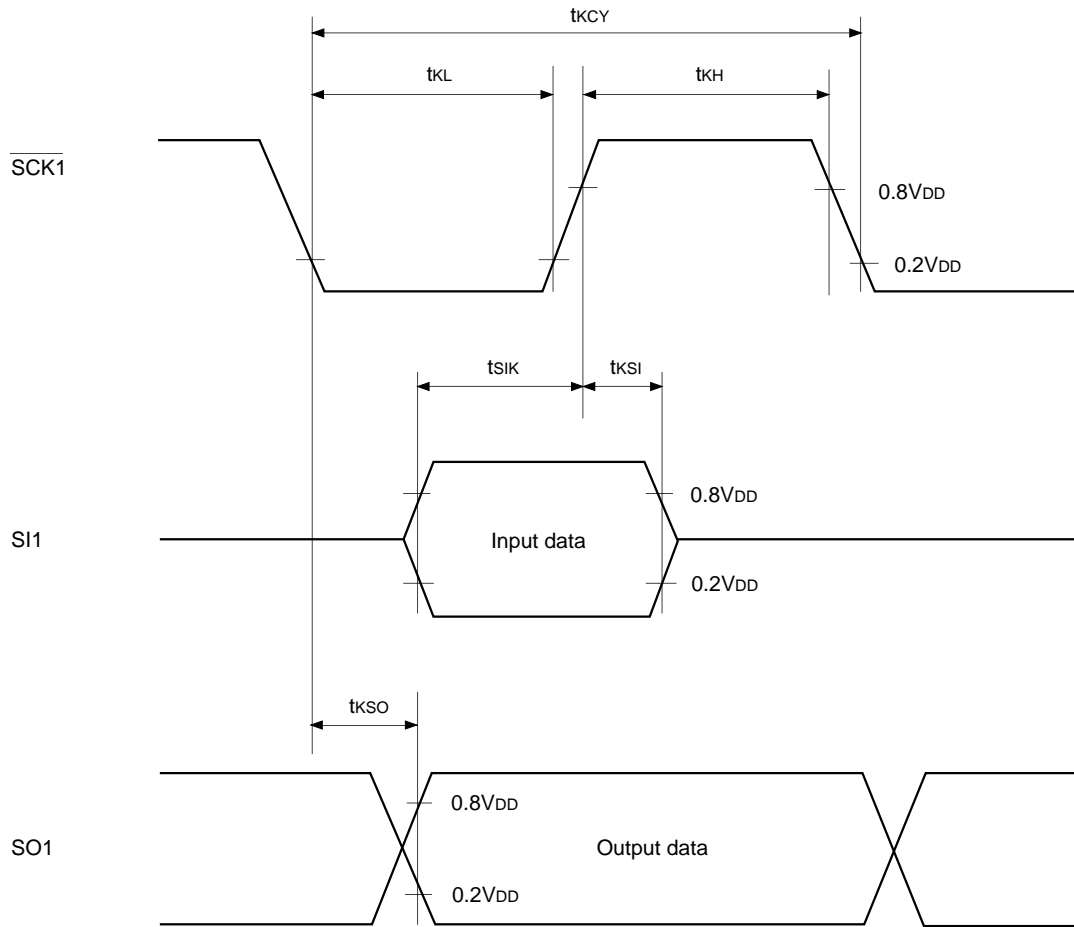
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{CY}	$\overline{\text{SCK1}}$	Input mode	$2t_{\text{sys}} + 200$		ns
			Output mode	$8000/f_c$		ns
$\overline{\text{SCK1}}$ high and low level widths	t_{KH} t_{KL}	$\overline{\text{SCK1}}$	Input mode	$t_{\text{sys}} + 100$		ns
			Output mode	$4000/f_c - 150$		ns
SI1 input setup time (against $\overline{\text{SCK1}} \uparrow$)	t_{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (against $\overline{\text{SCK1}} \uparrow$)	t_{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	$t_{\text{sys}} + 200$		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK1}} \downarrow \rightarrow \text{SO1}$ delay time	t_{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		$t_{\text{sys}} + 250$	ns
			$\overline{\text{SCK1}}$ output mode		125	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/ f_c (Upper 2 bits = "00"), 4000/ f_c (Upper 2 bits = "01"), 16000/ f_c (Upper 2 bits = "11")

Note 2) The load of $\overline{\text{SCK1}}$ output mode and SO1 output delay time is 50pF.

Fig. 5. Serial transfer CH1 timing

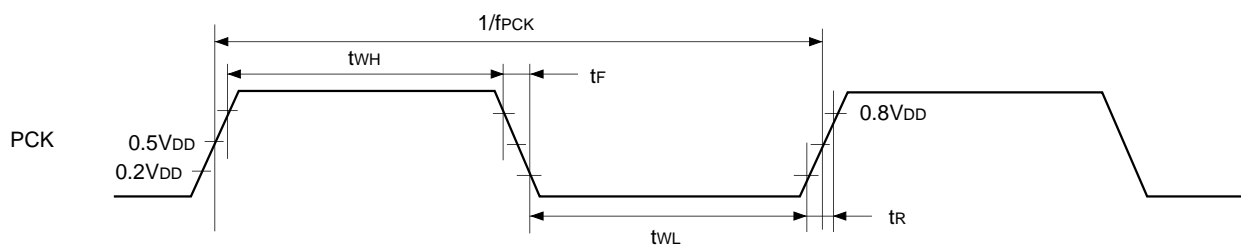


(3) General purpose prescaler

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
External clock input frequency	f_{PCK}	PCK				12	MHz
External clock input pulse width	t_{WH} , t_{WL}	PCK		33			ns
External clock input rise and fall times	t_R , t_F	PCK				200	ns

Fig. 6. General purpose prescaler timing



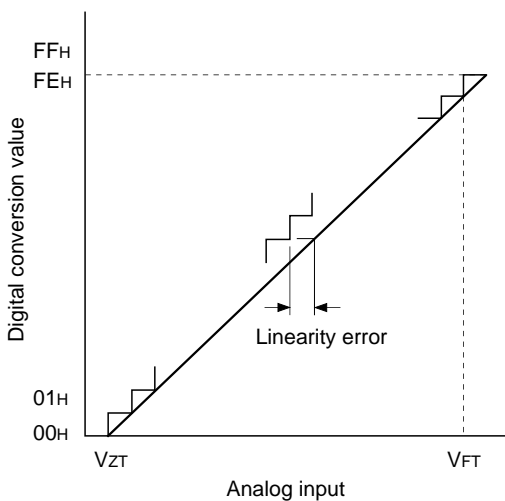
(4) A/D converter characteristics ($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = AV_{DD} = 4.5$ to 5.5V , $AV_{REF} = 4.0$ to AV_{DD} , $V_{SS} = AV_{SS} = 0\text{V}$)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			$T_a = 25^\circ\text{C}$ $V_{DD} = AV_{DD} = AV_{REF} = 5.0\text{V}$ $V_{SS} = AV_{SS} = 0\text{V}$			± 1	LSB
Absolute error						± 2	LSB
Conversion time	t_{CONV}			$160/f_{ADC}^*$			μs
Sampling time	t_{SAMP}			$12/f_{ADC}^*$			μs
Reference input voltage	V_{REF}	AV_{REF}	$V_{DD} = AV_{DD} = 4.5$ to 5.5V	$AV_{DD} - 0.5$		AV_{DD}	V
Analog input voltage	V_{IAN}	$AN0$ to $AN11$		0			V
AV_{REF} current	I_{REF}	AV_{REF}	Operating mode		0.6	1.0	mA
	I_{REFS}		SLEEP mode STOP mode 32kHz operating mode			10	μA

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = AV_{DD} = 3.0$ to 3.6V , $AV_{REF} = 2.7$ to AV_{DD} , $V_{SS} = AV_{SS} = 0\text{V}$)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			$T_a = 25^\circ\text{C}$ $V_{DD} = AV_{DD} = AV_{REF} = 5.0\text{V}$ $V_{SS} = AV_{SS} = 0\text{V}$			± 1	LSB
Absolute error						± 2	LSB
Conversion time	t_{CONV}			$160/f_{ADC}^*$			μs
Sampling time	t_{SAMP}			$12/f_{ADC}^*$			μs
Reference input voltage	V_{REF}	AV_{REF}	$V_{DD} = AV_{DD} = 3.0$ to 3.6V	$AV_{DD} - 0.3$		AV_{DD}	V
Analog input voltage	V_{IAN}	$AN0$ to $AN11$		0			
AV_{REF} current	I_{REF}	AV_{REF}	Operating mode		0.4	0.7	mA
	I_{REFS}		SLEEP mode STOP mode 32kHz operating mode			10	μA

Fig. 7. Definitions of A/D converter terms



* The value of f_{ADC} is as follows by selecting ADC operation clock (MSC: Address 01FFH bit 0).
 When PS2 is selected, $f_{ADC} = f_c/2$
 When PS1 is selected, $f_{ADC} = f_c$

(5) Interruption, reset input

(Ta = -20 to +75°C, VDD = 3.0 to 5.5V, VSS = 0V)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
External interruption high and low level widths	t _{IH} t _{IL}	$\overline{\text{INT0}}$ $\overline{\text{INT1}}$ $\overline{\text{INT2}}$ $\overline{\text{NMI}}$ PJ0 to PJ7		1		μs
Reset input low level width	t _{RSL}	$\overline{\text{RST}}$		32/fc		μs

Fig. 8. Interruption input timing

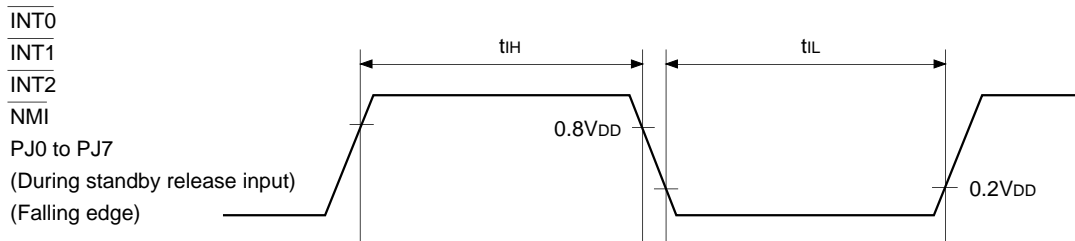
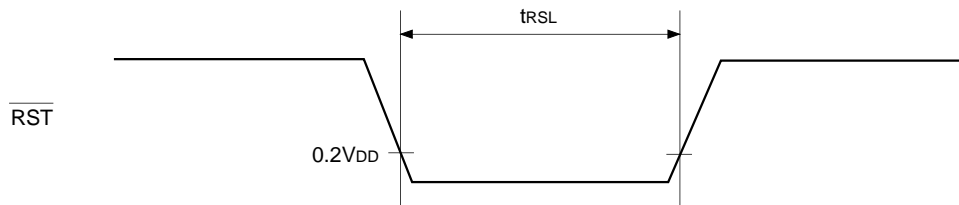


Fig. 9. Reset input timing



(6) Others

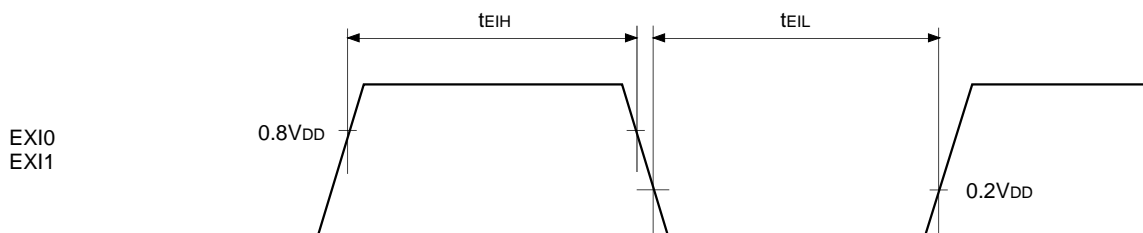
(Ta = -20 to +75°C, VDD = 3.0 to 5.5V, VSS = 0V)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
EXI input high and low level widths	t _{EIH} t _{EIL}	EXI0 EXI1	t _{sys} = 2000/fc	t _{FRC} × 8 + 200 + t _{sys}		ns

Note) t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

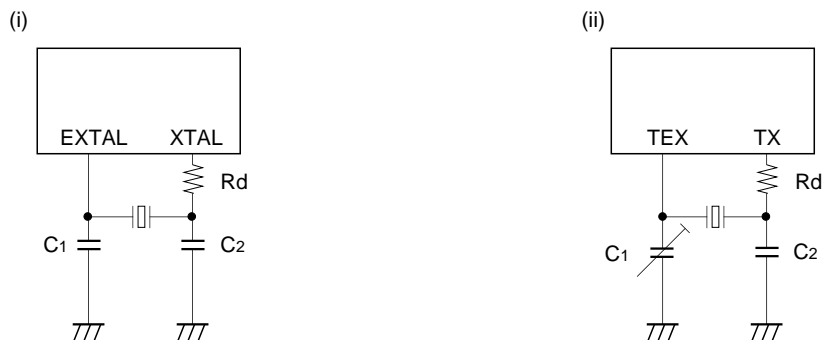
t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")
 t_{FRC} = 1000/fc [ns]

Fig. 10. Other timings



Supplement

Fig. 11. Recommended oscillation circuit

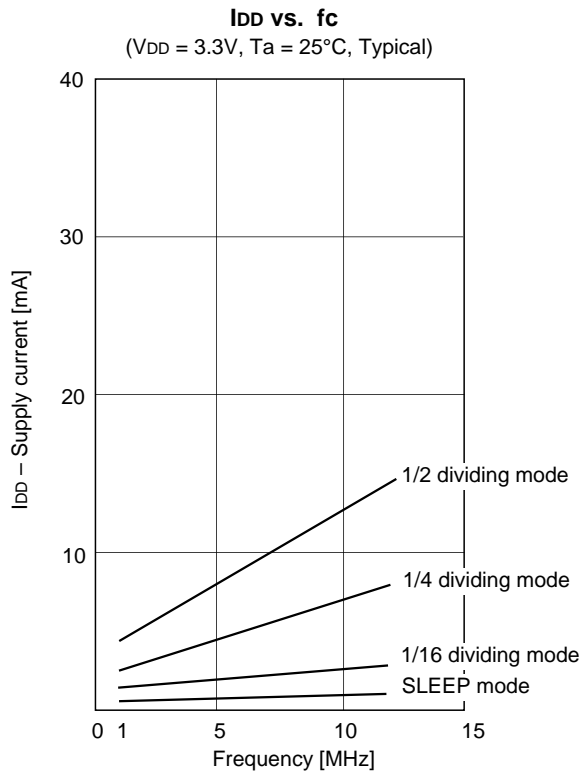
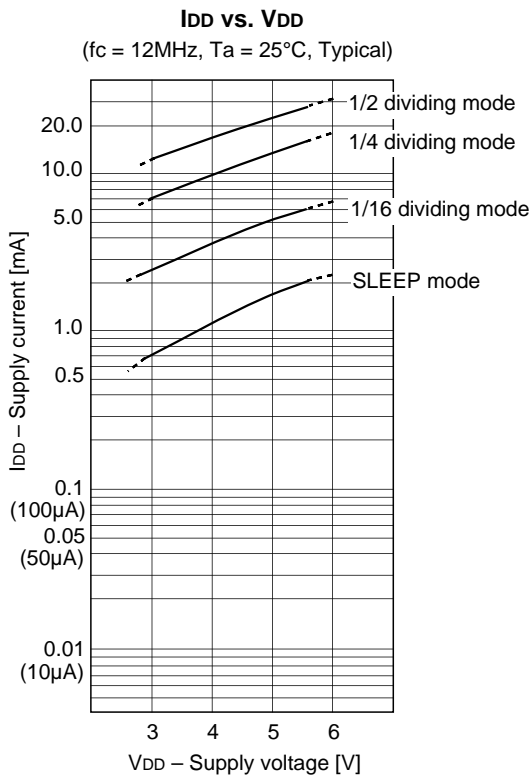
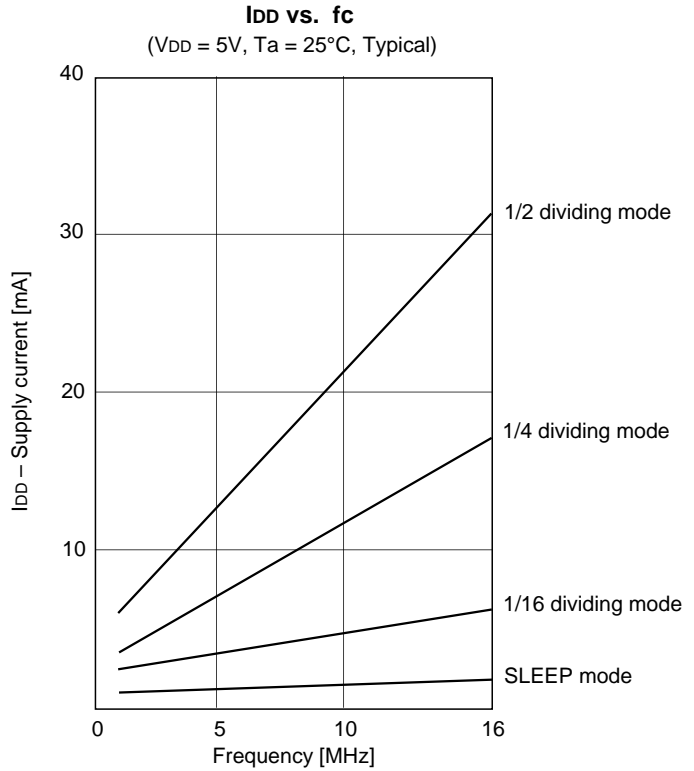
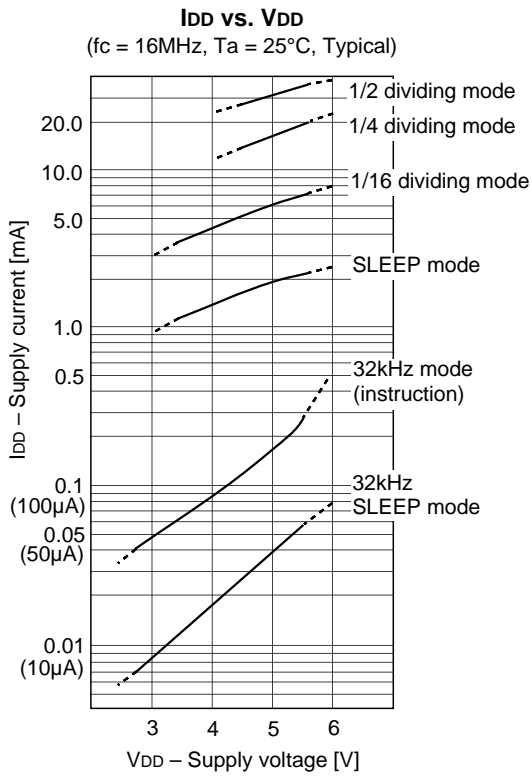


Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00	5	5		
		12.00				
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	16 (12)	16 (12)	0	(i)
		10.00	16 (12)	16 (12)		
		12.00	12	12		
		16.00	12	12		
	P3	32.768kHz	30	18	470K	(ii)

Mask option table

Item	Content	
Reset pin pull-up resistor	Non-existent	Existent

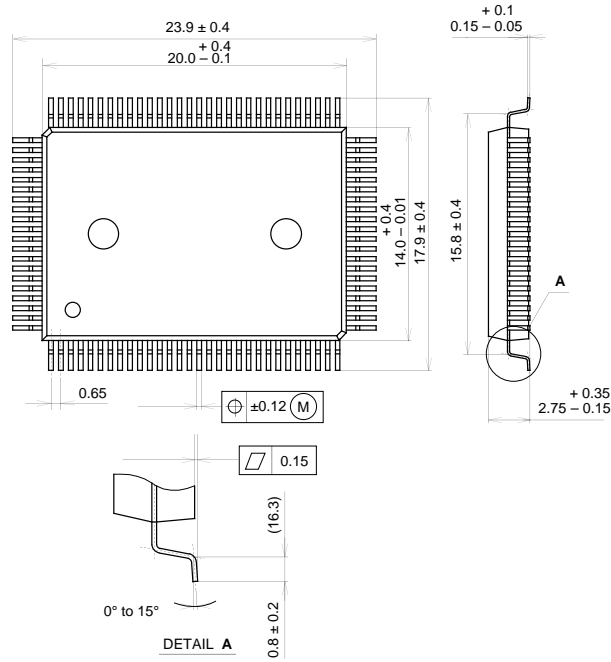
Characteristics Curve



Package Outline

Unit: mm

100PIN QFP (PLASTIC)

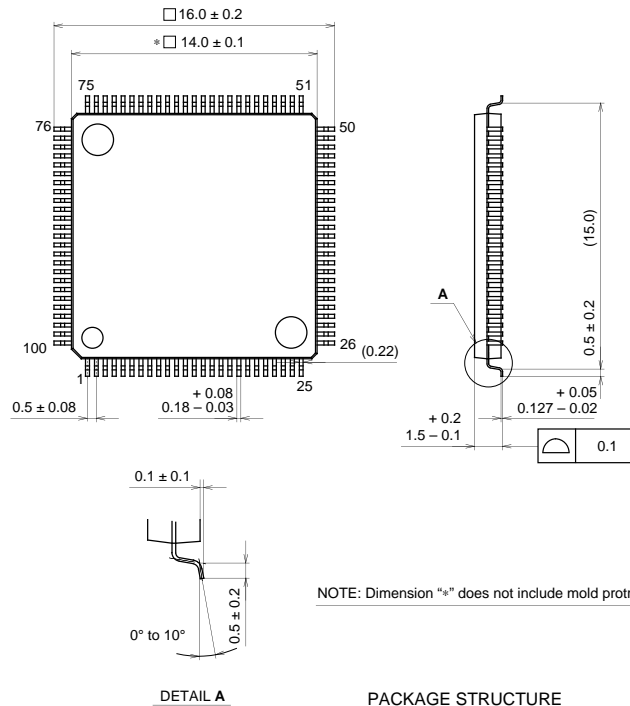


PACKAGE STRUCTURE

SONY CODE	QFP-100P-L01
EIAJ CODE	*QFP100-P-1420-A
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.4g

100PIN LQFP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	LQFP-100P-L01
EIAJ CODE	*QFP100-P-1414-A
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY/PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	_____