

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with Power Applied..... -55°C to +125°C
 Supply Voltage on V_{CC} to Relative GND^[3] -0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State^[3].....

..... -0.5V to V_{CC} + 0.5V

DC Input Voltage^[3] -0.5V to V_{CC} + 0.5V

Current into Outputs (LOW)..... 20 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	-40°C to +85°C	

Electrical Characteristics Over the Operating Range

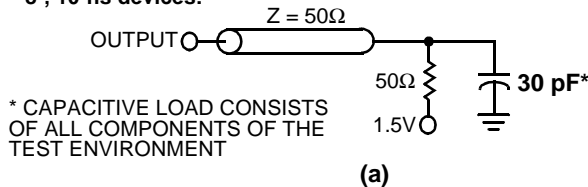
Parameter	Description	Test Conditions	-8 ^[2]		-10		-12		-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min.; I _{OH} = -4.0 mA	2.4		2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min.; I _{OL} = 8.0 mA		0.4		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.0	V _{CC} + 0.3	2.0	V _{CC} + 0.3	2.0	V _{CC} + 0.3	2.0	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage ^[3]		-0.3	0.8	-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-1	+1	-1	+1	-1	+1	-1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CC} , Output Disabled	-1	+1	-1	+1	-1	+1	-1	+1	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., f = f _{MAX} = 1/t _{RC}		100		90		85		80	mA
		Comm'l				100		95		90	mA
I _{SB1}	Automatic CE Power-down Current —TTL Inputs	Max. V _{CC} , CE ≥ V _{IH} ; V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		40		40		40		40	mA
			Ind'l								
I _{SB2}	Automatic CE Power-down Current —CMOS Inputs	Max. V _{CC} , CE ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f = 0		10		10		10		10	mA
			Com'l/Ind'l								

Capacitance^[4]

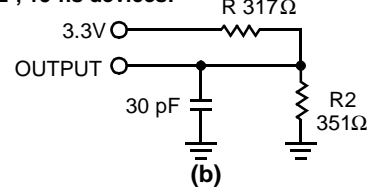
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz,	8	pF
C _{OUT}	I/O Capacitance	V _{CC} = 3.3V	8	pF

AC Test Loads and Waveforms^[5]

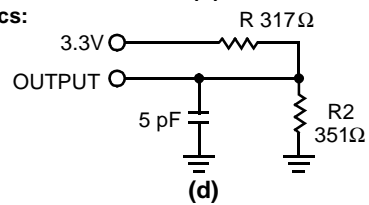
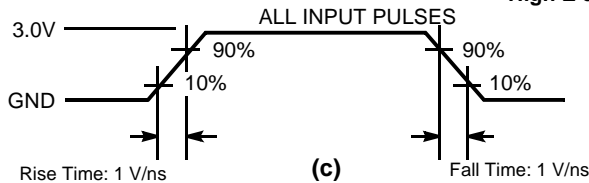
8-, 10-ns devices:



12-, 15-ns devices:



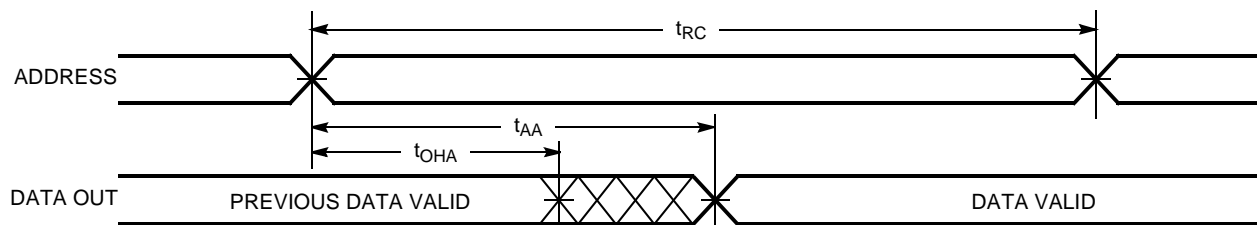
High-Z characteristics:


Notes:

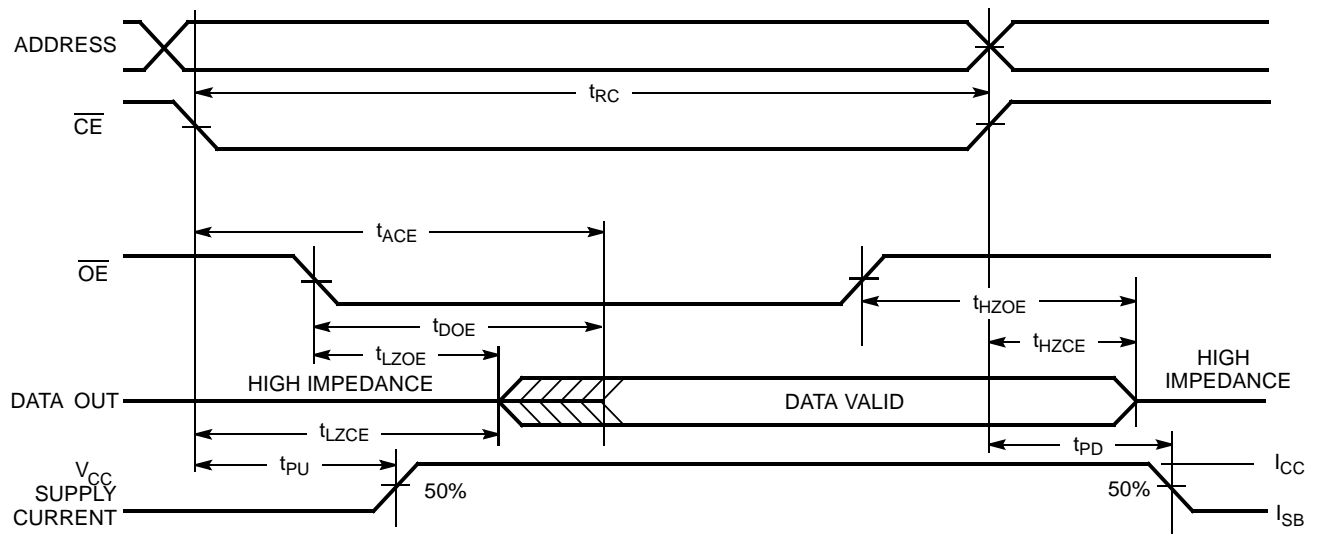
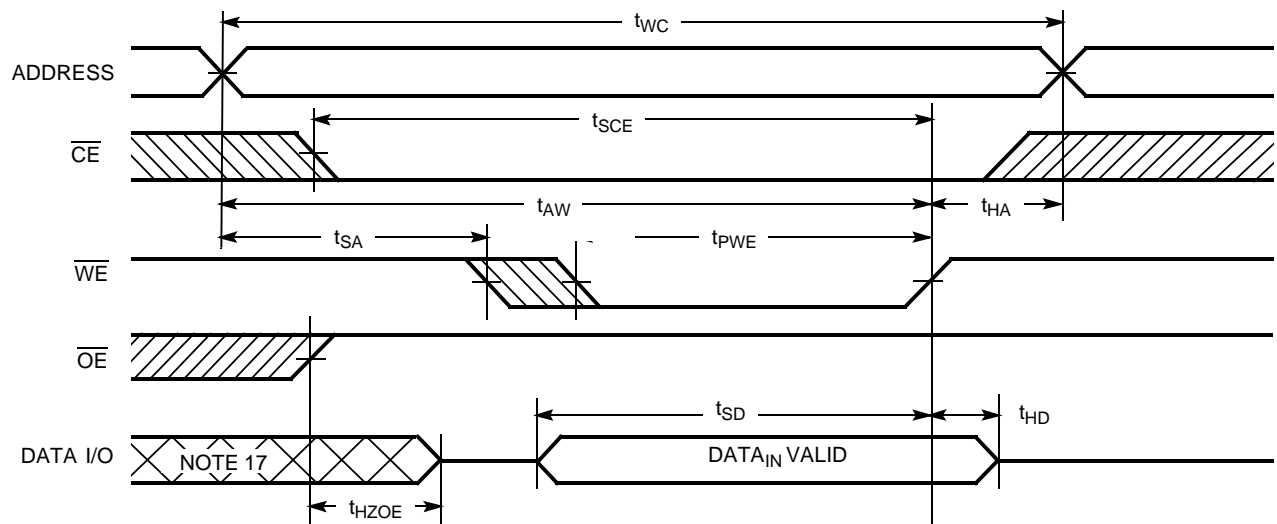
- V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.
- AC characteristics (except High-Z) for all 8-ns and 10-ns parts are tested using the load conditions shown in Figure (a). All other speeds are tested using the Thevenin load shown in Figure (b). High-Z characteristics are tested for all speeds using the test load shown in Figure (d).

AC Switching Characteristics^[6] Over the Operating Range

Parameter	Description	-8 ^[2]		-10		-12		-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
$t_{power}^{[7]}$	V_{CC} (typical) to the first access	1		1		1		1		μs
t_{RC}	Read Cycle Time	8		10		12		15		ns
t_{AA}	Address to Data Valid		8		10		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACE}	\overline{CE} LOW to Data Valid		8		10		12		15	ns
t_{DOE}	\overline{OE} LOW to Data Valid		4		5		6		7	ns
t_{LZOE}	\overline{OE} LOW to Low-Z	0		0		0		0		ns
t_{HZOE}	\overline{OE} HIGH to High-Z ^[8, 9]		4		5		6		7	ns
t_{LZCE}	\overline{CE} LOW to Low-Z ^[9]	3		3		3		3		ns
t_{HZCE}	\overline{CE} HIGH to High-Z ^[8, 9]		4		5		6		7	ns
t_{PU}	\overline{CE} LOW to Power-up	0		0		0		0		ns
t_{PD}	\overline{CE} HIGH to Power-down		8		10		12		15	ns
Write Cycle^[10, 11]										
t_{WC}	Write Cycle Time	8		10		12		15		ns
t_{SCE}	\overline{CE} LOW to Write End	6		7		8		10		ns
t_{AW}	Address Set-up to Write End	6		7		8		10		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		0		ns
t_{PWE}	\overline{WE} Pulse Width	6		7		8		10		ns
t_{SD}	Data Set-up to Write End	4		5		6		7		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	\overline{WE} HIGH to Low-Z ^[9]	3		3		3		3		ns
t_{HZWE}	\overline{WE} LOW to High-Z ^[8, 9]		4		5		6		7	ns

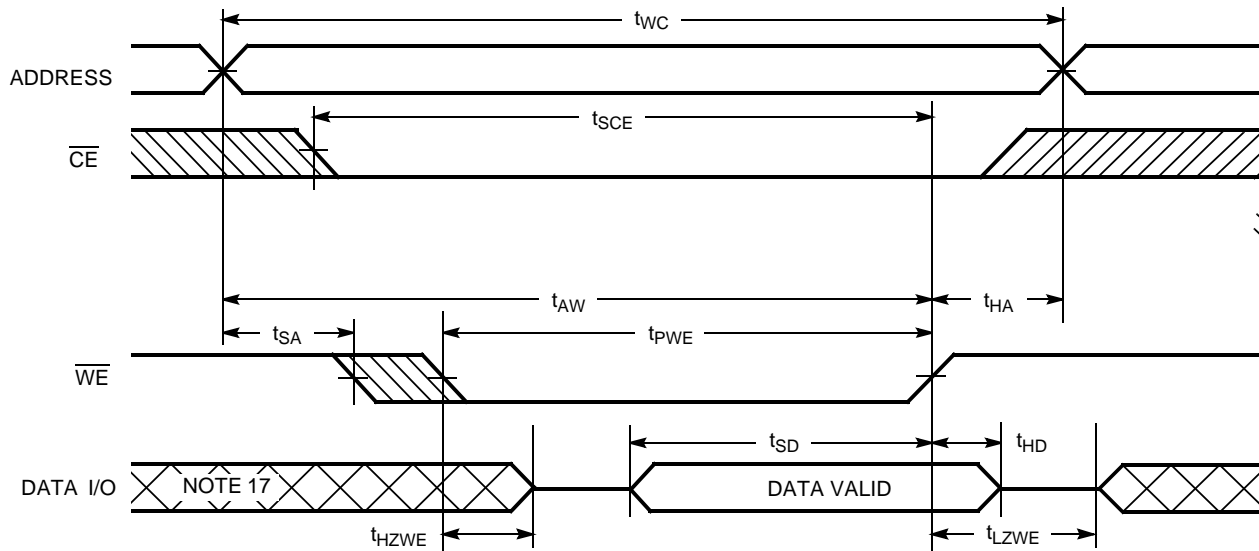
Switching Waveforms
Read Cycle No. 1^[12, 13]

Notes:

6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
7. t_{POWER} gives the minimum amount of time that the power supply should be at stable, typical V_{CC} values until the first memory access can be performed.
8. t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
10. The internal Write time of the memory is defined by the overlap of \overline{CE} LOW, and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a Write, and the transition of either of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
11. The minimum Write cycle time for Write Cycle No. 3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .
12. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{LL}$.
13. \overline{WE} is HIGH for Read cycle.

Switching Waveforms (continued)
Read Cycle No. 2 (\overline{OE} Controlled)^[13, 14]

Write Cycle No. 1 (\overline{WE} Controlled, \overline{OE} HIGH During Write)^[15, 16]

Notes:

14. Address valid prior to or coincident with \overline{CE} transition LOW.
15. Data I/O is high-impedance if $OE = V_{IH}$.
16. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.
17. During this period the I/Os are in the output state and input signals should not be applied.

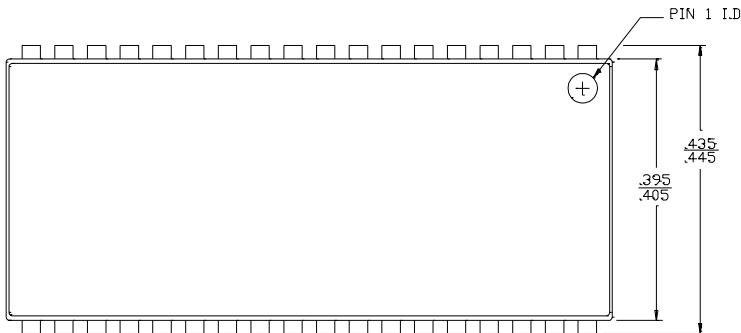
Switching Waveforms (continued)

Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} LOW)^[16]

Truth Table

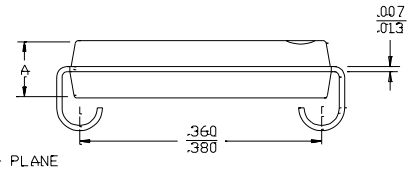
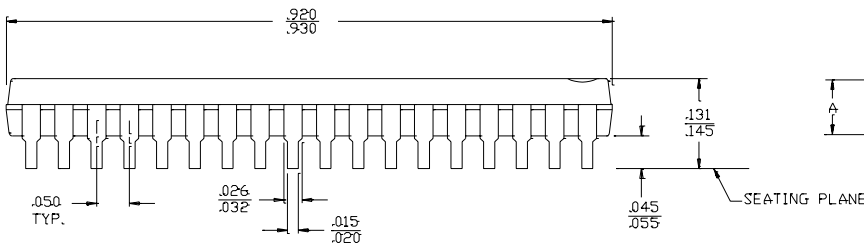
CE	OE	WE	I/O ₀ -I/O ₇	Mode	Power
H	X	X	High-Z	Power-down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High-Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1049CV33-10VC	V36	36-lead (400-Mil) Molded SOJ	Commercial
	CY7C1049CV33-10ZC	Z44	44-pin TSOP II	
	CY7C1049CV33-10VI	V36	36-lead (400-Mil) Molded SOJ	Industrial
	CY7C1049CV33-10ZI	Z44	44-pin TSOP II	
12	CY7C1049CV33-12VC	V36	36-lead (400-Mil) Molded SOJ	Commercial
	CY7C1049CV33-12ZC	Z44	44-pin TSOP II	
	CY7C1049CV33-12VI	V36	36-lead (400-Mil) Molded SOJ	Industrial
	CY7C1049CV33-12ZI	Z44	44-pin TSOP II	
15	CY7C1049CV33-15VC	V36	36-lead (400-Mil) Molded SOJ	Commercial
	CY7C1049CV33-15ZC	Z44	44-pin TSOP II	
	CY7C1049CV33-15VI	V36	36-lead (400-Mil) Molded SOJ	Industrial
	CY7C1049CV33-15ZI	Z44	44-pin TSOP II	

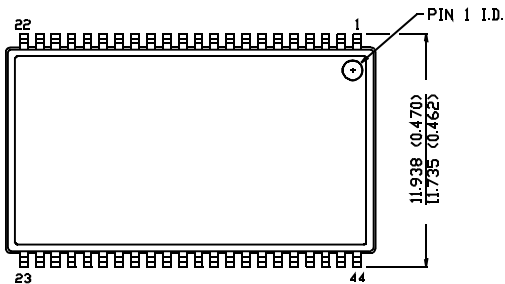
Package Diagrams
36-lead (400-mil) Molded SOJ V36

 DIMENSIONS IN INCHES
 MIN.
 MAX.

DIM. A	
ANAM	CSPI
.086	.095
.090	.115

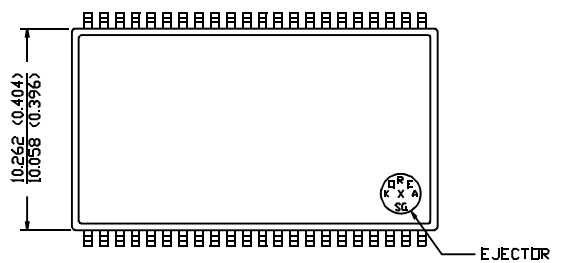


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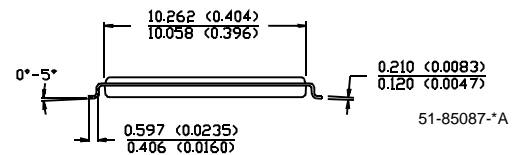
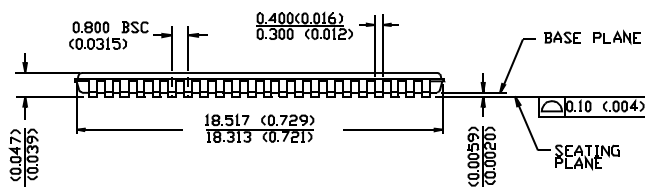
44-pin TSOP II Z44

 DIMENSION IN MM (INCH)
 MAX.
 MIN.


TOP VIEW



BOTTOM VIEW



51-85087-*A

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Document History Page

Document Title: CY7C1049CV33 512K x 8 Static RAM Document Number: 38-05006				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	112569	03/06/02	HGK	New Data Sheet
*A	114091	04/25/02	DFP	Changed Tpower unit from ns to μ s
*B	116479	09/16/02	CEA	Add applications foot note to data sheet, page 1.