HM6287, HM6287H Series

65536-word × 1-bit High Speed CMOS Static RAM

HITACHI

Description

The Hitachi HM6287/HM6287H is a high speed 64 k static RAM organized as 64-kword × 1-bit. It realizes high speed access time (25/35/45/55/70 ns) and low power consumption, employing CMOS process technology and high speed circuit design technology. It is most advantageous for high speed and high density memory, such as cache memory for mainframes or 32-bit MPUs. The HM6287/HM6287H is packaged in a 300-mil plastic DIP and SOJ, and is available for high density mounting. The low power version retains data with battery backup.

Features

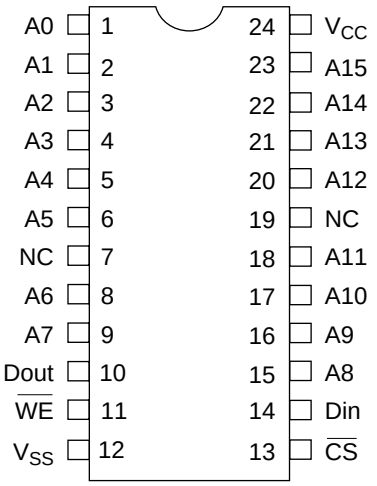
- Single 5 V supply and high density 22-pin DIP and 24-pin SOJ
- High speed: Fast access time 25/35/45/55/70 ns (max)
- Low power
  - — Operation: 300 mW (typ)
  - — Standby: 100 µW (typ)/10 µW (typ) (L-version)
- Completely static memory
- No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible: All inputs and outputs
- Battery backup capability (L-version)

Ordering Information

Type No.	Access Time	Package
HM6287P-45	45 ns	300-mil, 22-pin plastic DIP (DP-22N)
HM6287P-55	55 ns	
HM6287P-70	70 ns	
HM6287LP-45	45 ns	
HM6287LP-55	55 ns	
HM6287LP-70	70 ns	
HM6287HP-25	25 ns	300-mil, 22-pin plastic DIP (DP-22NB)
HM6287HP-35	35 ns	
HM6287HLP-25	25 ns	
HM6287HLP-35	35 ns	
HM6287HJP-25	25 ns	300-mil, 24-pin SOJ (CP-24D)
HM6287HJP-35	35 ns	
HM6287HLJP-25	25 ns	
HM6287HLJP-35	35 ns	

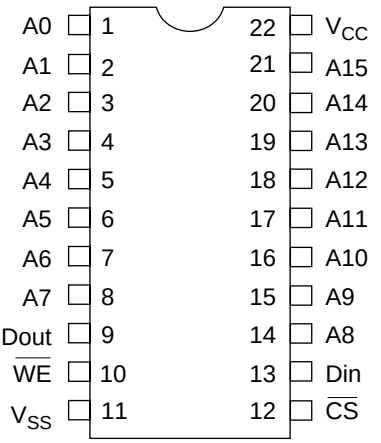
Pin Arrangement

HM6287P/HP Series



(Top view)

HM6287HJP

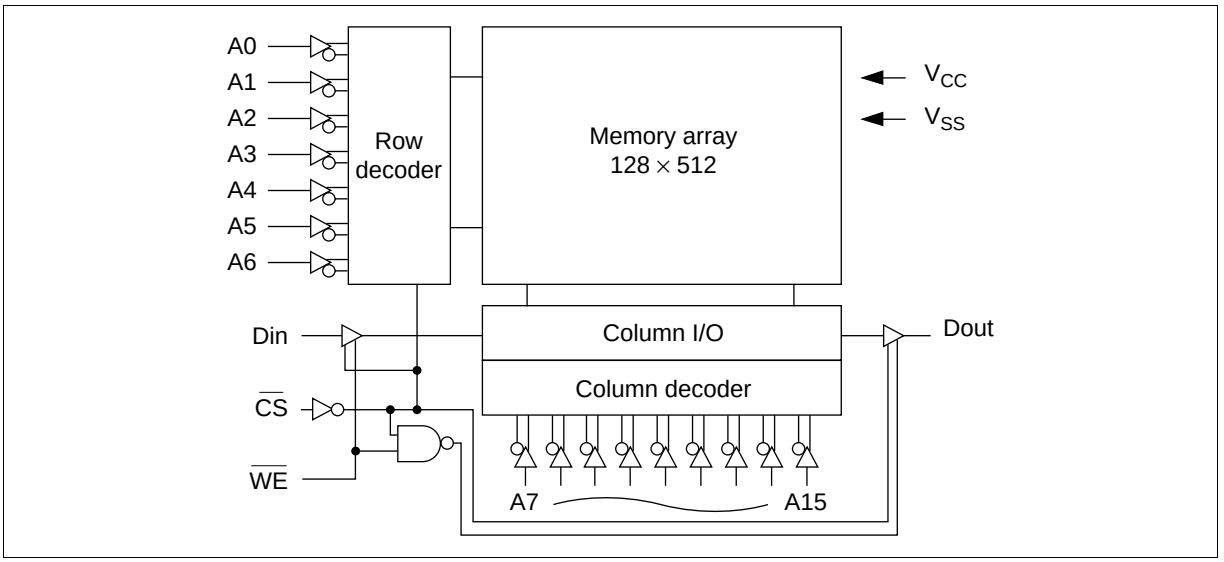


(Top view)

Pin Description

Pin Name	Function
A0–A15	Address
Din	Input
Dout	Output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} current	Dout pin	Ref. Cycle
H	×	Standby	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	I_{CC}	Dout	Read cycle 1, 2
L	L	Write	I_{CC}	High-Z	Write cycle 1, 2

Note: ×: Don't care.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage any pin relative to V_{SS}	V_T	–0.5* to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Note: V_T min: –3.5 V for pulse width ≤ 20 ns (HM6287 Series)
V_T min: –2.0 V for pulse width ≤ 10 ns (HM6287H Series)

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5*1	—	0.8	V

Note: 1. V_{IL} min: –3.0 V for pulse width ≤ 20 ns (HM6287 Series)
V_{IL} min: –2.0 V for pulse width ≤ 10 ns (HM6287H Series)

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM6287			HM6287H				
Parameter	Symbol	Min	Typ*1	Max	Min	Typ*1	Max	Unit	Test Conditions
Input leakage current	$\|I_{LI}\|$	—	—	2.0	—	—	2.0	µA	V_{CC} = Max Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	2.0	—	—	2.0	µA	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating V_{CC} current	I_{CC}	—	60	100	—	60	120	mA	$\overline{CS}$ = V_{IL}, Iout = 0 mA, min cycle
Standby V_{CC} current	I_{SB}	—	10	30	—	15	30	mA	$\overline{CS}$ = V_{IH}, min. cycle
Standby V_{CC} current (1)	I_{SB1}	— —	0.02 0.02*2	2.0 0.1*2	— —	0.02 0.02*2	2.0 0.1*2	mA mA	$\overline{CS}$ ≥ V_{CC} – 0.2 V 0 V ≤ Vin ≤ 0.2 V or V_{CC} – 0.2 V ≤ V_{in}
Output low voltage	V_{OL}	—	—	0.4	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	2.4	—	—	V	I_{OH} = –4.0 mA

Notes: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and not guaranteed.
2. These characteristics are guaranteed only for L-version.

Capacitance (Ta = 25°C, f = 1.0 MHz)[*1]

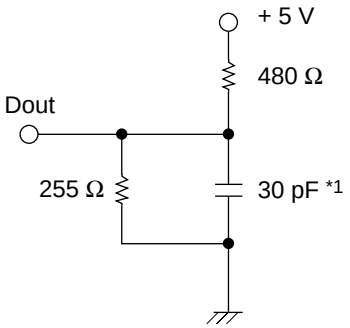
		HM6287		HM6287H			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Input capacitance	Cin	—	5	—	6	pF	Vin = 0 V
Output capacitance	Cout	—	7.5	—	8	pF	Vout = 0 V

Note: 1. These parameters are sampled and not 100% tested.

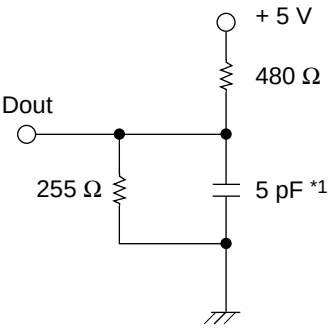
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input and output timing reference levels: 1.5 V
- Input rise and fall time: 5 ns
- Output load: See figure



Output load (A)



Output load (B)
(for t_{HZ}, t_{LZ}, t_{WZ} and t_{OW})

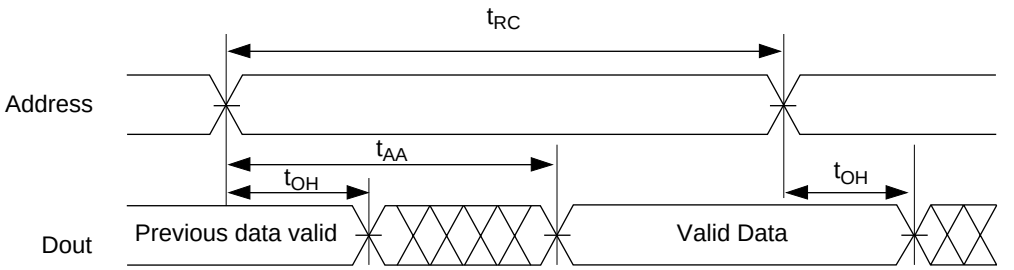
Note: 1. Including scope and jig

Read Cycle

		HM6287H-25		HM6287H-35		HM6287-45		HM6287-55		HM6287-70			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read cycle time	t_{RC}	25	—	35	—	45	—	55	—	70	—	ns	2
Address access time	t_{AA}	—	25	—	35	—	45	—	55	—	70	ns	
Chip select access time	t_{ACS}	—	25	—	35	—	45	—	55	—	70	ns	
Output hold from address change	t_{OH}	3	—	5	—	5	—	5	—	5	—	ns	
Chip selection to output in low-Z	t_{LZ}	5	—	5	—	5	—	5	—	5	—	ns	1, 3, 4
Chip deselection to output in high-Z	t_{HZ}	0	12	0	20	0	30	0	30	0	30	ns	1, 3, 4
Chip selection to power-up time	t_{PU}	0	—	0	—	0	—	0	—	0	—	ns	4
Chip deselection to power down time	t_{PD}	—	25	—	30	—	40	—	40	—	40	ns	4

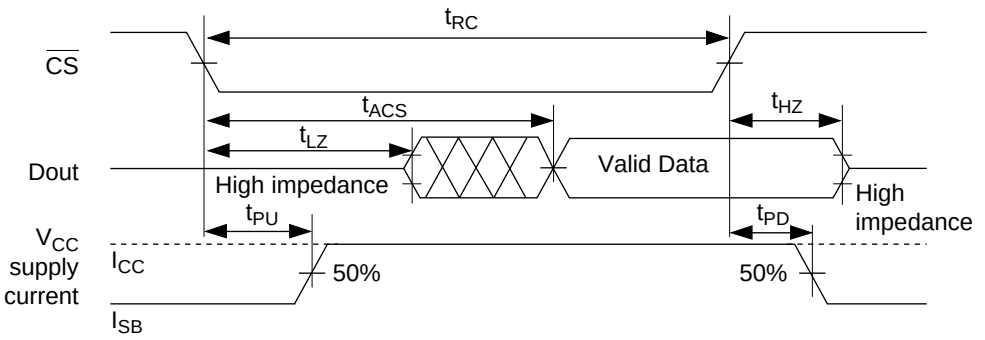
Notes: 1. Transistion is measured +200 mV from steady state voltage with load (B).
2. All read cycle timing is referenced from last valid address to the first transitioning address.
3. At any given temperature and voltage condition, t_{HZ} max, is less the t_{LZ} min both for a given device and from device to device.
4. These parameters are sampled and not 100% tested.

Read Timing Waveform (1)



Notes: 1. $\overline{WE}$ is high for read cycle.
2. Device is continously selected, $\overline{CS}$ = V_{IL}.
3. All read cycle timing is referred from last valid address to the first transitioning address.

Read Timing Waveform (2)



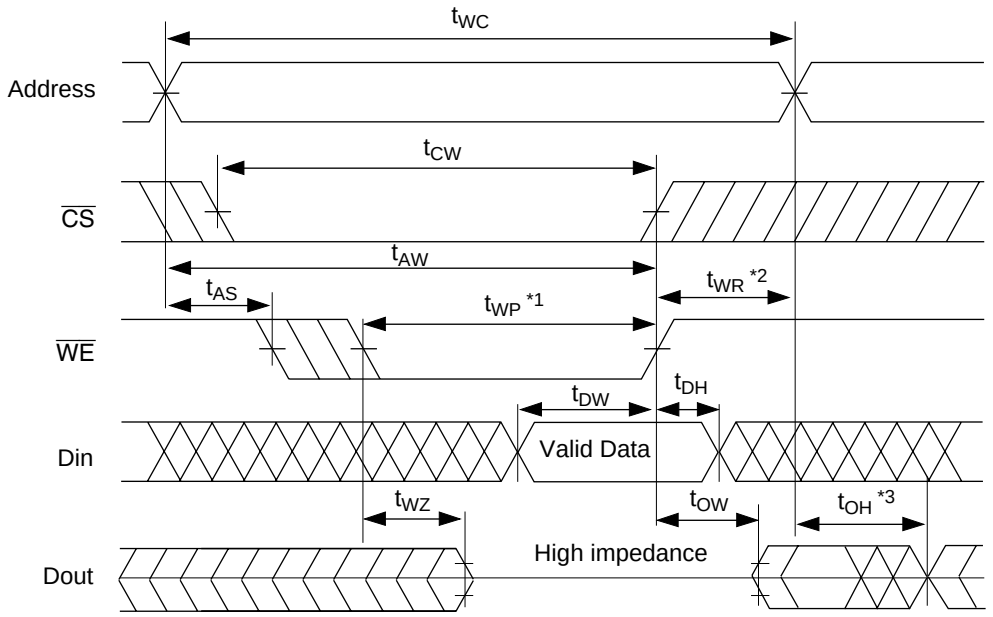
Notes: 1. $\overline{WE}$ is high for read cycle.
2. Address valid prior to or coincident with $\overline{CS}$ transistion low.

Write Cycle

		HM6287H-25		HM6287H-35		HM6287-45		HM6287-55		HM6287-70			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write cycle time	t_{WC}	25	—	35	—	45	—	55	—	70	—	ns	1
Chip selection to endof write	t_{CW}	20	—	30	—	40	—	50	—	55	—	ns	
Address valid to end of write	t_{AW}	20	—	30	—	40	—	50	—	55	—	ns	
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	
Write pulse width	t_{WP}	20	—	30	—	25	—	35	—	40	—	ns	
Write recovery time	t_{WR}	0	—	0	—	0	—	0	—	0	—	ns	
Data valid to end of write	t_{DW}	15	—	20	—	25	—	25	—	30	—	ns	
Data hold time	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	
Write enabled to output in high-Z	t_{WZ}	0	8	0	10	0	25	0	25	0	30	ns	2
Output active from end of write	t_{OW}	5	—	5	—	0	—	0	—	0	—	ns	2

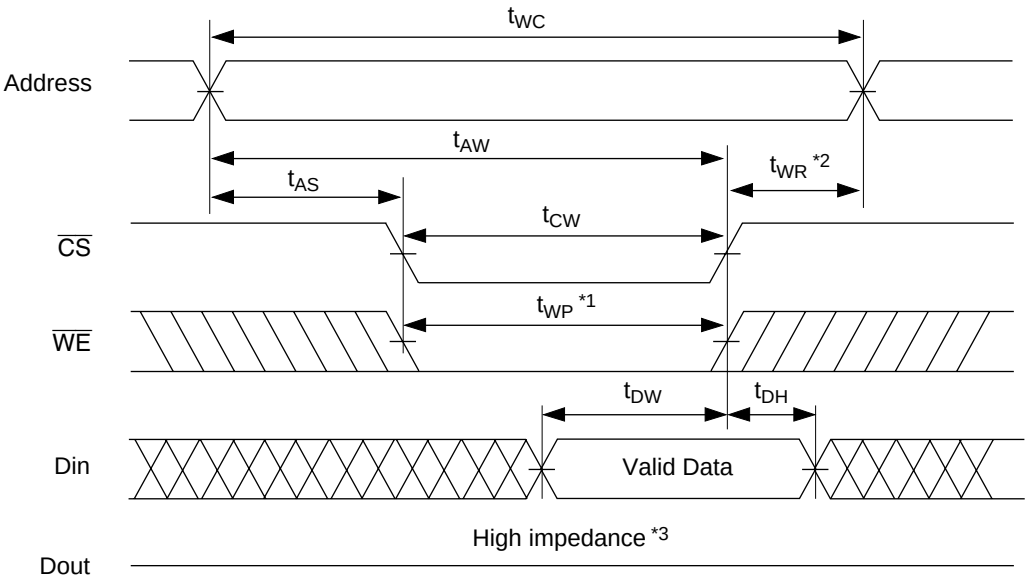
Notes: 1. All write cycle timing is referenced from the last valid address to first transitioning address.
2. Transition is measured ±200 mV from steady state voltage with load B. These parameters are sampled and not 100% tested.

Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
3. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

Write Timing Waveform (2) ($\overline{CS}$ Controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
3. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.

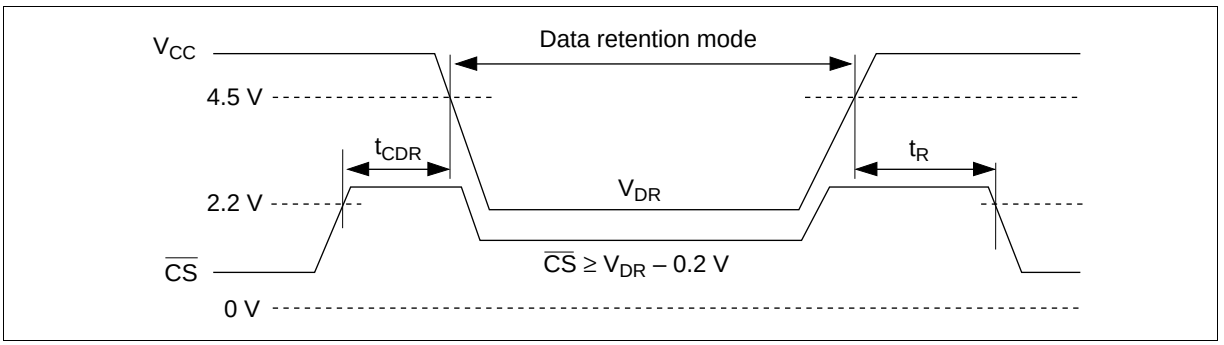
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

These specifications are guaranteed only for L-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, 0 V ≥ Vin – 0.2 V, or 0 V ≤ Vin ≤ 0.2V
Data retention current	I_{CCDR}	—	—	50*2	µA	
		—	—	35*3	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*1	—	—	ns	

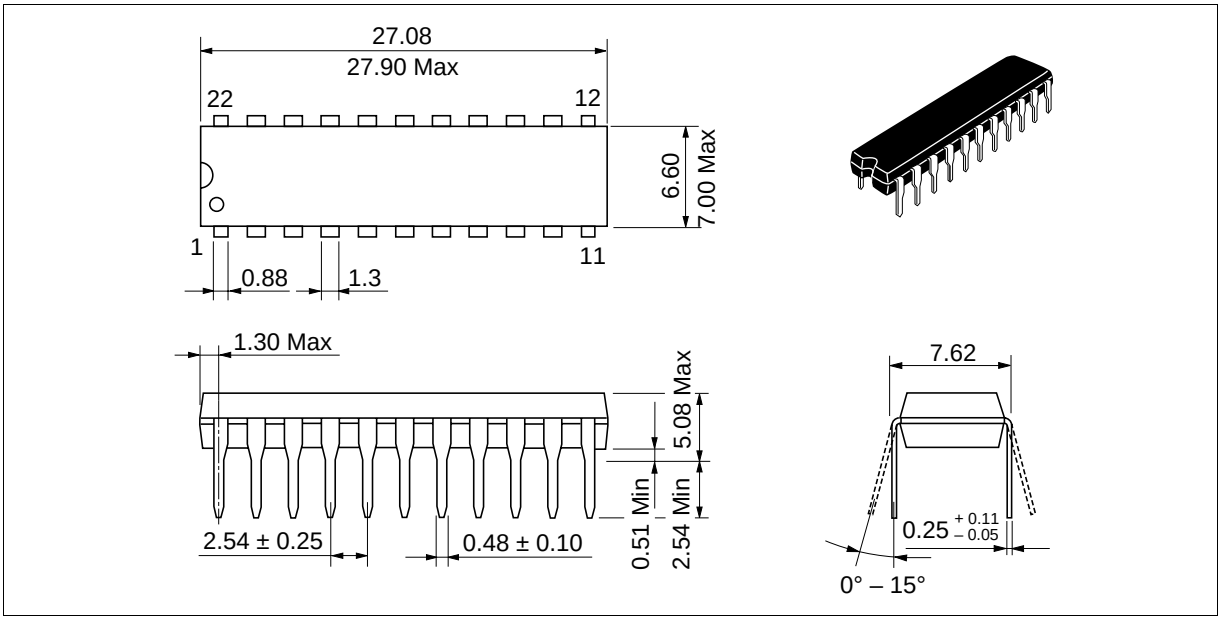
Notes: 1. t_{RC} = Read cycle time
2. V_{CC} = 3.0 V
3. V_{CC} = 2.0 V

Low V_{CC} Data Retention Waveform

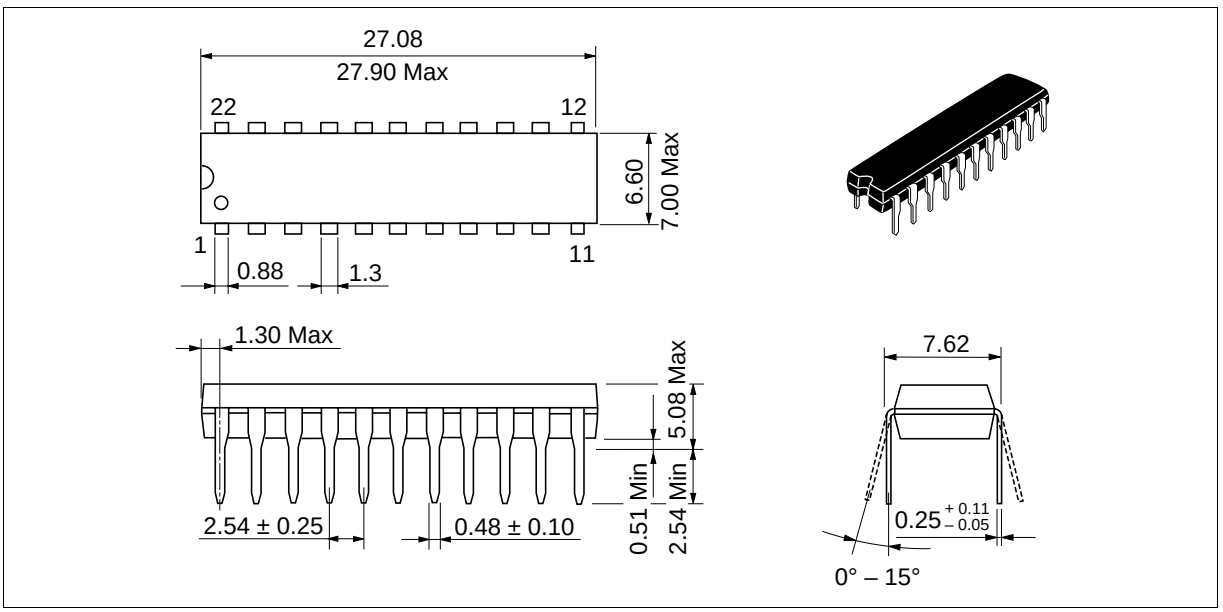


Package Dimensions

HM6287P/LP Series (DP-22N) Unit: mm



HM6287HP/HLP Series (DP-22NB) Unit: mm



HM6287HJP/HLJP Series (CP-24D) Unit: mm