Ultralow Noise Push-Pull DC/DC Controller

FEATURES

- **Greatly Reduced Conducted and Radiated EMI**
- **Low Switching Harmonic Content**
- **Independent Control of Output Switch Voltage and Current Slew Rates**
- **Greatly Reduced Need for External Filters**
- Dual N-Channel MOSFET Drivers
- 20kHz to 250kHz Oscillator Frequency
- Easily Synchronized to External Clock
- Regulates Positive and Negative Voltages
- Easier Layout Than with Conventional Switchers

APPLICATIONS

- Power Supplies for Noise Sensitive Communication Equipment
- EMI Compliant Offline Power Supplies
- Precision Instrumentation Systems
- Isolated Supplies for Industrial Automation
- Medical Instruments
- Data Acquisition Systems

DESCRIPTION

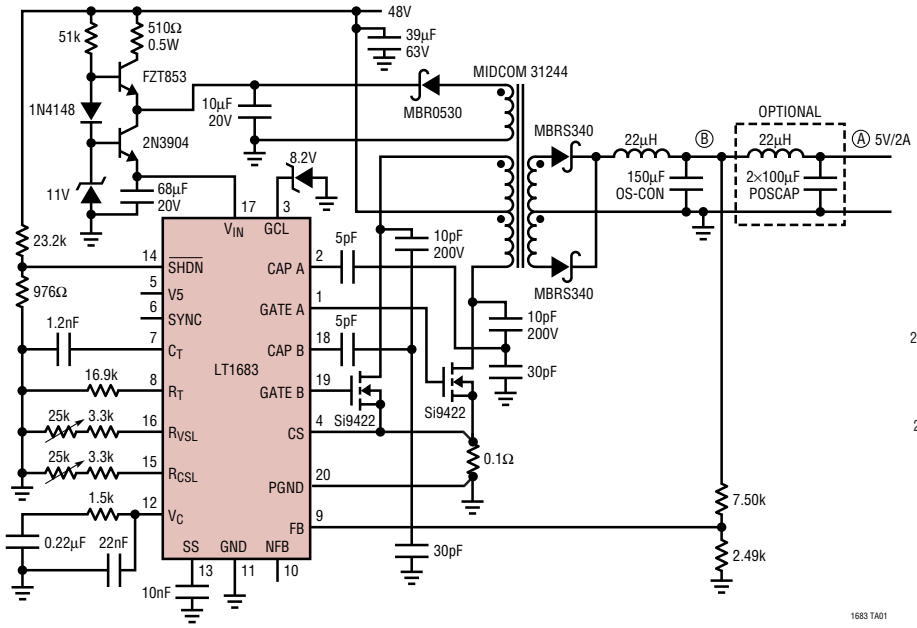
The LT®1683 is a switching regulator controller designed to lower conducted and radiated electromagnetic interference (EMI). Ultralow noise and EMI are achieved by controlling the voltage and current slew rates of external N-channel MOSFET switches. Current and voltage slew rates can be independently set to optimize harmonic content of the switching waveforms vs efficiency. The LT1683 can reduce high frequency harmonic power by as much as 40dB with only minor losses in efficiency.

The LT1683 utilizes a dual output (push-pull) current mode architecture optimized for low noise topologies. The IC includes gate drivers and all necessary oscillator, control and protection circuitry. Unique error amp circuitry can regulate both positive and negative voltages. The oscillator may be synchronized to an external clock for more accurate placement of switching harmonics.

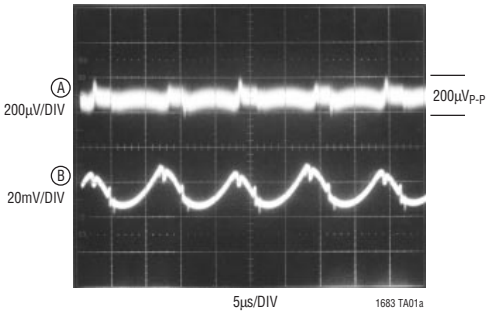
Protection features include gate drive lockout for low V_{IN}, opposite gate lockout, soft-start, output current limit, short-circuit current limiting, gate drive overvoltage clamp and input supply undervoltage lockout.

TYPICAL APPLICATION

Ultralow Noise 48V to 5V DC/DC Converter



5V Output Noise (Bandwidth = 100MHz)

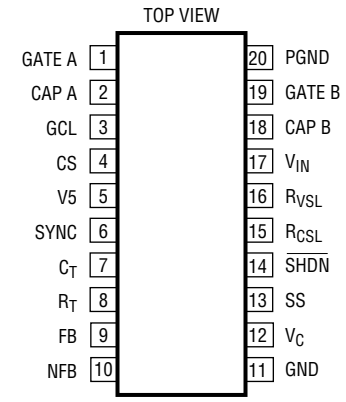


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{IN}) 20V
Gate Drive Current ..... Internal Limit
V5 Current ..... Internal Limit
$\overline{SHDN}$ Pin Voltage 20V
Feedback Pin Voltage (Trans. 10ms) ..... ±10V
Feedback Pin Current 10mA
Negative Feedback Pin Voltage (Trans. 10ms) ..... ±10V
CS Pin 5V
GCL Pin 16V
SS Pin 3V
Operating Junction Temperature Range
(Note 3) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
20-LEAD PLASTIC SSOP

T_{JMAX} = 150°C, θ_{JA} = 110°C/W

ORDER PART NUMBER
LT1683EG
LT1683IG

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, V_C = 0.9V, V_{FB} = V_{REF}, R_{VSL}, R_{CSL} = 16.9k, R_T = 16.9k and other pins open unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Error Amplifiers							
V_{REF}	Reference Voltage	Measured at Feedback Pin	●	1.235	1.250	1.265	V
I_{FB}	Feedback Input Current	V_{FB} = V_{REF}	●		250	1000	nA
FB_{REG}	Reference Voltage Line Regulation	2.7V ≤ V_{IN} ≤ 20V	●		0.012	0.03	%/V
V_{NFR}	Negative Feedback Reference Voltage	Measured at Negative Feedback Pin with Feedback Pin Open	●	–2.56	–2.500	–2.45	V
I_{NFR}	Negative Feedback Input Current	V_{NFB} = V_{NFR}		–37	–25		µA
NFB_{REG}	Negative Feedback Reference Voltage Line Regulation	2.7V ≤ V_{IN} ≤ 20V	●		0.009	0.03	%/V
g_m	Error Amplifier Transconductance	ΔI_C = ±50µA	 ●	1100 700	1500	2200 2500	µmho µmho
I_{ESK}	Error Amp Sink Current	V_{FB} = V_{REF} + 150mV, V_C = 0.9V	●	120	200	350	µA
I_{ESRC}	Error Amp Source Current	V_{FB} = V_{REF} – 150mV, V_C = 0.9V	●	120	200	350	µA
V_{CLH}	Error Amp Clamp Voltage	High Clamp, V_{FB} = 1V			1.27		V
V_{CLL}	Error Amp Clamp Voltage	Low Clamp, V_{FB} = 1.5V			0.12		V
A_V	Error Amplifier Voltage Gain			180	250		V/V
FB_{OV}	FB Overvoltage Shutdown	Outputs Drivers Disabled			1.47		V
I_{SS}	Soft-Start Charge Current	V_{SS} = 1V			9.0	12	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, V_C = 0.9V, V_{FB} = V_{REF}, R_{VSL}, R_{CSL} = 16.9k, R_T = 16.9k and other pins open unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Oscillator and Sync							
f_{MAX}	Max Switch Frequency				250		kHz
f_{SYNC}	Synchronization Frequency Range	Oscillator Frequency = 250kHz		290			kHz
V_{SYNC}	SYNC Pin Input Threshold		●	0.7	1.4	2.0	
R_{SYNC}	SYNC Pin Input Resistance				40		kΩ
Gate Drives (Specifications Apply to Either A or B Unless Otherwise Noted)							
DC_{MAX}	Maximum Switch Duty Cycle	R_{VSL} = R_{CSL} = 4.85k, Osc Frequency = 25kHz	●	45	46		%
VG_{ON}	Gate On Voltage	V_{IN} = 12, GCL = 12 V_{IN} = 12, GCL = 8		10 7.6	10.4 7.9	10.7 8.1	V V
VG_{OFF}	Gate Off Voltage	V_{IN} = 12V			0.2	0.35	V
IG_{SO}	Max Gate Source Current	V_{IN} = 12V		0.3			A
IG_{SK}	Max Gate Sink Current	V_{IN} = 12V		0.3			A
V_{INUVLO}	Gate Drive Undervoltage Lockout (Note 5)	V_{GCL} = 6.5V, Gates Enabled			7.3	7.5	V
Current Sense							
t_{IBL}	Switch Current Limit Blanking Time				100		ns
V_{SENSE}	Sense Voltage Shutdown Voltage	V_C Pulled Low	●	86	103	120	mV
V_{SENSEF}	Sense Voltage Fault Threshold		●		230	300	mV
Slew Control (for the Following Slew Tests See Test Circuit in Figure 1b)							
V_{SLEWR}	Output Voltage Slew Rising Edge	R_{VSL} = R_{CSL} = 17k			26		V/µs
V_{SLEWF}	Output Voltage Slew Falling Edge	R_{VSL} = R_{CSL} = 17k			19		V/µs
VI_{SLEWR}	Output Current Slew Rising Edge (CS Pin Voltage)	R_{VSL} = R_{CSL} = 17k			2.1		V/µs
VI_{SLEWF}	Output Current Slew Falling Edge (CS Pin Voltage)	R_{VSL} = R_{CSL} = 17k			2.1		V/µs
Supply and Protection							
V_{INMIN}	Minimum Input Voltage (Note 4)	V_{GCL} = V_{IN}	●		2.55	3.6	V
I_{VIN}	Supply Current (Note 2)	R_{VSL} = R_{CSL} = 17k, V_{IN} = 12 R_{VSL} = R_{CSL} = 17k, V_{IN} = 20	● ●		25 35	45 55	mA mA
V_{SHDN}	Shutdown Turn-On Threshold		●	1.31	1.39	1.48	V
ΔV_{SHDN}	Shutdown Turn-On Voltage Hysteresis		●	50	110	180	mV
I_{SHDN}	Shutdown Input Current Hysteresis		●	10	24	35	µA
V5	5V Reference Voltage	6.5V ≤ V_{IN} ≤ 20V, IV5 = 5mA 6.5V ≤ V_{IN} ≤ 20V, IV5 = –5mA		4.85 4.80	5 5	5.20 5.15	V V
$IV5_{SC}$	5V Reference Short-Circuit Current	V_{IN} = 6.5V Source V_{IN} = 6.5V Sink		10 –10			mA mA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Supply current specification includes loads on each gate as in Figure 1a. Actual supply currents vary with operating frequency, operating voltages, V5 load, slew rates and type of external FET.

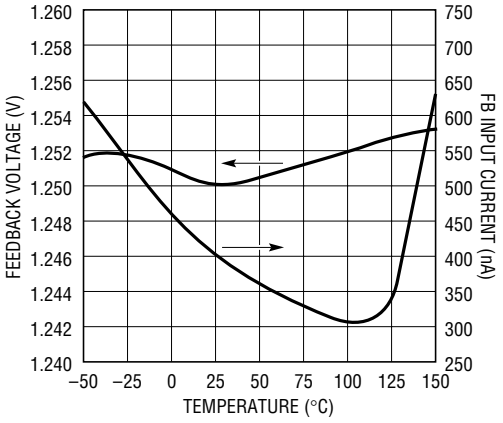
Note 3: The LT1683E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 125°C operating range are assured by design, characterization and correlation with statistical process controls. The LT1683I is guaranteed and tested over the –40° to 125° operating temperature range.

Note 4: Output gate drivers will be enabled at this voltage. The GCL voltage will also determine drivers' activity.

Note 5: Gate drivers are ensured to be on when V_{IN} is greater than the maximum value.

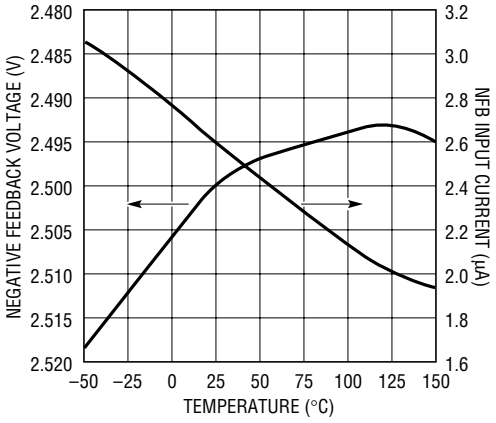
TYPICAL PERFORMANCE CHARACTERISTICS

Feedback Voltage and Input Current vs Temperature



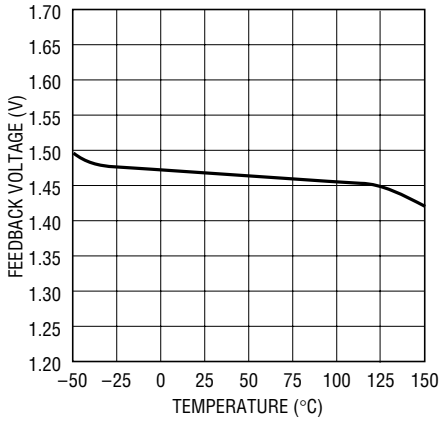
1683 G01

Negative Feedback Voltage and Input Current vs Temperature



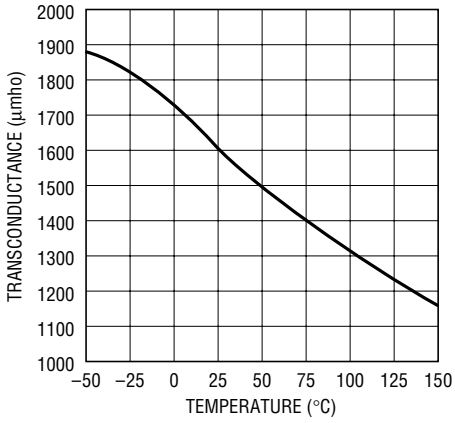
1683 G02

Feedback Overvoltage Shutdown vs Temperature



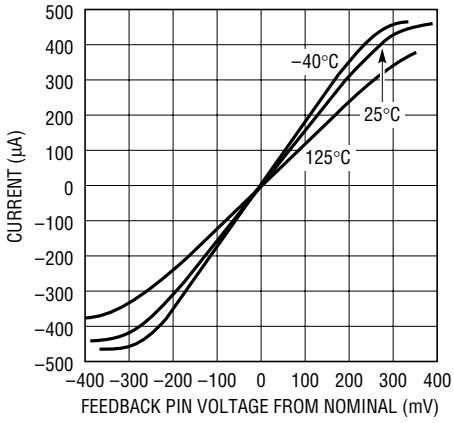
1683 G03

Error Amp Transconductance vs Temperature



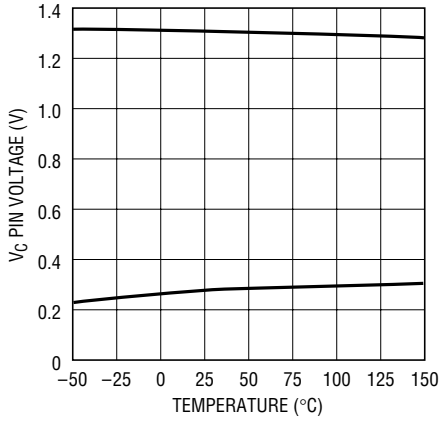
1683 G04

Error Amp Output Current vs Feedback Pin Voltage from Nominal



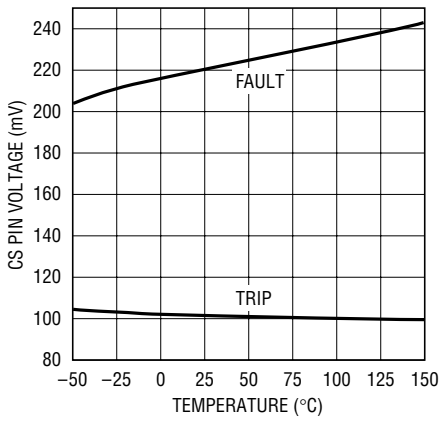
1683 G05

V_C Pin Threshold and Clamp Voltage vs Temperature



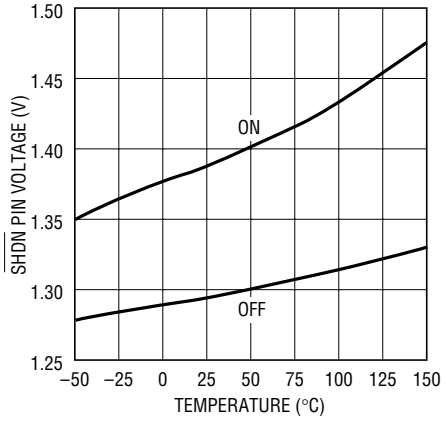
1683 G06

CS Pin Trip and CS Fault Voltage vs Temperature



1683 G07

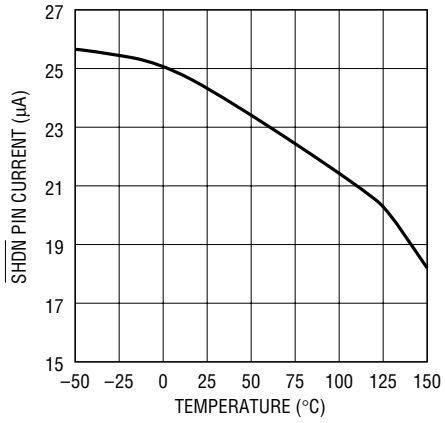
$\overline{SHDN}$ Pin On and Off Thresholds vs Temperature



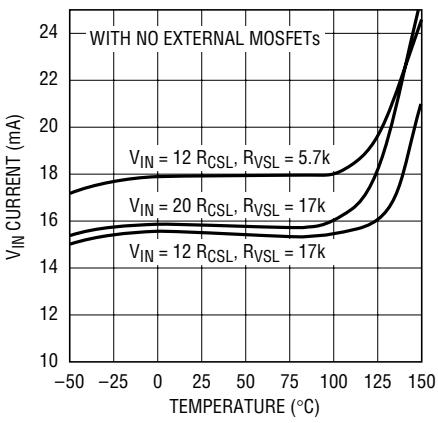
1683 G08

TYPICAL PERFORMANCE CHARACTERISTICS

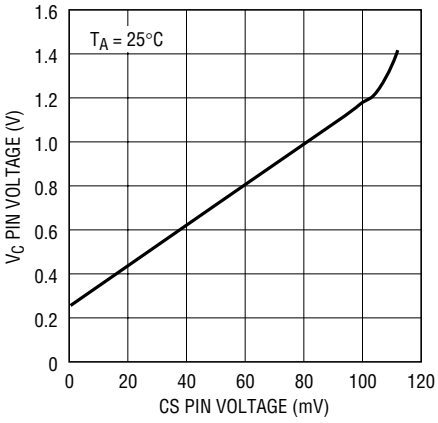
$\overline{SHDN}$ Pin Hysteresis Current vs Temperature



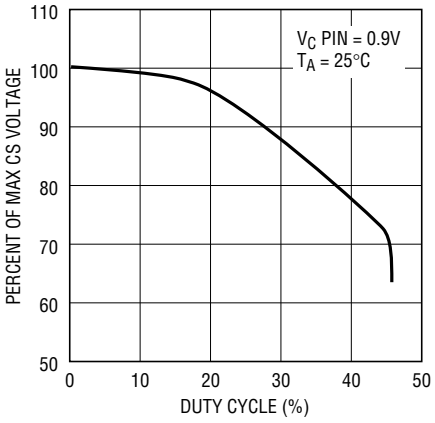
V_{IN} Current vs Temperature



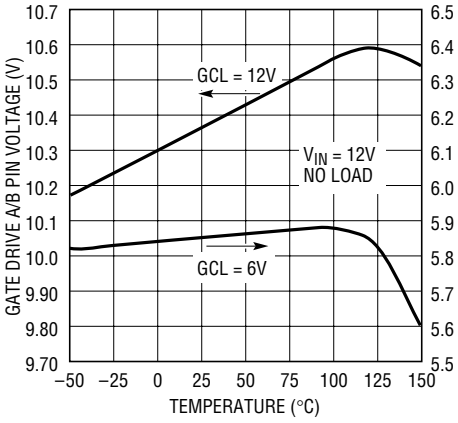
CS Pin to V_C Pin Transfer Function



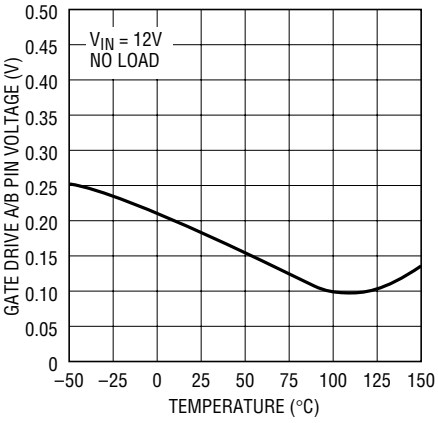
Slope Compensation



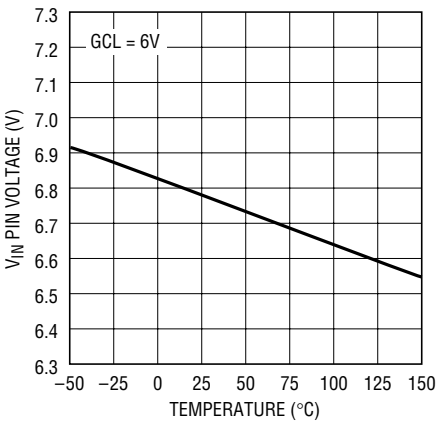
Gate Drive A/B High Voltage vs Temperature



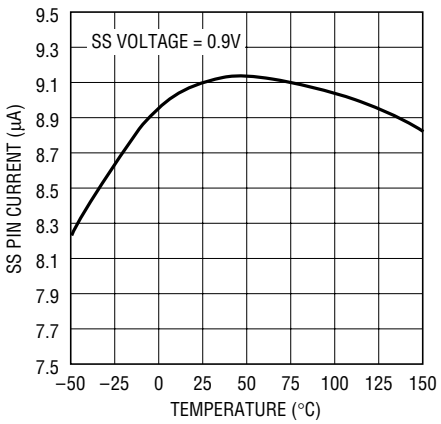
Gate Drive A/B Low Voltage vs Temperature



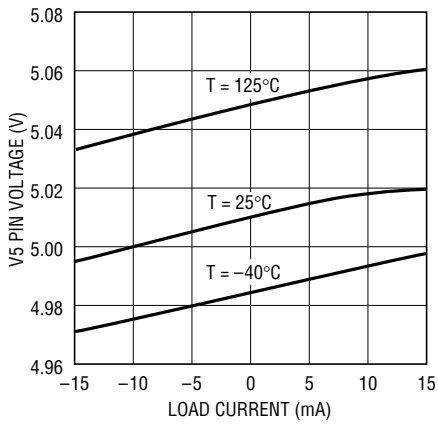
Gate Drive Undervoltage Lockout Voltage vs Temperature



Soft-Start Current vs Temperature



V5 Voltage vs Load Current



PIN FUNCTIONS

Part Supply

V5 (Pin 5): This pin provides a 5V output that can sink or source 10mA for use by external components. V5 source current comes from V_{IN} . Sink current goes to GND. V_{IN} must be greater than 6.5V in order for this voltage to be in regulation. If this pin is used, a small capacitor (<1µF) may be placed on this pin to reduce noise. This pin can be left open if not used.

GND (Pin 11): Signal Ground. The internal error amplifier, negative feedback amplifier, oscillator, slew control circuitry, V5 regulator, current sense and the bandgap reference are referred to this ground. Keep the connection to this pin, the feedback divider and V_C compensation network free of large ground currents.

$\overline{\text{SHDN}}$ (Pin 14): The shutdown pin can disable the switcher. Grounding this pin will disable all internal circuitry.

Increasing $\overline{\text{SHDN}}$ voltage will initially turn on the internal bandgap regulator. This provides a precision threshold for the turn on of the rest of the IC. As $\overline{\text{SHDN}}$ increases past 1.39V the internal LDO regulator turns on, enabling the control and logic circuitry.

24µA of current is sourced out of the pin above the turn on threshold. This can be used to provide hysteresis for the shutdown function. The hysteresis voltage will be set by the Thevenin resistance of the resistor divider driving this pin times the current sourced out. Above approximately 2.1V the hysteresis current is removed. There is approximately 0.1V of voltage hysteresis on this pin as well.

The pin can be tied high (to V_{IN} for instance).

V_{IN} (Pin 17): Input Supply. All supply current for the part comes from this pin including gate drives and V5 regulator. Charge current for gate drives can produce current pulses of hundreds of milliamperes. Bypass this pin with a low ESR capacitor.

When V_{IN} is below 2.55V the part will go into supply undervoltage lockout where the gate drivers are driven low. This, along with gate drive undervoltage lockout, prevents unpredictable behavior during power up.

PGND (Pin 20): Power Driver Ground. This ground comes from the MOSFET gate drivers. This pin can have several hundred milliamperes of current on it when the external MOSFETs are being turned off.

Oscillator

SYNC (Pin 6): The SYNC pin can be used to synchronize the part to an external clock. The oscillator frequency should be set close to the external clock frequency. Synchronizing the clock to an external reference is useful for creating more stable positioning of the switcher voltage and current harmonics. This pin can be left open or tied to ground if not used.

C_T (Pin 7): The oscillator capacitor pin is used in conjunction with R_T to set the oscillator frequency. For R_T = 16.9k:

$$C_{OSC}(nf) = 129/f_{OSC}(kHz)$$

R_T (Pin 8): The oscillator resistor pin is used to set the charge and discharge currents of the oscillator capacitor. The nominal value is 16.9k. It is possible to adjust this resistance ±25% to set oscillator frequency more accurately.

PIN FUNCTIONS

Gate Drive

GATE A, GATE B (Pins 1, 19): These pins connect to the gates of the external N-channel MOSFETs. GATE A and GATE B turn on with alternate clock cycles. These drivers are capable of sinking and sourcing at least 300mA.

The GCL pin sets the upper voltage of the gate drive. The gate pins will not be activated until V_{IN} reaches a minimum voltage as defined by the GCL pin (gate undervoltage lockout).

The gate drive outputs have current limit protection to safe guard against accidental shorts.

If the gate drive voltage is greater than about 1V the opposite gate drive is inhibited thus preventing cross conduction.

GCL (Pin 3): This pin sets the maximum gate voltage to the GATE A and GATE B pins to the MOSFET gate drives. This pin should be either tied to a Zener, a voltage source or V_{IN}.

If the pin is tied to a Zener or a voltage source, the maximum gate drive voltage will be approximately $V_{GCL} – 0.2V$. If it is tied to V_{IN}, the maximum gate voltage is approximately $V_{IN} – 1.6$.

Approximately 50µA of current can be sourced from this pin if $V_{GCL} < V_{IN} – 0.8V$.

This pin also controls undervoltage lockout of the gate drives. If the pin is tied to a Zener or voltage source, the gate drive will not be enabled until $V_{IN} > V_{GCL} + 0.8V$. If this pin is tied to V_{IN}, then undervoltage lockout is disabled.

There is an internal 19V Zener tied from this pin to ground to provide a fail-safe for maximum gate voltage.

Slew Control

CAP A, CAP B (Pins 2, 18): These pins are the feedback nodes for the external voltage slewing capacitors. Normally a small 1pf to 5pf capacitor is connected from this pin to the drain of its respective MOSFET.

The voltage slew rate is inversely proportional to this capacitance and proportional to the current that the part will sink and source on this pin. That current is inversely proportional to R_{VSL}.

R_{CSL} (Pin 15): A resistor to ground sets the current slew rate for the external drive MOSFETs during switching. The minimum resistor value is 3.3k and the maximum value is 68k. The time to slew between on and off states of the MOSFET current will determine how the di/dt related harmonics are reduced. This time is proportional to R_{CSL} and R_S (the current sense resistor) and maximum current. Longer times produce a greater reduction of higher frequency harmonics.

R_{VSL} (Pin 16): A resistor to ground sets the voltage slew rate for the drains of the external drive MOSFETs. The minimum resistor value is 3.3k and the maximum value is 68k. The time to slew between on and off states on the MOSFET drain voltage will determine how harmonics are reduced from this source. This time is proportional to R_{VSL}, $C_{VA/B}$ and the input voltage. Longer times produce more rolloff of harmonics. $C_{VA/B}$ is the equivalent capacitance from CAP A or B to the drain of the MOSFET.

Switch Mode Control

SS (Pin 3): The SS pin allows for ramping of the switch current threshold at startup. Normally a capacitor is placed on this pin to ground. An internal 9µA current source will charge this capacitor up. The voltage on the V_C pin cannot exceed the voltage on SS. Thus peak current will ramp up as the SS pin ramps up. During a short circuit fault the SS pin will be discharged to ground thus reinitializing soft-start.

When SS is below the V_C clamp voltage the V_C pin will closely track the SS pin.

This pin can be left open if not used.

PIN FUNCTIONS

CS (Pin 4): This is the input to the current sense amplifier. It is used for both current mode control and current slewing of the external MOSFETs. Current sense is accomplished via a sense resistor (R_S) connected from the sources of the external MOSFETs to ground. CS is connected to the top of R_S. Current sense is referenced to the GND pin.

The switch maximum operating current will be equal to 0.1V/R_S. At CS = 0.1V, the gate drivers will be immediately turned off (no slew control).

If CS = 0.22V in addition to the drivers being turned off, V_C and SS will be discharged to ground (short-circuit protection). This will hasten turn off on subsequent cycles.

FB (Pin 9): The feedback pin is used for positive voltage sensing. It is the inverting input to the error amplifier. The noninverting input of this amplifier connects internally to a 1.25V reference.

If the voltage on this pin exceeds the reference by 220mV, then the output drivers will immediately turn off the external MOSFETs (no slew control). This provides for output overvoltage protection

When this input is below 0.9V then the current sense blanking will be disabled. This will assist start up.

NFB (Pin 10): The negative feedback pin is used for sensing a negative output voltage. The pin is connected to the inverting input of the negative feedback amplifier through a 100k source resistor. The negative feedback amplifier provides a gain of –0.5 to the FB pin. The nominal regulation point would be –2.5V on NFB. This pin should be left open if not used.

If NFB is being used then overvoltage protection will occur at 0.44V below the NFB regulation point.

At NFB < –1.8 current sense blanking will be disabled.

V_C (Pin 12): The compensation pin is used for frequency compensation and current limiting. It is the output of the error amplifier and the input of the current comparator. Loop frequency compensation can be performed with an RC network connected from the V_C pin to ground. The voltage on V_C is proportional to the switch peak current. The normal range of voltage on this pin is 0.25V to 1.27V. However, during slope compensation the upper clamp voltage is allowed to increase with the compensation.

During a short-circuit fault the V_C pin will be discharged to ground.

TEST CIRCUITS

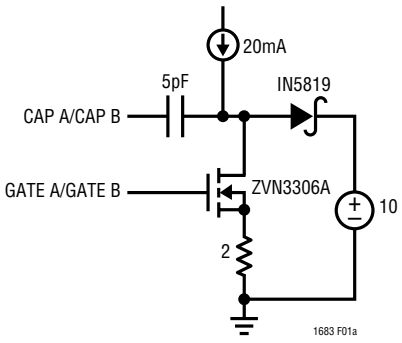


Figure 1a. Typical Test Circuitry

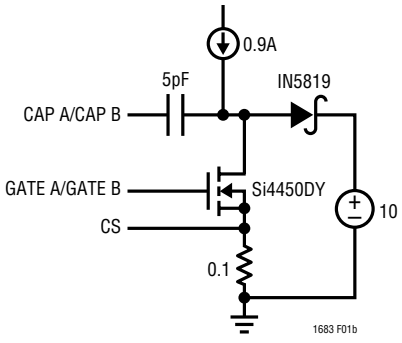
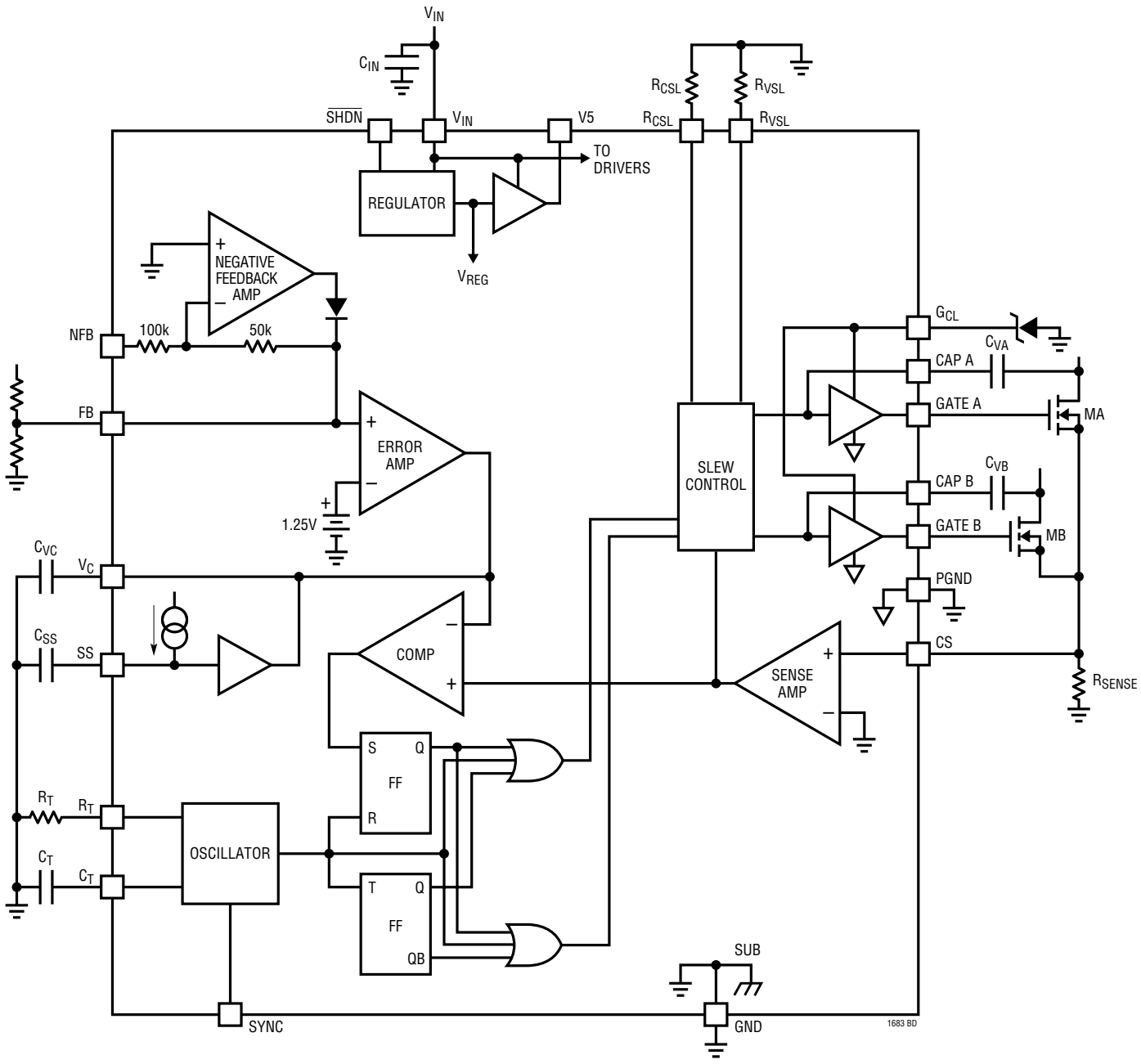


Figure 1b. Test Circuit for Slew

BLOCK DIAGRAM



OPERATION

In noise sensitive applications switching regulators tend to be ruled out as a power supply option due to their propensity for generating unwanted noise. When switching supplies are required due to efficiency or input/output constraints, great pains must be taken to work around the noise generated by a typical supply. These steps may include pre and post regulator filtering, precise synchronization of the power supply oscillator to an external clock, synchronizing the rest of the circuit to the power supply oscillator or halting power supply switching during noise sensitive operations. The LT1683 greatly simplifies the task of eliminating supply noise by enabling the design of an inherently low noise switching regulator power supply.

The LT1683 is a fixed frequency, current mode switching regulator with unique circuitry to control the voltage and current slew rates of the output switches. Current mode control provides excellent AC and DC line regulation and simplifies loop compensation.

Slew control capability provides much greater control over the power supply components that can create conducted and radiated electromagnetic interference. Compliance with EMI standards will be an easier task and will require fewer external filtering components.

The LT1683 uses two external N-channel MOSFETs as the power switches. This allows the user to tailor the drive conditions to a wide range of voltages and currents.

CURRENT MODE CONTROL

Referring to the block diagram. A switching cycle begins with an oscillator discharge pulse, which resets the RS flip-flop, turning on one of the external MOSFET drivers. The switch current is sensed across the external sense resistor and the resulting voltage is amplified and compared to the output of the error amplifier (V_C pin). The driver is turned off once the output of the current sense amplifier exceeds the voltage on the V_C pin. In this way pulse by pulse current limit is achieved. The toggle flip-flop ensures that the two MOSFETs are enabled on alternate clock cycles. Internal slope compensation is provided to ensure stability under high duty cycle conditions.

Output regulation is obtained using the error amp to set the switch current trip point. The error amp is a transconductance amplifier that integrates the difference between the feedback output voltage and an internal 1.25V reference. The output of the error amp adjusts the switch current trip point to provide the required load current at the desired regulated output voltage. This method of controlling current rather than voltage provides faster input transient response, cycle-by-cycle current limiting for better output switch protection and greater ease in compensating the feedback loop. The V_C pin is used for loop compensation and current limit adjustment. During normal operation the V_C voltage will be between 0.25V and 1.27V. An external clamp on V_C or SS may be used for lowering the current limit.

The negative voltage feedback amplifier allows for direct regulation of negative output voltages. The voltage on the NFB pin gets amplified by a gain of – 0.5 and driven on to the FB input, i.e., the NFB pin regulates to –2.5V while the amplifier output internally drives the FB pin to 1.25V as in normal operation. The negative feedback amplifier input impedance is 100k (typ) referred to ground.

Soft-Start

Control of the switch current during start up can be obtained by using the SS pin. An external capacitor from SS to ground is charged by an internal 9μA current source. The voltage on V_C cannot exceed the voltage on SS. Thus as the SS pin ramps up the V_C voltage will be allowed to ramp up. This will then provide for a smooth increase in switch maximum current. SS will be discharged as a result of the CS voltage exceeding the short circuit threshold of approximately 0.22V.

Slew Control

Control of output voltage and current slew rates is achieved via two feedback loops. One loop controls the MOSFET drain dV/dt and the other loop controls the MOSFET dI/dt.

The voltage slew rate uses an external capacitor between CAP A or CAP B and the respective MOSFET drain. These integrating caps close the voltage feedback loop. The external resistor R_{VSL} sets the current for the integrator.

OPERATION

The voltage slew rate is thus inversely proportional to both the value of capacitor and R_{VSL}.

The current slew feedback loop consists of the voltage across the external sense resistor, which is internally amplified and differentiated. The derivative is limited to a value set by R_{CSL}. The current slew rate is thus inversely proportional to both the value of sense resistor and R_{CSL}.

The two control loops are combined internally so that a smooth transition from current slew control to voltage slew control is obtained. When turning on, the driver current will slew before voltage. When turning off, voltage will slew before current. In general it is desirable to have R_{VSL} and R_{CSL} of similar value.

Internal Regulator

Most of the control circuitry operates from an internal 2.4V low dropout regulator that is powered from V_{IN}. The internal low dropout design allows V_{IN} to vary from 2.7V to 20V with stable operation of the controller. When $\overline{SHDN}$ < 1.3V the internal regulator is completely disabled.

5V Regulator

A 5V regulator is provided for powering external circuitry. This regulator draws current from V_{IN} and requires V_{IN} to be greater than 6.5V to be in regulation. It can sink or source 10mA. The output is current limited to prevent against destruction from accidental short circuits.

Safety and Protection Features

There are several safety and protection features on the chip. The first is overcurrent limit. Normally the gate drivers will go low when the output of the internal sense amplifier exceeds the voltage on the V_C pin. The V_C pin is clamped such that maximum output current is attained when the CS pin voltage is 0.1V. At that level the outputs will be immediately turned off (no slew). The effect of this control is that the output voltage will foldback with overcurrent.

In addition, if the CS voltage exceeds 0.22V, the V_C and SS pins will be discharged to ground also, resetting the soft-start function. Thus if a short is present this will allow for faster MOSFET turnoff and less MOSFET stress.

If the voltage on the FB pin exceeds regulation by approximately 0.22V, the outputs will immediately go low. The implication is that there is an overvoltage fault.

The voltage on GCL determines two features. The first is the maximum gate drive voltage. This will protect the MOSFET gate from overvoltage.

With GCL tied to a Zener or an external voltage source then the maximum gate driver voltage is approximately V_{GCL} – 0.2V. If GCL is tied to V_{IN}, then the maximum gate voltage is determined by V_{IN} and is approximately V_{IN} – 1.6V. There is an internal 19V Zener on the GCL pin that prevents the gate driver pin from exceeding approximately 19V.

In addition, the GCL voltage determines undervoltage lockout of the gate drives. This feature disables the gate drivers if V_{IN} is too low to provide adequate voltage to turn on the MOSFETs. This is helpful during start up to insure the MOSFETs have sufficient gate drive to saturate.

If GCL is tied to a voltage source or Zener less than 6.8V, the gate drivers will not turn on until V_{IN} exceeds GCL voltage by 0.8V. For V_{GCL} above 6.5V, the gate drives are insured to be off for V_{IN} < 7.3V and they will be turned on by V_{GCL} + 0.8V.

If GCL is tied to V_{IN}, the gate drivers are always enabled (undervoltage lockout is disabled).

When driving a push pull transformer, it is important to make sure that both drivers are not on at the same time. Even though runaway cannot occur under such cross conduction with this chip because current slew is regulated, increased current would be possible. This chip has opposite gate lockout whereby when one MOSFET is on the other MOSFET cannot be turned on until the gate of the first drops below 1V. This insures that cross conduction will not occur.

The gate drives have current limits for the drive currents. If the sink or source current is greater than 300mA then the current will be limited.

The V5 regulator also has internal current limiting that will only guarantee ±10mA output current.

OPERATION

There is also an on chip thermal shutdown circuit that will turn off the outputs in the event the chip temperature rises to dangerous levels. Thermal shutdown has hysteresis that will cause a low frequency (<1kHz) oscillation to occur as the chip heats up and cools down.

The chip has an undervoltage lockout feature that will force the gate drivers low in the event that V_{IN} drops below 2.5V. This insures predictable behavior during start up and shut down. $\overline{SHDN}$ can be used in conjuction with an external resistor divider to completely disable the part if the input voltage is too low. This can be used to insure adequate voltage to reliably run the converter. See the section in Applications Information.

Table 1 summarizes these features.

Table 1. Safety and Protection Features

FEATURE	FUNCTION	EFFECT on GATE DRIVERS	SLEW CONTROL	EFFECT on V_C, SS
Maximum Current Fault	Turn Off FETs at Maximum Switch Current (V_{SENSE} = 0.1)	Immediately Goes Low	Overridden	None
Short-Circuit Fault	Turn Off FETs and Reset V_C for Short-Circuit (V_{SENSE} = 0.2)	Immediately Goes Low	Overridden	Discharge V_C, SS to GND
Overvoltage Fault	Turn Off Drivers If FB > V_{REG} + 0.22V (Output Overvoltage)	Immediately Goes Low	Overridden	None
GCL Clamp	Set Max Gate Voltage to Prevent FET Gate Breakdown	Limits Max Voltage	None	None
Gate Drive Undervoltage Lockout	Disable Gate Drives When V_{IN} Is Too Low. Set Via GCL Pin	Immediately Goes Low	Overridden	None
Thermal Shutdown	Turn Off Drivers If Chip Temperature Is Too Hot	Immediately Goes Low	Overridden	None
Opposite Gate Lockout	Prevents Opposite Driver from Turning on Until Driver Is Off (Cross Conduction in Transformer)	Inhibits Turn On of Opposite Driver	None	None
V_{IN} Undervoltage Lockout	Disable Part When $V_{IN} \cong$ 2.55V	Immediately Goes Low	Overridden	None
Gate Drive Source and Sink Current Limit	Limit Gate Drive Current	Limit Drive Current	None	None
V5 Source/Sink Current Limit	Limit Current from V5	None	None	None
Shutdown	Disable Part When $\overline{SHDN}$ <1.3V			

APPLICATIONS INFORMATION

Reducing EMI from switching power supplies has traditionally invoked fear in designers. Many switchers are designed solely on efficiency and as such produce waveforms filled with high frequency harmonics that then propagate through the rest of the system.

The LT1683 provides control over two of the more important variables for controlling EMI with switching inductive loads: switch voltage slew rate and switch current slew rate. The use of this part will reduce noise and EMI over conventional switch mode controllers. Because these variables are under control, a supply built with this part will exhibit far less tendency to create EMI and less chance of encountering problems during production.

It is beyond the scope of this data sheet to get into EMI fundamentals. Application Note 70 contains much information concerning noise in switching regulators and should be consulted.

Oscillator Frequency

The oscillator determines the switching frequency and therefore the fundamental positioning of all harmonics. The use of good quality external components is important to ensure oscillator frequency stability. The oscillator is of a sawtooth design. A current defined by external resistor R_T is used to charge and discharge the capacitor C_T . The discharge rate is approximately ten times the charge rate.

By allowing the user to have control over both components, trimming of oscillator frequency can be more easily achieved.

The external capacitance C_T is chosen by:

$$C_T(nF) = \frac{2180}{f(kHz) \bullet R_T(k\Omega)}$$

where f is the desired oscillator frequency in kHz. For R_T equal to 16.9k, this simplifies to:

$$C_T(nF) = \frac{129}{f(kHz)}$$

e.g., C_T = 1.29nF for f = 100kHz

Nominally R_T should be 16.9k. Since it sets up current, its temperature coefficient should be selected to compliment the capacitor. Ideally, both should have low temperature coefficients.

Oscillator frequency is important for noise reduction in two ways. First the lower the oscillator frequency the lower the waveform's harmonics, making it easier to filter them. Second the oscillator will control the placement of the output voltage harmonics which can aid in specific problems where you might be trying to avoid a certain frequency bandwidth.

Oscillator Sync

If a more precise frequency is desired (e.g., to accurately place harmonics) the oscillator can be synchronized to an external clock. Set the RC timing components for an oscillator frequency 10% lower than the desired sync frequency.

Drive the SYNC pin with a square wave (with greater than 1.4V amplitude). The rising edge of the sync square wave will initiate clock discharge. The sync pulse should have a minimum pulse width of 0.5µs.

Be careful in sync'ing to frequencies much different from the part since the internal oscillator charge slope determines slope compensation. It would be possible to get into subharmonic oscillation if the sync doesn't allow for the charge cycle of the capacitor to initiate slope compensation. In general, this will not be a problem until the sync frequency is greater than 1.5 times the oscillator free-run frequency.

Slew Rate Setting

The primary reason to use this part is to gain advantage of lower EMI and noise due to slew control. The rolloff in higher frequency harmonics has its theoretical basis with two primary components. First, the clock frequency sets the fundamental positioning of harmonics and second, the associated normal frequency rolloff of harmonics.

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This part creates a second higher frequency rolloff of harmonics that inversely depends on the slew time, the time that voltage or current spends between the off state and on state. This time is adjustable through the choice of the slew resistors, the external resistors to ground on the R_{VSL} and R_{CSL} pins and the external components used for the external voltage feedback capacitors C_{AV}, C_{BV} (from CAP A or CAP B to their respective MOSFET drains) and the sense resistor. Lower slew rates (longer slew times, lower frequency for harmonics rolloff) is created with higher values of R_{VSL}, R_{CSL}, C_{AV}, C_{BV} and the current sense resistor

Setting the voltage and current slew rates should be done empirically. The most practical way of determining these components is to set C_{AV}, C_{BV} and the sense resistor value. Then, start by making R_{VSL}, R_{CSL} each a 50k resistor pot in series with 3.3k. Starting from the lowest resistor setting (fast slew) adjust the pots until the noise level meets your guidelines. Note that slower slewing waveforms will dissipate more power so that efficiency will drop. You can monitor this as you make your slew adjustment by measuring input and output voltage and their respective currents. Monitor the MOSFET temperature as slew rates are slowed. These components will heat up as efficiency decreases.

Measuring noise should be done carefully. It is easy to introduce noise by poor measurement techniques. Consult AN70 for recommended measurement techniques. Keeping probe ground leads very short is essential.

Usually it will be desirable to keep the voltage and current slew resistors approximately the same. There are circumstances where a better optimization can be found by adjusting each separately, but as these values are separated further, a loss of independence of control may occur.

It is possible to use a single slew setting resistor. In this case the R_{VSL} and R_{CSL} pins are tied together. A resistor with a value of 1.8k to 34k (one half the individual resistors) can then be tied from these pins to ground.

In general only the R_{CSL} value will be available for adjustment of current slew. The current slew time does also depend on the current sense resistor but this resistor is normally set with consideration of the maximum current in the MOSFETs.

Setting the voltage slew also involves selection of the capacitors C_{AV}, C_{BV}. The voltage slew time is proportional to the output voltage swing (basically input voltage), the external voltage feedback capacitor and the R_{VSL} value. Thus at higher input voltages smaller capacitors will be used with lower R_{VSL} values. For a starting point use Table 2.

Table 2

INPUT VOLTAGE	CAPACITOR VALUE
< 25V	5pF
50V	2.5pF
100V	1pF

Smaller value capacitors can be made in two ways. The first is simply combining two capacitors in series. The equivalent capacitance is then (C1 • C2)/(C1 + C2).

The second method makes use of a capacitor divider. Care should be taken that the voltage ratings of the capacitors satisfy the full voltage swing (2x input voltage for push-pull configurations) thus essentially the same rating as the MOSFETs.

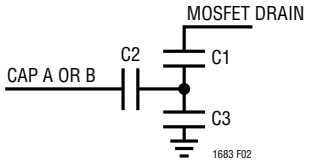

Figure 2

The equivalent slew capacitance for Figure 2 is (C1 • C2)/(C1 + C2 + C3).

Positive Output Voltage Setting

Sensing of a positive output voltage is usually done using a resistor divider from the output to the FB pin. The positive input to the error amp is connected internally to a 1.25V bandgap reference. The FB pin will regulate to this voltage.

Referring to Figure 3, R1 is determined by:

$$R1 = R2\left(\frac{V_{OUT}}{1.25} - 1\right)$$

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The FB bias current represents a small error and can usually be ignored for values of R1||R2 up to 10k.

One word of caution, sometimes a feedback zero is added to the control loop by placing a capacitor across R1. If the feedback capacitively pulls the FB pin above the internal regulator voltage (2.4V), output regulation may be disrupted. A series resistance with the feedback pin can eliminate this potential problem. There is an internal clamp on FB that clamps at 0.7V above the regulation voltage that should also help prevent this problem.

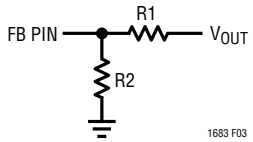


Figure 3

Negative Output Voltage Setting

Negative output voltage can be sensed using the NFB pin. In this case regulation will occur when the NFB pin is at –2.5V. The nominal input bias current for the NFB is –25µA (I_{NFB}), which needs to be accounted for in setting up the divider.

Referring to Figure 4, R1 is chosen such that:

$$R1 = R2\left(\frac{\left|V_{OUT}\right| - 2.5}{2.5 + R2 \bullet 25\mu A}\right)$$

A suggested value for R2 is 2.5k. The NFB pin is normally left open if the FB pin is being used.

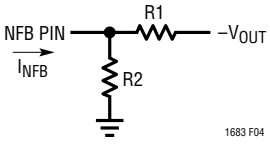


Figure 4

Dual Polarity Output Voltage Sensing

Certain applications may benefit from sensing both positive and negative output voltages. When doing this each output voltage resistor divider is individually set as previously described. When both FB and NFB pins are used, the LT1683 will act to prevent either output from going beyond its set output voltage. The highest output (lightest load) will dominate control of the regulator. This technique would prevent either output from going unregulated high at no load. However, this technique will also compromise output load regulation.

Shutdown

If $\overline{SHDN}$ is pulled low, the regulator will turn off. As the $\overline{SHDN}$ pin voltage is increased from ground the internal bandgap regulator will be powered on. This will set a 1.39V threshold for turn on of the internal regulator that runs most of the control circuitry of the regulator. Note after the control circuitry powers on, gate driver activity will depend on the voltage of V_{IN} with respect to the voltage on GCL.

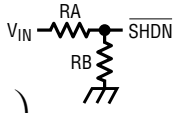
As the $\overline{SHDN}$ pin enables the internal regulator a 24µA current will be sourced from the pin that can provide hysteresis for undervoltage lockout. This hysteresis can be used to prevent part shutdown due to input voltage sag from an initial high current draw.

In addition to the current hysteresis, there is also approximately 100mV of voltage hysteresis on the $\overline{SHDN}$ pin.

When the $\overline{SHDN}$ pin is greater than 2.2V, the hysteretic current from the part will be reduced to essentially zero.

If a resistor divider is used to set the turn on threshold then the resistors are determined by the following equations.

$$V_{ON} = \left(\frac{RA + RB}{RB}\right) \bullet V_{SHDN}$$



$$V_{HYST} = RA \bullet \left(\frac{\Delta V_{SHDN}}{RA \| RB} + I_{SHDN}\right)$$

Reworking these equations yields:

$$RA = \frac{(V_{HYST} \bullet V_{SHDN} - V_{ON} \bullet \Delta V_{SHDN})}{(I_{SHDN} \bullet V_{SHDN})}$$

$$RB = \frac{(V_{HYST} \bullet V_{SHDN} - V_{ON} \bullet \Delta V_{SHDN})}{\left[I_{SHDN} \bullet (V_{ON} - V_{SHDN})\right]}$$

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So if we wanted to turn on at 20V with 2V of hysteresis:

$$RA = \frac{2V \bullet 1.39V - 20V \bullet 0.1V}{24\mu A \bullet 1.39V} = 23.4k$$

$$RB = \frac{2V \bullet 1.39V - 20V \bullet 0.1V}{24\mu A \bullet (20V - 1.39V)} = 1.75k$$

Resistor values could be altered further by adding Zeners in the divider string. A resistor in series with $\overline{SHDN}$ pin could further change hysteresis without changing turn on voltage.

Frequency Compensation

Loop frequency compensation is accomplished by way of a series RC network on the output of the error amplifier (V_C pin).

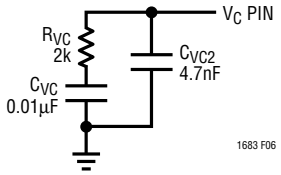

Figure 6

Referring to Figure 6, the main pole is formed by capacitor C_{VC} and the output impedance of the error amplifier (approximately 400kΩ). The series resistor R_{VC} creates a "zero" which improves loop stability and transient response. A second capacitor C_{VC2}, typically one-tenth the size of the main compensation capacitor, is sometimes used to reduce the switching frequency ripple on the V_C pin. V_C pin ripple is caused by output voltage ripple attenuated by the output divider and multiplied by the error amplifier. Without the second capacitor, V_C pin ripple is:

$$V_{CPINRIPPLE} = \frac{1.25 \bullet V_{RIPPLE} \bullet gm \bullet R_{VC}}{V_{OUT}}$$

where V_{RIPPLE} = Output ripple (V_{P-P})

gm = Error amplifier transconductance

R_{VC} = Series resistor on V_C pin

V_{OUT} = DC output voltage

To prevent irregular switching, V_C pin ripple should be kept below $50mV_{P-P}$. Worst-case V_C pin ripple occurs at maximum output load current and will also be increased if poor quality (high ESR) output capacitors are used. The addition of a 0.0047µF capacitor for C_{VC2} pin reduces switching frequency ripple to only a few millivolts. A low value for R_{VC} will also reduce V_C pin ripple, but loop phase margin may be inadequate.

Setting Current Limit

The sense resistor sets the value for maximum operating current. When the CS pin voltage is 0.1V the gate drivers will immediately go low (no slew control). Therefore the sense resistor value should be set to $R_S = 0.1V/I_{SW(PEAK)}$, where $I_{SW(PEAK)}$ is the peak current in the MOSFETs. $I_{SW(PEAK)}$ will depend on the topology and component values and tolerances. Certainly it should be set below the saturation current value for the transformer.

If CS pin voltage is 0.22V in addition to the drivers going low, V_C and SS will be discharged to ground. This is to provide additional protection in the event of a short circuit. By discharging V_C and SS the MOSFET will not be stressed as hard on subsequent cycles since the current trip will be set lower.

Turn off of the MOSFETs will normally be inhibited for about 100ns at the start of every turn on cycle. This is to prevent noise from interfering with normal operation of the controller. This current sense blanking does not prevent the outputs from be turned off in the event of a fault. Slewing of the gate voltage effectively provides additional blanking.

Traces to the SENSE resistor should be kept short and wide to minimize resistance and inductance.

Soft-Start

The soft-start pin is used to provide control of switching current during startup. The max voltage on the V_C pin is approximately the voltage on the SS pin. A current source will linearly charge a capacitor on the SS pin. The V_C pin voltage will thus ramp also. The approximate time for the voltage on these pins to ramp is (1.31V/9µA) • C_{SS} or approximately 146ms per µF.

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The soft-start current will be initiated as soon as the part turns on. Soft-start will be reinititated after a short-circuit fault.

Thermal Considerations

Most of the IC power dissipation is derived from the V_{IN} pin. The V_{IN} current depends on a number of factors including: oscillator frequency; loads on V5; slew settings; gate charge current. Additional power is dissipated if V5 sinks current and during the MOSFET gate discharge.

The power dissipation in the IC will be the sum of:

1) The RMS V_{IN} current times V_{IN}

2) V5 RMS sink current times 5V

3) The gate drive's RMS discharge current times voltage

Because of the strong V_{IN} component it is advantageous to operate the LT1683 at as low a V_{IN} as possible.

It is always recommended that package temperature be measured in each application. The part has an internal thermal shutdown to minimize the chance of IC destruction but this should not replace careful thermal design.

The thermal shutdown feature does not protect the external MOSFETs. A separate analysis must be done for those devices to insure that they are operating within safe limits.

Once IC power dissipation, P_{DIS}, is determined die junction temperature is then computed as:

$$T_J = T_{AMB} + P_{DIS} \bullet \theta_{JA}$$

where T_{AMB} is ambient temperature and θ_{JA} is the package thermal resistance. For the 20-pin SSOP, θ_{JA} is 100°C/W.

Magnetics

Design of magnetics is dependent on topology. The following details the design of the magnetics for a push-pull converter. In this converter the transformer usually stores little energy. The following equations should be considered as the starting point to building a prototype.

The following definitions will be used:

V_{IN} = Input supply voltage

R_{ON} = Switch-on resistance

I_{SW} = Maximum switch current

V_{OUT} = Desired output voltage

I_{OUT} = Output current

f = Oscillator frequency

V_F = Forward drop of the rectifier

Duty cycle is the major defining equation for this topology. Note that the output L and C basically filter the chopped voltage so duty cycle controls output voltage. N is the turns ratio of the transformer. The turns ratio must be large enough to ensure that the transformer can put out a voltage equal to the output voltage plus the diode under minimum input conditions. Note the transformer operates at half the oscillator frequency (f).

$$N = \frac{V_{OUT} + V_F}{\left(2 \bullet DC_{MAX}\right)\left[V_{IN(MIN)} - I_{SW}\left(R_{ON} + R_{SENSE}\right)\right]}$$

DC_{MAX} is the maximum duty cycle of each driver with respect to the entire cycle, which consists of two periods (A on and B on). So the effective duty cycle is $2 \bullet DC_{MAX}$. The controller, in general, determines maximum duty cycle. A 44% maximum duty cycle is a guaranteed value for this part.

Remember to add sufficient margin in the turns ratio to account for IR drops in the transformer windings, worst-case diode forward drops and switch on voltage. Also at very slow slew rates the effective DC may be reduced.

There are a number of ways to choose the inductance value for L. We suggest as a starting point that L be selected such that the converter is continuous at $I_{OUT(MAX)}/4$. If your minimum I_{OUT} is higher than this or your components can handle higher peak currents then use a higher number.

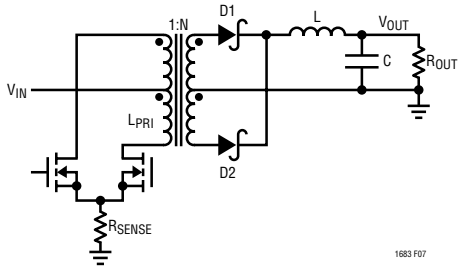

Figure 7. Push-Pull Topology

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Continuous operation occurs when the current in the inductor never goes to zero. Discontinuous operation occurs when the inductor current drops to zero before the start of the next cycle and can occur with small inductors and light loads. There is nothing inherently bad about discontinuous operation, however, converter control and operation are somewhat different. The inductor is smaller for discontinuous operation but the peak currents in the switch, the transformer, the diodes, inductor and capacitor will be higher which may produce greater losses.

For continuous operation the inductor ripple current must be less than twice the output current. The worst case for this is at maximum input (lowest duty cycle, DC_{MIN}) but in the following we will evaluate at nominal input since the $I_{OUT}/4$ is somewhat arbitrary.

Note when both inputs are off, the inductor current splits between both secondary outputs and the diode common goes to 0V.

Looking at the inductor current during off time, output ripple current is:

$$\Delta I_{OUT} = 2 \bullet I_{OUT(MIN)}$$

$$I_{OUT(MIN)} = I_{OUT(MAX)} / 4$$

$$L = \frac{\left(V_{OUT(MIN)} + V_F\right) \bullet \left(1 - 2 \bullet DC\right)}{\Delta I_{OUT} \bullet f}$$

The inductance of the transformer primary should be such that L, when reflected into the primary, dominates the input current. In other words, we want the magnetizing current of the transformer small with respect to the current going through the transformer to L. In general, then, the inductance of the primary should be at least five times that of L reflected to the input. This ensures that most of the power will be passed through the transformer to the load. It also increases the power capability of the converter and reduces the peak currents that the switch will see.

$$L_{PRI} = \frac{5 \bullet L}{N^2}$$

If the magnetizing current is small, say below 100mA, then a smaller L can be used with a higher percentage of the switch current generated by the magnetizing current.

With the value of L set, the ripple in the inductor is:

$$\Delta I_L = \frac{\left(V_{OUT} + V_F\right) \bullet \left(1 - 2 \bullet DC\right)}{L \bullet f}$$

However, the peak inductor current is evaluated at maximum load and maximum input voltage (minimum DC).

$$I_{L(MAX)} = I_{L(MAX)} + \frac{\Delta I_{L(MAX)}}{2}$$

The magnetizing ripple current can be shown to be:

$$\Delta I_{MAG} = \frac{V_{OUT} + V_F}{N \bullet L_{PRI} \bullet f}$$

and the peak current in the switch is:

$$I_{SW(PEAK)} = N \bullet I_{L(MAX)} + \Delta I_{MAG}$$

This current should be less than the current limit.

Worst-case switch ripple is:

$$\Delta I_{SW(PEAK)} = N \bullet \Delta I_{L(MAX)} + \Delta I_{MAG}$$

In the push-pull converter the maximum switch voltage will be $2 \bullet V_{IN}$. Because voltage is slew-controlled, the leakage spikes are small. So, the MOSFET should have a maximum rated switch voltage at least 20% higher than $2 \bullet V_{IN}$.

So, given the turns ratio, primary inductance and current, the transformer can be designed. The design of the transformer will require analyzing the power losses of the transformer and making necessary adjustments.

Most transformer companies can assist you with designing an optimal solution. For instance Midcom, Inc. (1-800-643-2661). Linear Technology's application group can also help.

As an example say we are designing a 48V ±20% to 5V 100kHz converter with 2A output and 500mA ripple. Then starting with a guess for the on voltage of the MOSFET plus sense resistor of 0.5V and V_F of 0.5V:

$$N = \frac{5 + 0.5}{88\% \bullet \left(48 \bullet 80\% - 0.5\right)} = \frac{1}{6.1}$$

APPLICATIONS INFORMATION

For continuous operation at $I_{OUT(MIN)} = I_{OUT(MAX)}/4$, inductor ripple (the same as output ripple):

$$\Delta I_L = 2 \bullet \frac{2A}{4} = 1A$$

The duty cycle for nominal input is:

$$DC_{NOM} = \frac{V_{OUT} + V_F}{2 \bullet N\left(V_{IN(NOM)} - I_{SW} \bullet R_{ON}\right)}$$

$$= \frac{5.5}{\frac{2}{6.1} \bullet 47.5} = 35.3\%$$

Then

$$L = \frac{\left(5 + 0.5\right) \bullet \left(1 - 2 \bullet 35.3\%\right)}{1A \bullet 100kHz} = 16\mu H$$

Off-the-shelf components can be used for this inductor. Say we choose a 22µH inductor then ripple current at maximum input (DC = 29.1%) is:

$$\Delta I_L = \frac{\left(5 + 0.5\right) \bullet \left(1 - 2 \bullet 29.1\%\right)}{22\mu F \bullet 100kHz} = 1.03A$$

The maximum inductor current is:

$$I_{L(MAX)} = 2A + \frac{1.03A}{2} = 2.52A$$

Primary inductance should be greater than:

$L_{PRI} = 5 \bullet 22\mu H \bullet 6.1^2 = 4.1mH$

The secondary inductance would then be:

$4.1mH/6.1^2 = 110\mu H$

The magnetizing ripple current is approximately:

$$\Delta I_{MAG} = \frac{5.5}{\frac{1}{6.1} \bullet 4.1mH \bullet 100kHz} = 81mA$$

Peak switch current is:

$$I_{SW(PEAK)} = \frac{1}{6.1} \bullet 2.51A + 81mA = 494mA$$

Note that you can discern your magnetizing ripple by looking at the reflected inductance ripple and subtracting it from the switch current ripple.

$\Delta I_{MAG} = N \bullet I_L - \Delta I_{SW}$

The max ripple current on the switch is:

$$\Delta I_{SW(MAX)} = \frac{1.03A}{6.1} + 81mA = 0.25A$$

Knowing the peak switch current we can go back and iterate with a more accurate switch on voltage. We would have to know the R_{ON} of the FET. In our case our assumptions of a 0.5V switch on voltage is valid for $R_{ON} + R_{SENSE} < 1\Omega$.

Capacitors

Correct choice of input and output capacitors is very important to low noise switcher performance. Push-pull topologies and other low noise topologies will in general have continuous currents, which reduce the requirements for capacitance. However, noise depends more on the ESR of the capacitors. In addition lower ESR can also improve efficiency.

Input capacitors must also withstand surges that occur during the switching of some types of loads. Some solid tantalum capacitors can fail under these surge conditions.

Design Note 95 offers more information but the following is a brief summary of capacitor types and attributes.

Aluminum Electrolytic: Low cost and higher voltage. They can be used in this application but in general you will need higher capacitance to achieve low ESR. Additional nonelectrolytic capacitors may be required to achieve better performance.

Specialty Polymer Aluminum: Panasonic has come out with their series CD capacitors. While they are only available for voltages below 16V, they have very low ESR and good surge capability.

APPLICATIONS INFORMATION

Solid Tantalum: Small size and low impedance. Typically the maximum voltage rating is 50V. With large surge currents the capacitor may need to be derated or you need a special type such as AVX TPS line.

OS-CON: Lower impedance than aluminum but only available for 35V or less. Form factor may be a problem.

Ceramic: Generally used for high frequency and high voltage bypass. They may resonate with their ESL before ESR becomes dominant. Recent multilayer ceramic (MLC) capacitors provide larger capacitance with low ESR.

There are continuous improvements being made in capacitors so consult with manufacturers as to your specific needs.

Input Capacitors

The input capacitor should have low ESR at high frequencies since this will be an important factor concerning how much conducted noise is created.

There are two separate requirements for input capacitors. The first is for supply to the part's V_{IN} pin. The V_{IN} pin will provide current for the part itself and the gate charge current.

The worst component from an AC point is the gate charge current. The actual peak current depends on gate capacitance and slew rate, being higher for larger values of each. The total current can be estimated by gate charge and frequency of operation. Because of the slewing with this part gate charge is spread out over a longer time period than with a normal FET driver. This reduces capacitance requirements.

Typically the current will have spikes of under 100mA located at the gate voltage transitions. This is charge/discharge to and from the threshold voltage. Most slewing occurs with the gate voltage near threshold.

Since the part's V_{IN} will typically be under 15V many options are available for choice of capacitor. Values of input capacitor for just V_{IN} requirement will typically be in the 50µF range with an ESR of under 0.1Ω.

In addition to the part supply, decoupling of the supply to the transformer needs to be considered. If this is the same supply as the V_{IN} pin then that capacitor will need to be increased. However, often with this part the transformer supply will be a higher voltage and as such a separate capacitor.

The transformer decoupling capacitor will see the switch current as ripple.

The above switch current computation can be used to estimate the capacity for these capacitors.

$$C_{IN} = \frac{1}{\frac{\Delta V_{CAP}}{\Delta I_{SW(MAX)}} - ESR} \bullet \frac{DC_{MIN}}{f}$$

where ΔV_{CAP} is the allowed sag on the input capacitor. ESR is the equivalent series resistance for the cap. In general allowed sag will be a few tenths of volts.

Output Filter Capacitor

The output capacitor is chosen both for capacity and ESR. The capacity must supply the load current in the switch off state. While slew control reduces higher frequency components of the ripple current in the capacitor, the capacitor ESR and the magnitude of the output ripple current controls the fundamental component. ESR should also be low to reduce capacitor dissipation.

The capacitance value can be computed by consideration of desired load ripple, duty cycle and ESR.

$$C_{OUT} = \frac{1}{\frac{\Delta V_{OUT}}{\Delta I_{L(MAX)}} - ESR} \bullet \frac{DC_{MIN}}{f}$$

APPLICATIONS INFORMATION

MOSFET Selection

There is a wide variety of MOSFETs to choose from for this part. The part will work with either normal threshold (3V to 4V) or logic level threshold devices (1V to 2V).

Select a voltage rating to insure under worst-case conditions that the MOSFET will not break down. Next choose an R_{ON} sufficiently low to meet both the power dissipation capabilities of the MOSFET package as well as overall efficiency needs of the converter.

The LT1683 can handle a large range of gate charges. However at very large charge stability may be affected.

The power dissipation in the MOSFET depends on several factors. The primary element is I^2R heating when the device is on. In addition, power is dissipated when the device is slewing. An estimate for power dissipation is:

$$P = \left\{ V_{IN} \bullet \frac{I^2 + \frac{\Delta I^2}{4}}{I_{SR}} + \frac{\left[V_{IN}^{\,2} - R_{ON}^{\,2} \bullet \left(I^2 + \frac{3 \bullet \Delta I^2}{4} \right) \right]}{V_{SR}} \right\} \bullet f + I^2 \bullet R_{ON} \bullet DC$$

where I is the average current, ΔI is the ripple current in the switch, I_{SR} is the current slew rate, V_{SR} is the voltage slew rate, f is the oscillator frequency, DC is the duty cycle and R_{ON} is the MOSFET on-resistance.

Setting GCL Voltage

Setting the voltage on the GCL pin depends on what type of MOSFET is used and the desired gate drive undervoltage lockout voltage.

First determine the maximum gate drive that you require. Typically you will want it to be at least 2V greater than the maximum threshold. Higher voltages will lower the on resistance and increase efficiency. Be certain to check the maximum allowed gate voltage. Often this is 20V but for some logic threshold MOSFETs it is only 8V to 10V.

V_{GCL} needs to be set approximately 0.2V above the desired max gate threshold. In addition V_{IN} needs to be at least 1.6V above the gate voltage.

The GCL pin can be tied to V_{IN} which will result in a maximum gate voltage of $V_{IN} – 1.6V$.

This pin also controls undervoltage lockout of the gate drives. The undervoltage lockout will prevent the MOSFETs from switching until there is sufficient drive present.

If GCL is tied to a voltage source or Zener less than 6.8V, the gate drivers will not turn on until V_{IN} exceeds the GCL voltage by 0.8V. For V_{GCL} above 6.5V, the gate drives are insured to be off for $V_{IN} < 7.3V$ and they will be turned on by $V_{GCL} + 0.8V$.

If GCL is tied to V_{IN}, the gate drivers are always on (undervoltage lockout is disabled).

Approximately 50µA of current can be sourced from this pin if $V_{IN} > V_{GCL} + 0.8V$. This could be used to bias a Zener.

The GCL pin has an internal 19V Zener to ground that will provide a failsafe for maximum gate voltage.

As an example say we are using a Siliconix Si4480DY which has $R_{DS(ON)}$ rated at 6V. To get 6V, V_{GCL} needs to be set to 6.2V and V_{IN} needs to be at least 7.6V.

APPLICATIONS INFORMATION

Gate Driver Considerations

In general, the MOSFETs should be positioned as close to the part as possible to minimize inductance.

When the part is active the gate drives will be pulled low to less than 0.2V. When the part is off, the gate drives contain a 40k resistor in series with a diode to ground that will offer passive holdoff protection. If you are using some logic level MOSFETs this might not be sufficient. A resistor may be placed from gate to ground, however the value should be reasonably high to minimize DC losses and possible AC issues.

The gate drive source current comes from V_{IN}. The sink current exits through PGND. In general the decoupling cap should be placed close to these two pins.

Switching Diodes

In general, switching diodes should be Schottky diodes. Size and breakdown voltage depend on the specific converter. A lower forward drop will improve converter efficiency. No other special requirements are needed.

PCB Layout Considerations

As with any switcher careful consideration should be given to PC board layout. Because this part reduces high frequency EMI the board layout is less critical, however high currents and voltages still produce the need for careful board layout to eliminate poor and erratic performance.

Basic Considerations

Keep the high current loops physically small in area. The main loops are shown in Figure 8: the power switch loops (A and B) and the rectifier loop (C and D). These loops can be kept small by physically keeping the components close to one another. In addition, connection traces should be kept wide to lower resistance and inductances. Components should be placed to minimize connecting paths. Careful attention to ground connections must also be maintained. Without getting into elaborate detail be careful that currents from different high current loops do not get coupled into the ground paths of other loops. Using singular points of connection for the grounds is the best way to do this. The two major points of connection are the bottom of the input decoupling cap and the bottom of the output decoupling cap. Typically the sense resistor device PGND and device GND will tie to the bottom of the input cap.

There are two other loops to pay attention to. The current slew involves a high bandwidth control that goes through the MOSFET switch, the sense resistor and into the CS pin of the part and out the GATE pin to the MOSFET. Trace inductance and resistance should be kept low on the GATE drive trace. The CS trace should have low inductance. The sense resistor should be physically close to PGND and the MOSFETs' sources.

Finally care should be taken with the CAP A, CAP B pins. The part will tolerate stray capacitance to ground on these pins (<5pF) however stray capacitance to the respective drains should be minimized. This path would provide an alternate capacitive path for the voltage slew.

More Help

AN70 contains information about low noise switchers and measurement of noise and should be consulted. AN19 and AN29 also have general knowledge concerning switching regulators. Also, our Application Department is always ready to lend a helping hand.

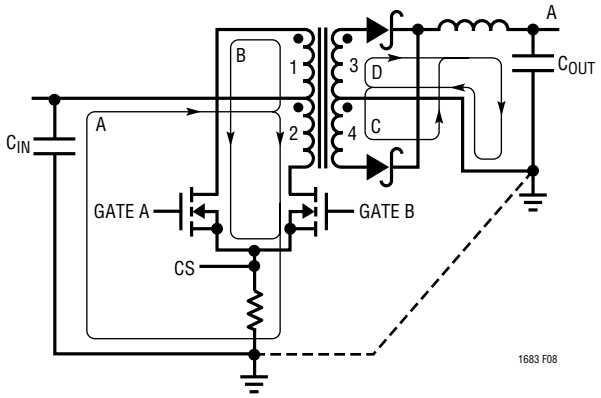
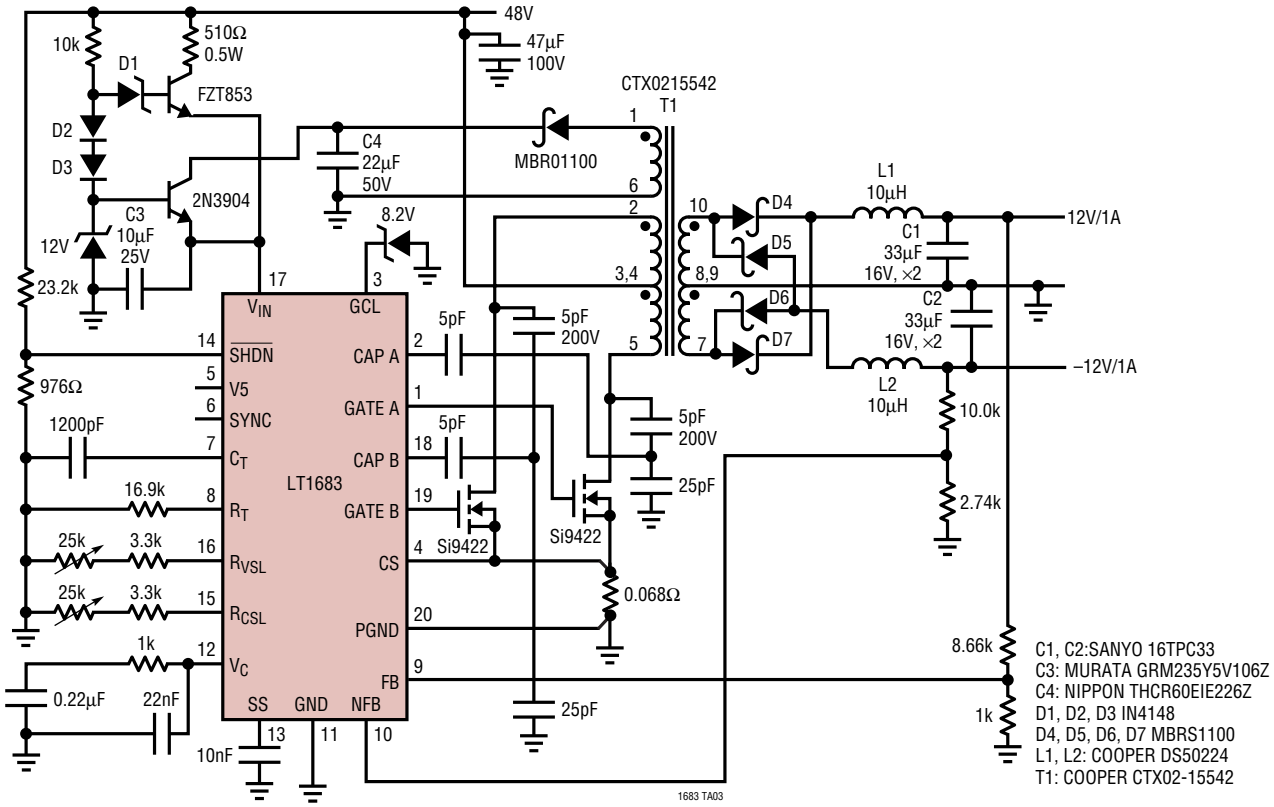


Figure 8

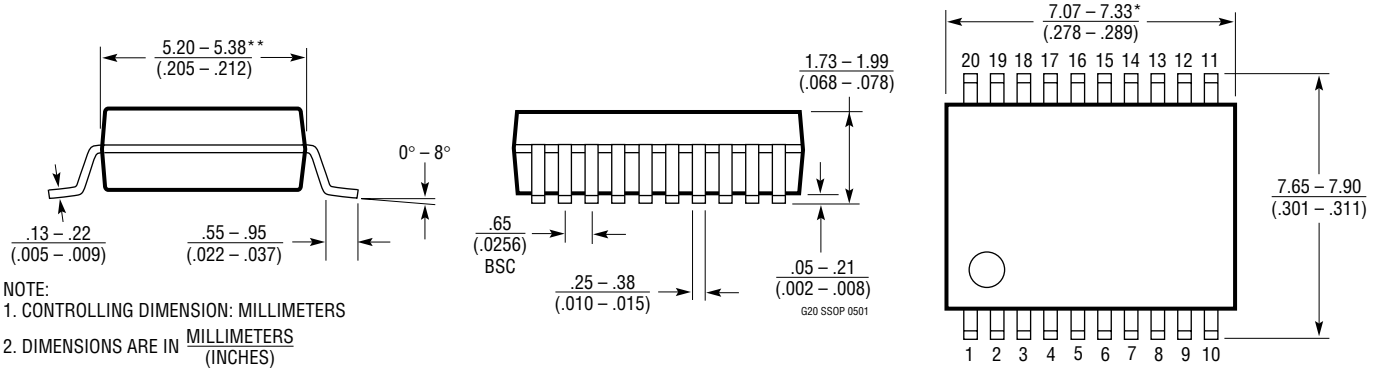
TYPICAL APPLICATION

Ultralow Noise 48V to ±12V DC/DC Converter



PACKAGE DESCRIPTION

G Package
20-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)



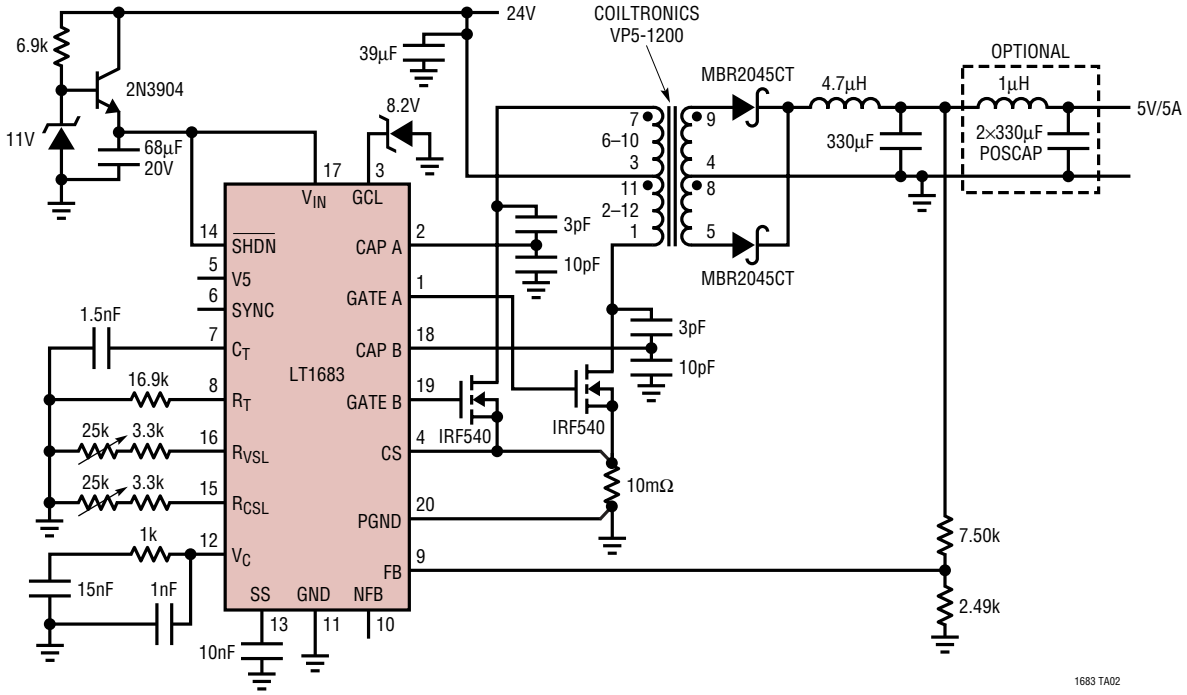
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

TYPICAL APPLICATION

Ultralow Noise 24V to 5V DC/DC Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1533	Ultralow Noise 1A Switching Regulator	Push-Pull Design for Low Noise Isolated Supplies
LT1534	Ultralow Noise 2A Switching Regulator	Ultralow Noise Regulator for Boost Topologies
LT1738	Ultralow Noise DC/DC Controller	High Current Output Ultralow Noise Boost Regulator; Drives External MOSFET
LT1777	Low Noise Step-Down Switching Regulator	Programmable dI/dt; Internally Limited dV/dt
LT1425	Isolated Flyback Switching Regulator	Excellent Regulation without Transformer “Third Winding”
LT1576	1.5A, 200kHz Step-Down Switching Regulator	Constant Frequency, 1.21V Reference Voltage
LT176X Family	Low Dropout, Low Noise Linear Regulator	150mA to 3A, SOT-23 to TO-220
LTC1922-1	Synchronous Phase Modulated Full-Bridge Controller	Adaptive DirectSense™ Zero Voltage Switching, 50W to Kilowatts, Synchronous Rectification

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