M65824AFP

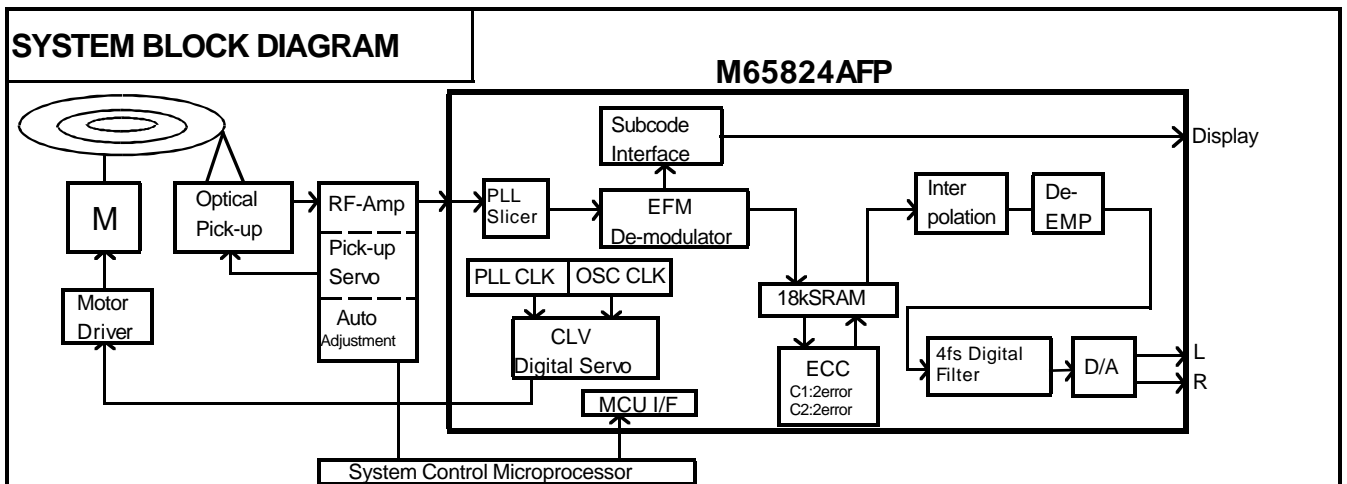## CD PLAYER DIGITAL SIGNAL PROCESSOR WITH BUILT-IN DAC

DESCRIPTION

The M65824AFP is a CMOS IC developed for compact disc players.
(suitable for CD-DA:Compact Disc-Digital Audio)
It has built-in memory,adjustment-free PLL and D/A converter with DSP function.

FEATURES

♦ Adjustment free EFM-PLL circuit(Includes VCO)
♦ ±8 frames jitter margin
♦ Digital CLV servo control
♦ Attenuation(-12dB)
♦ 4 times over sampling IIR type digital filter
♦ Digital de-emphasis function
♦ D/A converter
♦ A smaller package
♦ Analog LPF
♦ Digital audio interface
♦ External D/A mode

RECOMMENDED OPERATING CONDITIONS

Supply voltage range(interface)··DVDD=2.7 to 5.5V
Supply voltage range(internal logic system and analog)····················DSPS,AVDD=2.7 to 3.3V
Rated supply voltage(interface)···DVDD=5.0V
Rated supply voltage(internal logic system and analog)·······························DSPS,AVDD=3.0V
Rated power dissipation···100mW

SYSTEM BLOCK DIAGRAM

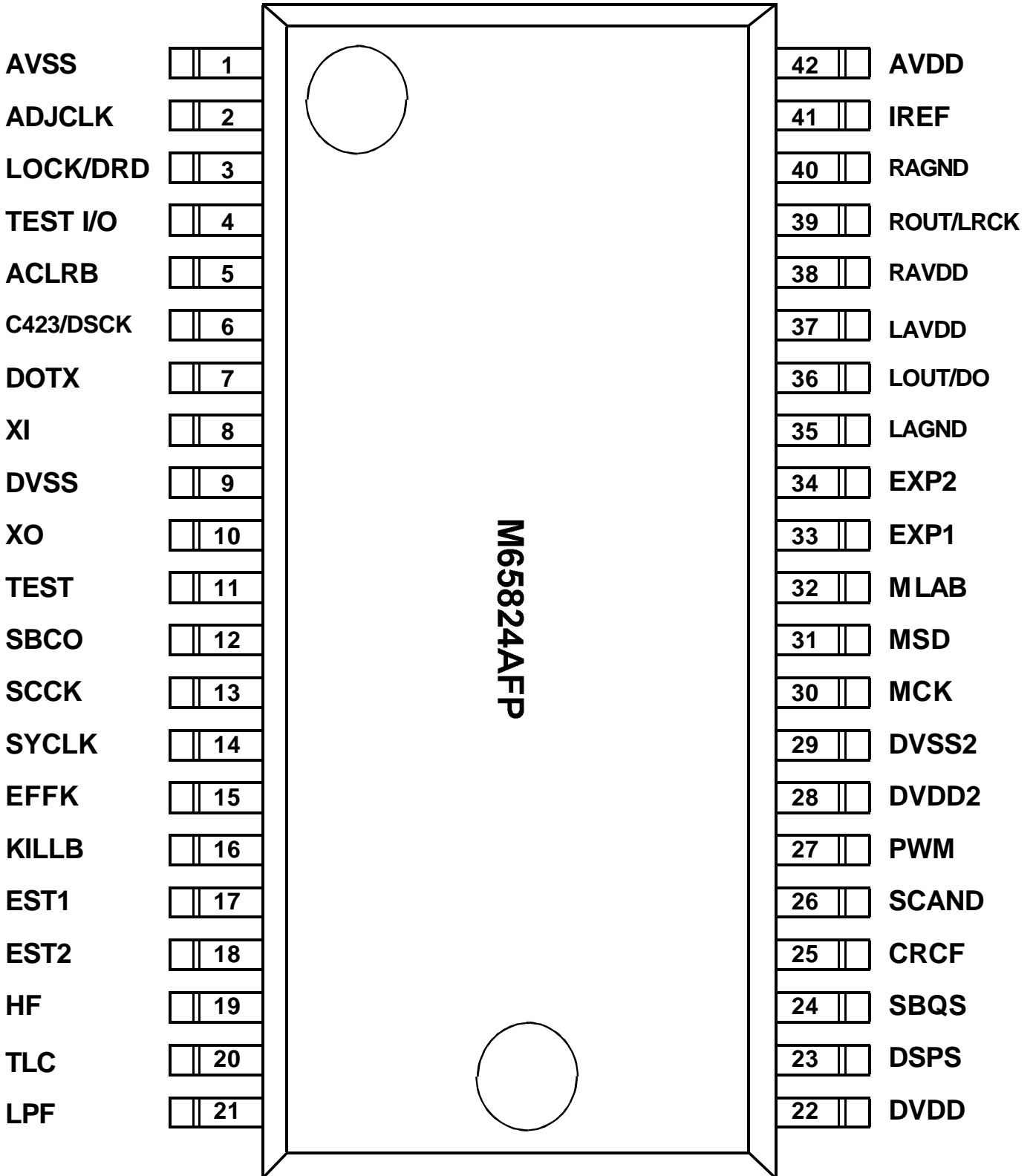## CD PLAYER DIGITAL SIGNAL PROCESSOR WITH BUILT-IN DAC

1.BUILT-IN FUNCTIONS

Functional block	Description:
D/A converter	• 64fs 1bit $\Sigma\Delta$ D/A converter • S/N:74dB(theoretically)
Memory	• 18kSRAM(built-in) • ±8 fames jitter margin
PLL	• Adjustment free VCO • Slice level control
EFM demodulator	• EFM demodulation • Frame sync.detection,protection&interpolation • Frame sync.signal output
Subcode decoding	• Subcode P to W decoding,serial output • Subcode Q register • Subcode Q-CRC Check • Subcode sync.signal output(S0/S1) • Emphasis detection,built-in de-emphasis circuit control
CRC decoding	• C1:Duplex,C2:Duplex • De-scramble • De-interleave • Error monitor output
Data interpolator	• Averaging/Holding
D/A interface	• Muting control
Digital filter	• 4 times over sampling digital filter
De-emphasis	• Digital de-emphasis (IIR type digital filter) • Automatic emphasis flag detection
CLV digital servo	• PWM output • Low disc rotation detection
Microcomputer interface	• CLV digital servo control • Muting control • Attenuation(-12dB) • Subcode Q register interface
Digital audio interface	• Digital audio interface output ON/OFF • Clock accuracy input
HFD	• TLC voltage "hold" • LPF output "open" • PWM output "regular acceleration"

M65824AFP

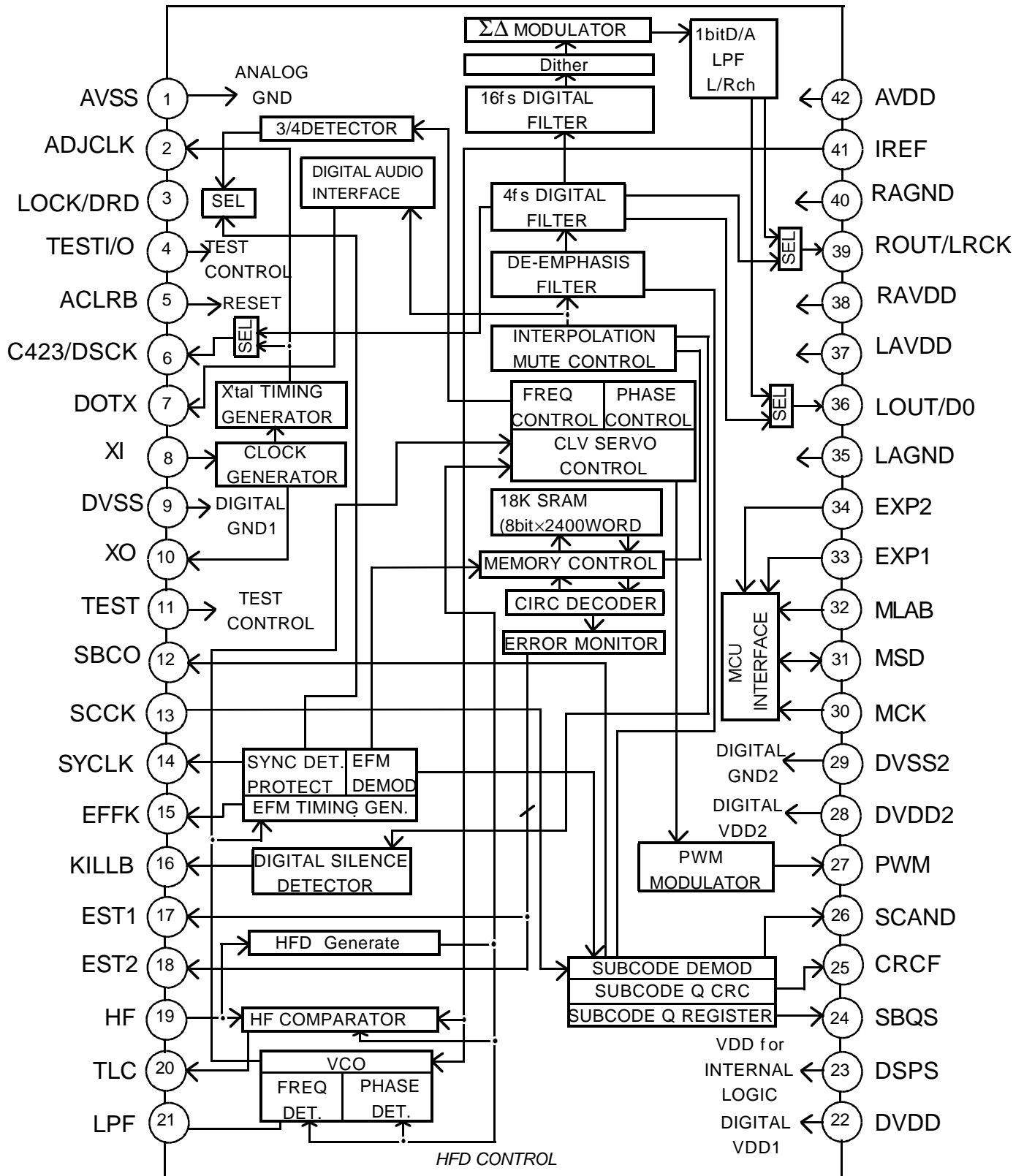## CD PLAYER DIGITAL SIGNAL PROCESSOR WITH BUILT-IN DAC

2. PIN CONFIGURATION

Pin	Left		Pin	Right
1	AVSS		42	AVDD
2	ADJCLK		41	IREF
3	LOCK/DRD		40	RAGND
4	TEST I/O		39	ROUT/LRCK
5	ACLRB		38	RAVDD
6	C423/DSCK		37	LAVDD
7	DOTX		36	LOUT/DO
8	XI		35	LAGND
9	DVSS		34	EXP2
10	XO		33	EXP1
11	TEST		32	MLAB
12	SBCO		31	MSD
13	SCCK		30	MCK
14	SYCLK		29	DVSS2
15	EFFK		28	DVDD2
16	KILLB		27	PWM
17	EST1		26	SCAND
18	EST2		25	CRCF
19	HF		24	SBQS
20	TLC		23	DSPS
21	LPF		22	DVDD

M65824AFP

MITSUBISHI ELECTRIC

M65824AFP

CD PLAYER DIGITAL SIGNAL PROCESSOR WITH BUILT-IN DAC

3. BLOCK DIAGRAM

CD PLAYER DIGITAL SIGNAL PROCESSOR WITH BUILT-IN DAC

4. PIN DESCRIPTION

pin No.	Name	I/O	Function
1	AVSS	-	Analog system GND
2	ADJCLK	O	Clock output for servo adjustment:f=88.2KHz
3	LOCK/DRD	O	Lock monitor / low disc rotation detect output
4	TEST I/O	I	Test control
5	ACLRB	I	System reset input : reset ="L"　　No pull-up
6	C423/DSCK	O	Crystal system clock output f=4.2336MHz　Ext.D/A mode: Data shift clock output
7	DOTX	O	Digital out
8	XI	I	Crystal oscillator input (with Feedback R) f:8.4672MHz
9	DVSS	-	Digital system GND
10	XO	O	Crystal oscillator output
11	TEST	I	Normal/Test select input : Test"H"
12	SBCO	O	Subcode serial output
13	SCCK	I	Shift clock input for subcode data read
14	SYCLK	O	Frame lock status output : Lock="H"
15	EFFK	O	EFM frame clock output : duty=50%
16	KILLB	O	Digital silence : DIGITAL ZERO="L" Opendrain output
17	EST1	O	Error status output 1 "H"When error detect at C1 decoder
18	EST2	O	Error status output 1 "H"When error detect at C2 decoder
19	HF	I	High frequency signal input
20	TLC	O	Slice level control signal output
21	LPF	I/O	Loop filter for PLL
22	DVDD	-	Digital interface power supply
23	DSPS	-	Digital system power supply(internal logic)

CD PLAYER DIGITAL SIGNAL PROCESSOR WITH BUILT-IN DAC

4.PIN DESCRIPTION(CONTINUANCE)

pin No.	Name	I/O	Function
24	SBQS	O	Subcode Q register read interrupt signal "L" for read
25	CRCF	O	CRC checked results of Subcode Q:CRC OK="H"
26	SCAND	O	Subcode sync.signal output:"H" for sync.
27	PWM	O	Disc motor driver PWM output(Both sides)
28	DVDD2	-	Digital interface power supply2
29	DVSS2	-	Digital system GND2
30	MCK	I	Microcomputer interface shift clock input
31	MSD	I/O	Microcomputer interface serial data I/O
32	MLAB	I	Microcomputer interface latch clock Built-in 22KΩ pull up resistor to DVDD
33	EXP1	I	Input pin (be read via serial I/F) No.1 Built-in 4.7KΩ pull up resistor to DVDD
34	EXP2	I	Input pin (be read via serial I/F) No.2 Built-in 4.7KΩ pull up resistor to DVDD
35	LAGND	-	Lch Analog GND
36	LOUT/D0	-	Audio signal output(L-ch) Ext.D/A mode;Audio serial data output
37	LAVDD	O	Lch Analog power supply
38	RAVDD	-	Rch Analog power supply
39	ROUT/LRCK	O	Audio signal output(R-ch) Ext.D/A mode;LR clock output
40	RAGND	-	Rch Analog GND
41	IREF	I	PLL circuit reference current setting
42	AVDD	-	Analog System power supply

Schmitt trigger input is the following

ACLRB(No.5),TEST(No.11),SCCK(No.13),MCK(No.30)

MLAB(No.32),EXP1(No.33),EXP2(No.34)

Reset condition for ACLRB(No.5:No pull-up resistor,Normal CMOS input)

minimum reset time :1μsec

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CD PLAYER DIGITAL SIGNAL PROCESSOR WITH BUILT-IN DAC

5.ABSOLUTE MAXIMUM RATINGS(Ta=25℃,unless otherwise noted)

Symbol	Item	Rating	Unit
DVDD-DVSS	Supply voltage(interface)	-0.3 to +6.5	V
AVDD-AVSS	Supply voltage(analog)	-0.3 to +3.6	V
DSPS-DVSS	Supply voltage(internal)	-0.3 to +3.6	V
Vi	Input voltage	DVSS-0.3≦Vi≦DVDD+0.3	V
Vo	Output voltage	DVSScVo≦DVDD	V
Pd	Power dissipation	350	mV
Topr	Operating temperature	-10 to +70	℃
Tstg	Storage temperature	-40 to +125	℃

6.RECOMMENDED OPERATING CONDITIONS

Symbol	Item	conditions	Min	Typ	Max	Unit
DVDD	Supply voltage (interface)		2.7	5.0	5.5	V
AVDD	Supply voltage (analog)		2.7	3.0	3.3	V
DSPS	Supply voltage (internal)		2.7	3.0	3.3	V
VIH	Input voltage ("H"level)	Except Schmitt input	DVDD×0.7	-	DVDD	V
VIL	Input voltage ("L"level)	Except Schmitt input	DVSS	-	DVDD×0.3	V
fosc	Output frequency	Normal speed	-	8.4672	-	MHz
fvco	Output frequency	Normal speed	-	8.4636	-	MHz

CD PLAYER DIGITAL SIGNAL PROCESSOR WITH BUILT-IN DAC

7.ELECTRICAL CHARACTERISTICS
(Ta=25℃,DVDD=5V,AVDD/DSPS=3V unless otherwise noted)

Symbol	Item	conditions	Min	Typ	Max	Unit
IDD	Circuit current	fosc=8.4672MHz fvco=8.6436MHz	-	20.0	-	mA
VOH	Output voltage ("H"level)	DVDD=5.0V IOH=-1.0mA	4.5	-	-	V
VOL	Output voltage ("L"level)	DVDD=5.0V IOL=1.0mA	-	-	0.4	V
IIH	Input current ("H"level)	VIH=4.5V	-	-	2	μA
IIL	Input current ("L"level)	VIL=0.5V	-2	-	-	μA
Ru	Pull up resistor	EXP1(33),EXP2(34)	2.35	-	9.4	KΩ
		MLAB(32)	11	-	44	
VOH (DOTX)	output voltage ("H"level)	DVDD=5.0V Ioh=-4.0mA	4.6	-	-	V
VOL (DOTX)	output voltage ("L"level)	DVDD=5.0V Iol=4.0mA	-	-	0.4	V
Ileak (DOTX)	output leakage current	DVDD=5V	-	-	10	μA
Tf	output (DOTX) fall time	CL=20pF	-	-	10	nsec
Tr	output (DOTX) rise time	CL=20pF	-	-	10	nsec

8.D/A converter output
(Ta=25℃,DVDD=5V,AVDD/DSPS=3V unless otherwise noted)

Symbol	Item	conditions	Min	Typ	Max	Unit
Vomax	Maximum output voltage	with System construction	1.8	2.0	2.2	V
Freq	Frequency characteristic	with System construction (at 20KHz)	-	-3.0	-	dB
THD	Distortion	20Hz to 20KHz (20KHz LPF)	-	-	0.2	%
SNR	Signal noise ratio	20KHz LPF	72	-	-	dB
		A-weighted(20KHz LPF)	72	-	-	dB
DR	Dynamic range	at-60dB(20KHz LPF)	72	-	-	dB
Vgpass	Passband ripple	at 20KHz	-	-	-1.5	dB

CD PLAYER DIGITAL SIGNAL PROCESSOR WITH BUILT-IN DAC
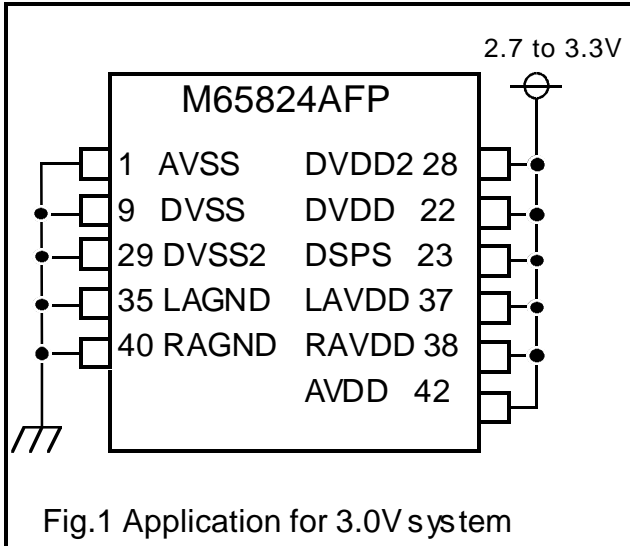
9. POWER SUPPLY
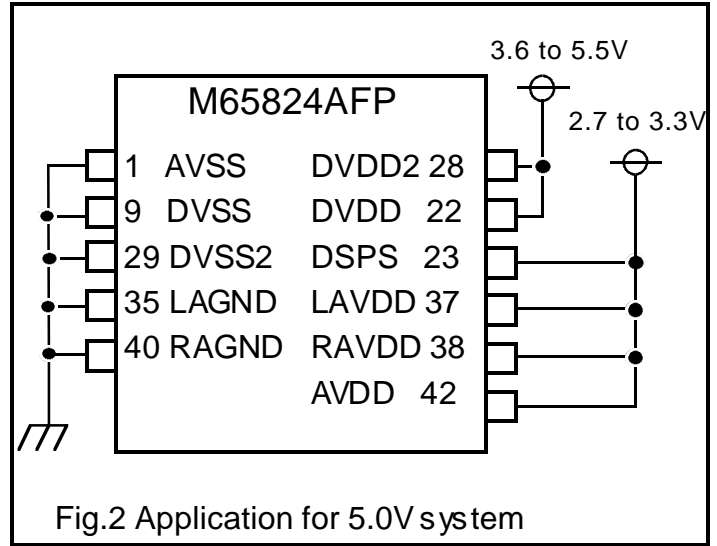

Fig.1 Application for 3.0V system

Fig.2 Application for 5.0V system

Fig.1 shows an application circuit for 3.0V system.
Voltage range is between 2.7V to 3.3V.
Fig.2 shows an application circuit for 5.0V system.
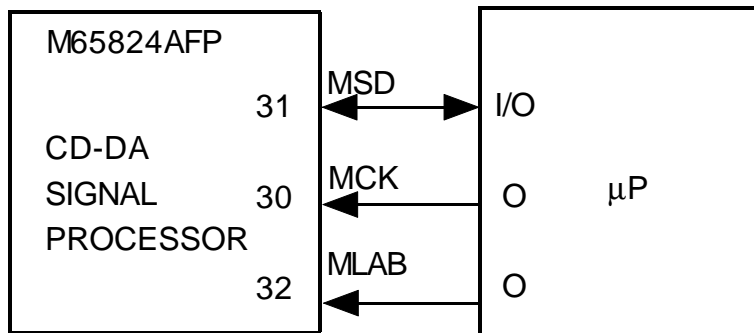The M65824AFP needs dual power supply.
AVSS,DVSS,DVSS2,LAGND and RAGND should be connected to GND(0V).
(Fig.1 and Fig.2)

10. FUNCTION DESCRIPTION

10-1 MICROCOMPUTER INTERFACE

(1) Connection

(2) Pin description
MLAB:Microcomputer latch line for latching commands into the
M65824AFP and for switching the communication mode.
(MLAB=1:µP writes to the M65824AFP)
(MLAB=0:µP reads from the M65824AFP)

CD PLAYER DIGITAL SIGNAL PROCESSOR WITH BUILT-IN DAC

MCK:Microcomputer clock line for clocking bits to or from the
M65824AFP.
MSD:Microcomputer data line for sending or receiving data bits from
the M65824AFP.

(3) Operation

*Microcomputer command read/write operation
The data bits (MSD) are accepted on the rising edge of the clock
pulse(MCK).The falling edge of the latch line(MLAB) decides the
complete command.
At the same moment the data line is switched to output mode and
indicates the status as requested by data bits D3,D2,D1 and D0.
When the latch line becomes high,the data line is switched to
input mode.

*Status request / interface command
If the microcomputer wants to read a certain status, it has to
write a status request command with the appropriate bits D3,D2,D1
and D0 to the M65824AFP. After latching the command into the
M65824AFP, the data line becomes the request status information
as long as the latch line(MLAB) remains low.

(4) Microcomputer I/O timing
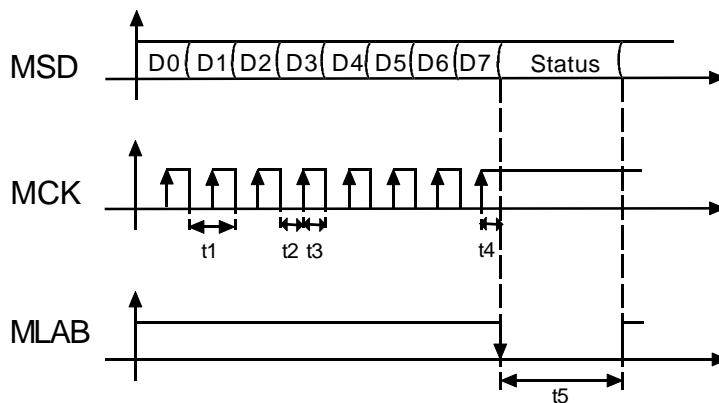
t1:Shift clock width   (min.200nsec)
t2:Shift clock setup time   (min.100nsec)
t3:Shift clock hold time   (min.100nsec)
t4.Latch pulse setup time   (min.100nsec)
t5:Latch pulse width 50nsec≦t5≦50μs
    Subcode-Q reading:50nsec≦t5

CD PLAYER DIGITAL SIGNAL PROCESSOR WITH BUILT-IN DAC

(5) M65824AFP commands table

Initial value after power on:00000000

D7	D6	D5	D4	D3	D2	D1	D0
Disc motor mode		Audio function		Status Request/Interface command			

(6) Data description

① Reset condition

function	Internal D/A mode , DOTX : OFF , Disc motor switched off , Audio muted , ACCK clock level ϫ II

② Disc motor Mode

D7	D6	Function
0	0	Disc motor switched off
0	1	Disc motor accelerate,applies maximum voltage for acceleration to the disc motor
1	0	Disc motor brake,applies maximum voltage for braking to the disc motor
1	1	Disc motor CLV control mode

③ Audio function

D5	D4	Function
0	0	Audio muted
0	1	Audio mute off
1	0	***Prohibited***
1	1	Audio attenuate by 12dB

④ Status request / Interface command

D3	D2	D1	D0	Function
0	0	0	0	Disc rotation down status,Status="L" when disc motor speed <2/3 of nominal speed
0	0	0	1	PLL lock status,Status="L" when PLL is locked
0	0	1	0	Subcode ready status,Status="L" when new subcode has been received
0	0	1	1	Status=Logical value of EXP1(Pin33)
0	1	0	0	Status=Logical value of EXP1(Pin34)
0	1	0	1	DOTX output
0	1	1	0	DOTX off (high impedance)
0	1	1	1	ACCK Clock accuracy input Level
1	0	0	0	ACCK Clock accuracy input Level
1	0	0	1	External D/A mode (IIS)
1	0	1	0	External D/A mode (EIAJ)
1	1	1	1	Internal D/A mode

CD PLAYER DIGITAL SIGNAL PROCESSOR WITH BUILT-IN DAC
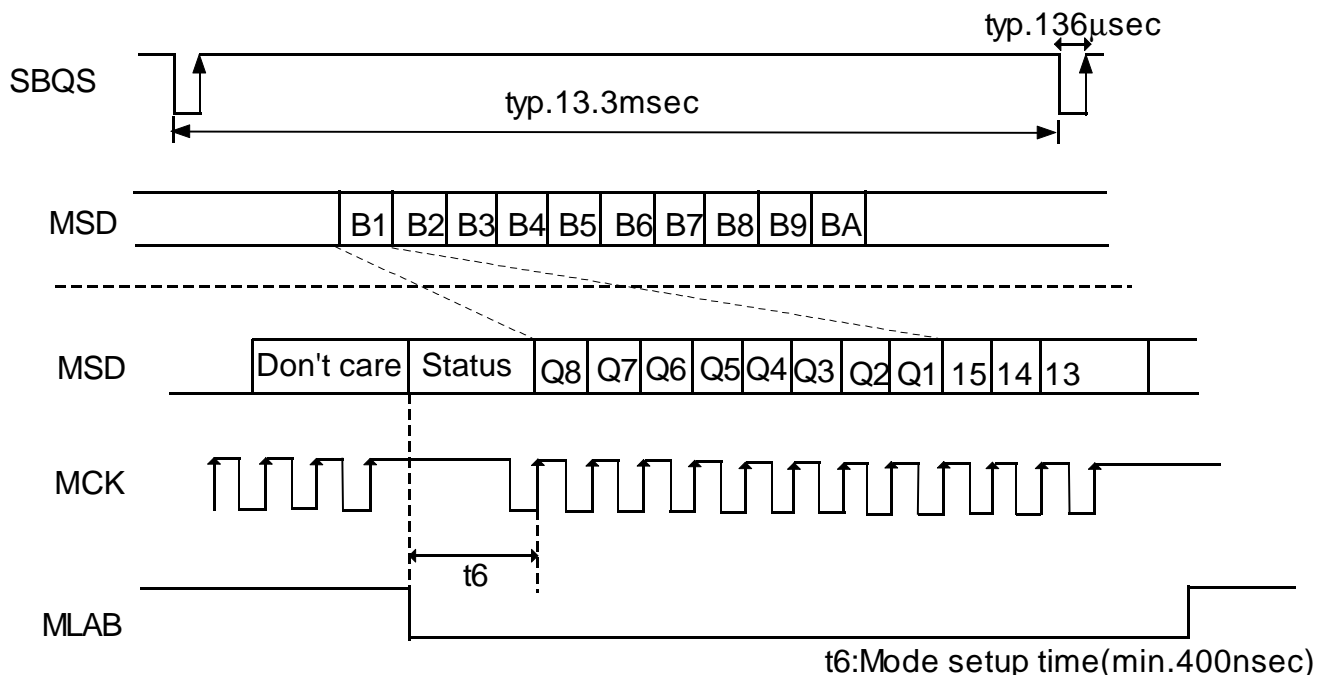
(7) Subcode Q register interface

The data of subcode Q stored in the internal 80-bit register can be read with a serial clock from the microcomputer.

Procedure

1. THE microcomputer has to issue a subcode ready status command to the M65824AFP.
   Set MSD data "0100xxxx" and write to the M65824AFP.
2. If the status returned by the M65824AFP equals to subcode ready (status="L") then the microcomputer can read a subcode-Q data.
3. If the status is ready then the microcomputer starts clocking out the subcode-Q data from the M65824AFP with remaining the latch line "MLAB" status "L" as long as the microcomputer requires.
4. The microcomputer certainly sends 81 clocks.
   From the first clock to 80th clock read out subcode-Q data and 81th clock sets the status "H".
5. When the microcomputer finishes reading the subcode-Q data, (send 81 clocks) "MLAB" should be changed from "L" to "H".
6. If communication is aborted or doesn't finish normally,the M65824AFP and sends 81 clocks for initializing the internal 80-bit register and setting status "H".

typ.136μsec

SBQS   typ.13.3msec

MSD   B1 B2 B3 B4 B5 B6 B7 B8 B9 BA

MSD   Don't care | Status | Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1 15 14 13

MCK

t6

MLAB

t6:Mode setup time(min.400nsec)

CD PLAYER DIGITAL SIGNAL PROCESSOR WITH BUILT-IN DAC

Description

① Conditions under which the SBQS is placed in "L"

(a) When the CRC checked results is good.

(b) When both subcode sync signals S0 and S1 are detected in the specified position

When both conditions (a) and (b) above are satisfied, the SBQS pin outputs "L".

② If SBQS does not turn to "L" then the subcode ready status indicates "H" (=not ready).When the subcode ready status is "H",the microcomputer can not read a valid subcode Q-channel data from the M65824AFP.

③ The subcode-Q data is renewed at the same timing of the signal "SBQS" status is "L".

When the microcomputer send a subcode ready status command,if the signal "MLAB" is changed from "H" to "L" during the signal "SBQS" status is "L" then the M65824AFP will return the status not ready. (status="H")

While the latch line "MLAB" is remained "L", the subcode-Q data is not renewed.

④ The M65824AFP output a subcode-Q data with reversed each 1-byte.

(8)Subcode interface R-W

The subcode data(P,Q,R,S,T,U,V,W) can be read from the SBCO pin by inputting clocks to the SCCK pin among the data converted from 14-bit EFM signal to 8-bit symbol.

When both subcode sync. patterns S0,S1 are detected in the specified position as a sync. signal of this subcode, a sync. signal is output from SCAND pin.

If 8 or more clocks are input to the SCCK, the SBCO is placed in "L".

10-2 DISCMOTORCONTROLPULSE(CLVMODE)
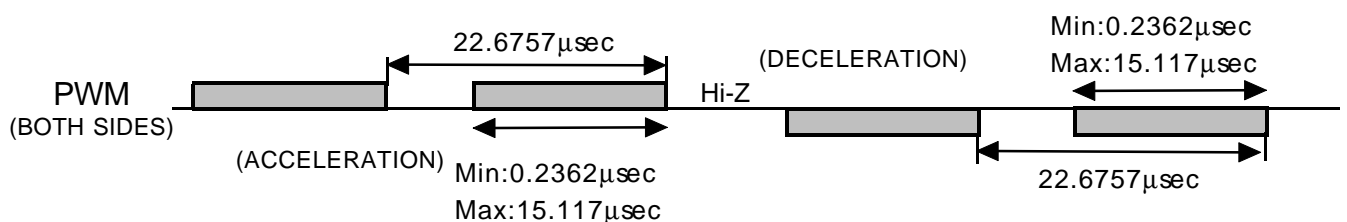
CD PLAYER DIGITAL SIGNAL PROCESSOR WITH BUILT-IN DAC

10-4. EFM - PLL circuit
(1) Data slicing / PLL

The M65824AFP has an analog front -end for incoming HF (EFM) signal. Using CMOS - Analog technology , the front - end is comprised of an automatic slice level control circuit and EFM - PLL circuit with internal adjust - free VCO. Under figure shows a block - diagram of the analog front - end. The HF signal is sliced by the HF comparator and a DC level is feed back from TLC to HF through some the external CR. If HFD becomes "H" because of defect in disk, then TLC becomes off state and holds the DC level. EFM -PLL is for extracting the EFM clock signal from the HF signal. The PLL circuit has a phase / frequency comparator so the M65824AFP has a wide capture / lock range and there is no need to adjust the VCO. LPF is the charge- pump output and same - time control voltage input to the VCO. LPF becomes off state if HFD becomes "H".
IREF is the reference current input used to determine the current of charge pumps of TLC and LPF, operating point of HF comparator , and VCO free running frequency.
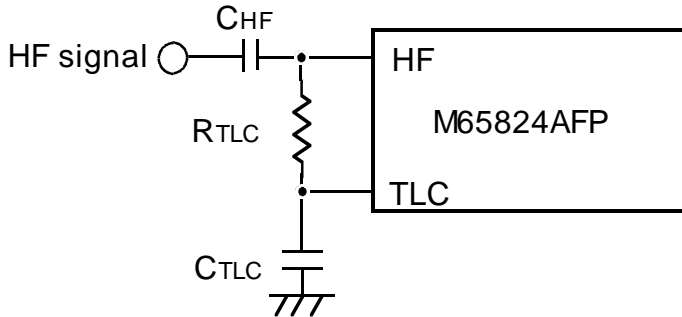If IREF is connected to a noisy power supply through a resistor , the VCO would be modulated and the error - rate would increase. Therefore , power supply noise at IREF must be held to a minimum.
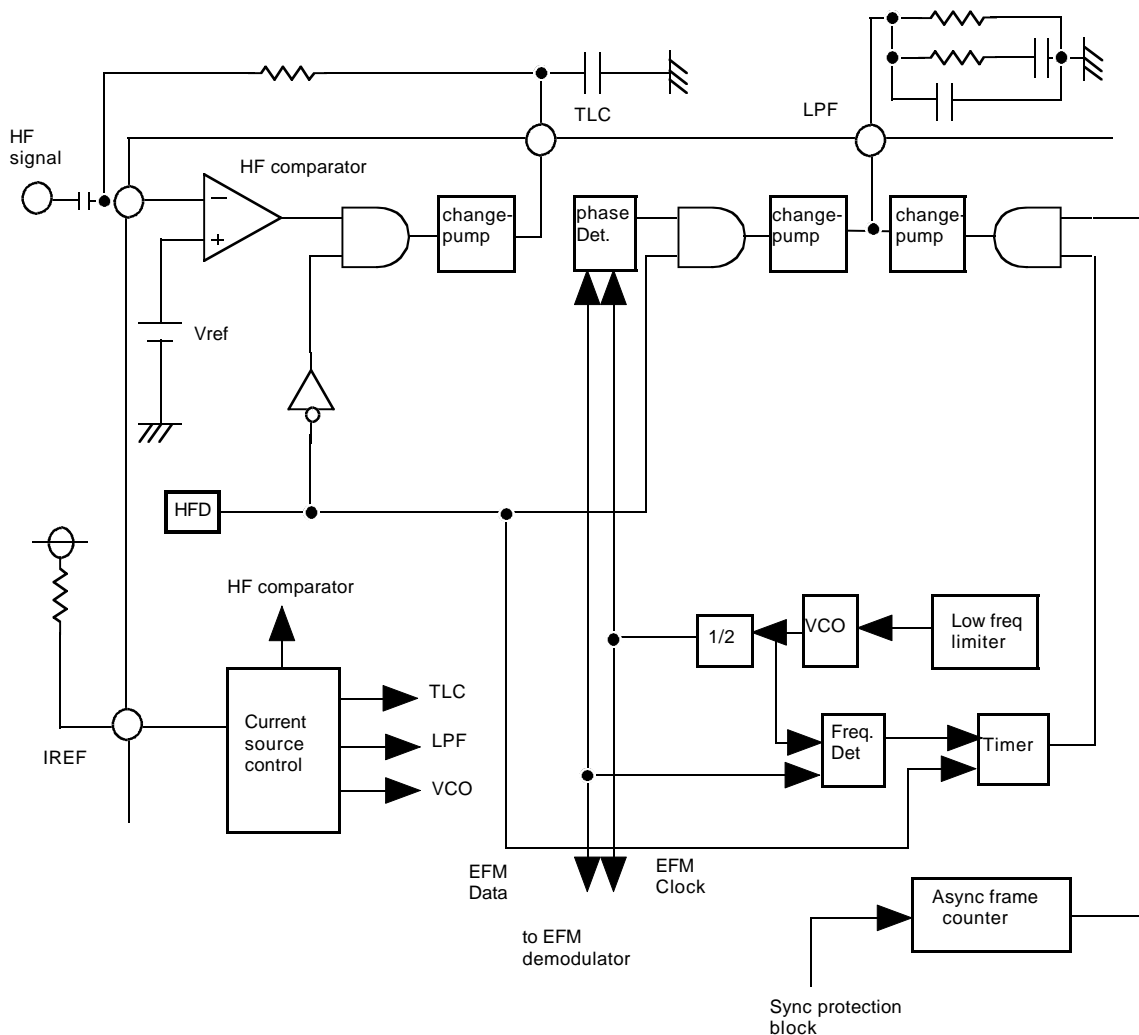
CD PLAYER DIGITAL SIGNAL PROCESSOR WITH BUILT-IN DAC

(2) Automatic slice level control

The slice level control circuit is formed by connecting a resistor and capacitors to the HF (High - frequency signal input) pins. TLC(Slice level control output) pins.
(Tentative Value)

C_{HF}=0.0010μF
C_{TLC}=0.022μF
R_{TLC}=33KΩ
Vin HF 0.5Vp-p min

Since the adjustment - free VCO is built in, the adjustment - free PLL circuit can be formed by connecting a resistor and capacitors to the LPF (Low - pass filter) pin.
(Tentative Value)

C_{LPF}=470pF
C1=0.15μF to 1.0μF*
R_{LPF}=1.8KΩ
R_{PD}=3.3MΩ

(3) PLL circuit

From 0.15μF to 1.0μF capacitor is available for C1.

In high speed search such as track count search,the rotation of disc decrease. If this is problem, this problem is improved by using large C1.

A resistor must be connected between the IREF pin and VDD in order to set the reference current used in determining the current values of the TLC pin and LPF pin , the comparator operating current of the slice level control circuit , and the VCO free - run frequency.
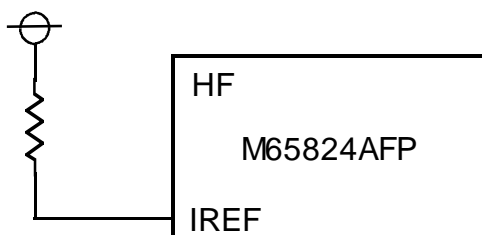(Tentative Value)

R_{IREF}=100KΩ (Normal speed)
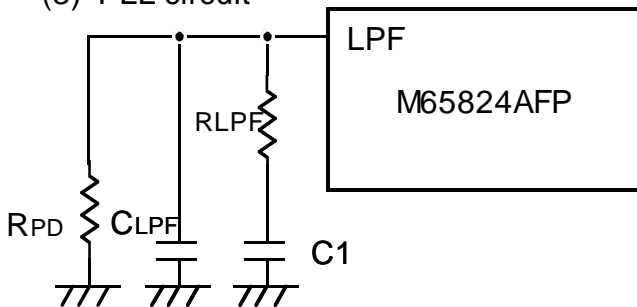
(4) Reference current

CD PLAYER DIGITAL SIGNAL PROCESSOR WITH BUILT-IN DAC

10-5.EFM demodulation

The EFM signal that has been converted to logic level , and the EFM clock that has been extracted from the EFM signal are input to the demodulator and convert to 8bit symbol.

The EFM demodulation depend on EFM table in the RED book.

To demodulate , the demodulator must be synchronized to EFM signal for each frame. The frame sync.protection circuit holds the synchronization inspire of some lack of sync.pattern, and prevents false synchronization of the demodulator bit - slipping or mis - synchronization occurs.
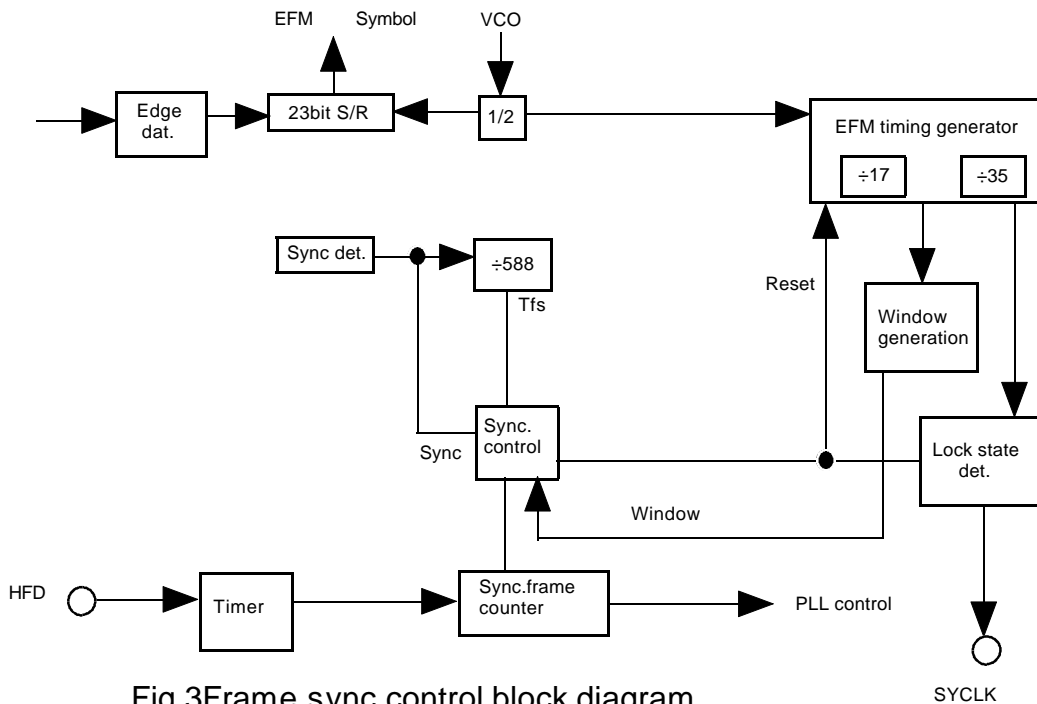
Frame sync.control block diagram show Fig.3.

Fig.3Frame sync.control block diagram

The generating condition of counter reset signal (Reset) in the EFM timing generator is indicated as follows

$$Reset = (Sync * Tfs) + (Sync * Window)$$

*:Logical product

+:Logical sun

Sync:Synchronizing signal

Tfs:Detection signal of synchronizing signal

space = 588

Window:Window signal ±7ck

In the synchronous state , Sync and Tfs generate simultaneously and Sync comes to the center of the window. At this time , "H" is output to the SYCLK pin , and EFM signal is synchronized by frame unit.

Content	SYCLK
Frame lock	L
Frame unlock	H

CD PLAYER DIGITAL SIGNAL PROCESSOR WITH BUILT-IN DAC

To monitor a sync.state with a control microcomputer,it is necessary to provide a signal from which a short-period missing of sync.pattern due to a disc defect,which occurs even in a sync.state is eliminated.

In M65824AFP, this signal is allocated to LOCK/DRD pins.When the braking instruction from the microcomputer is not input, the LOCK/DRD pins monitor the sync.state in 1/16period of EFM frame clock, outputting the results; if monitored status is "locked" then output is "H" , continuous 8 times "unlocked " output becomes "L".

And , when the disc rotation does not become the target speed , lock monitor may become "LOCK" state. In such state , some internal circuit does not work. So when the disc rotation become the target speed and change from rough servo mode to CLV mode , LOCK / DRD output lock monitor.

LOCK/DRD pin outputs DRD signal when the disc motor is braking under the command from MCU.

Condition	Content	LOCK/DRD
Not BRAKE status	Unlock by 1/16 frame clock	L
	Lock by 1/16 frame clock (Not CLV mode)	
	Lock by 1/16 frame clock (CLV mode)	H
BRAKE status	Low disc rotation monitor signal	DRD signal

CD PLAYER DIGITAL SIGNAL PROCESSOR WITH BUILT-IN DAC

10-6 Low disc rotary control
When M65824AFP detects than the number of rotations is less than 2/3 that of the normal play state and the disc motor is braking under the command from MCU, it outputs the disc rotation deterioration signal to LOCK / DRD pin.
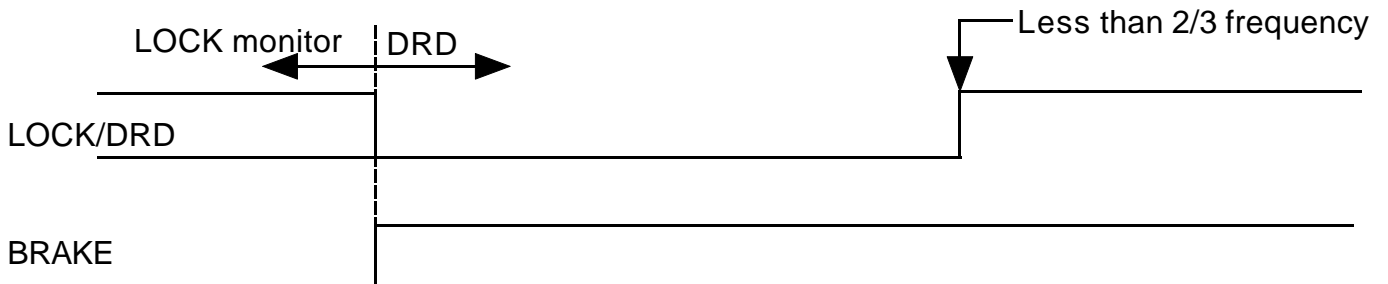
Term	Content	LOCK/DRD
Not BRAKE	Sync.status monitor output	LOCK
BRAKE	Disc rotation speed is more than 2/3	L
	Disc rotation speed is less than 2/3	H

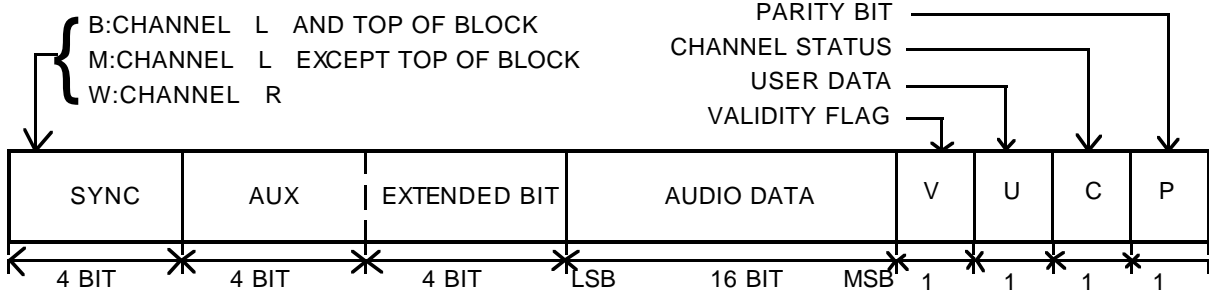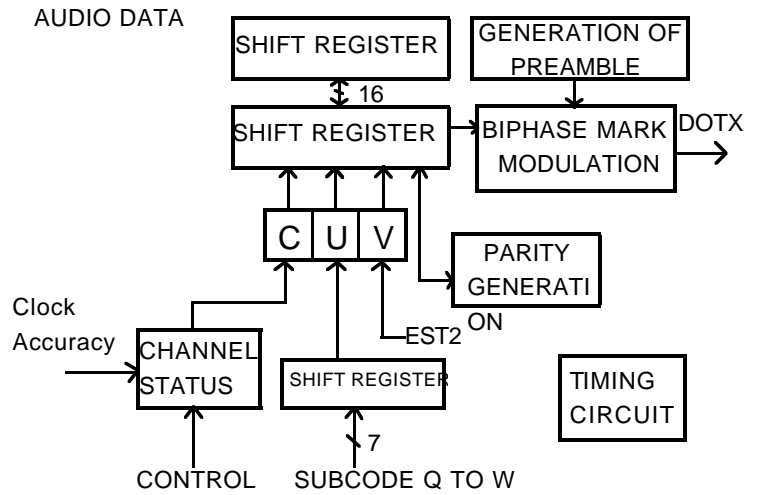## CD PLAYER DIGITAL SIGNAL PROCESSOR WITH BUILT-IN DAC

10-7. DIGITAL OUT

The digital audio signal formatted according to EIAJ
Standard CP-340 "Digital Audio Interface" is
outputted to DOTX pin.
The validity flag is internally set to "1" automatically
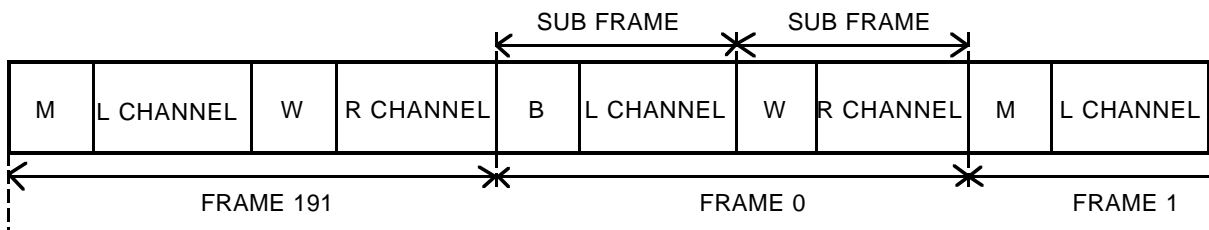when the interpolated word is transmitted.
The user data, which is read in the subcode
interface
circuit,is transmitted.
Channel clock precision can be set from the outside
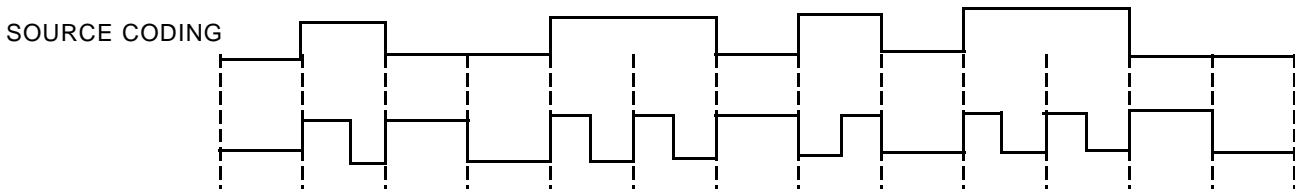so that it is compatible with the validity pitch.
The channel status is set to level Ⅲ in the validity
pitch,mode,and level Ⅱ is set automatically when it
is not in the validity pitch mode.

AUDIO DATA

SHIFT REGISTER   GENERATION OF PREAMBLE

↕ 16

SHIFT REGISTER → BIPHASE MARK MODULATION → DOTX

C | U | V

Clock
Accuracy

CHANNEL STATUS   SHIFT REGISTER

EST2

PARITY GENERATION

TIMING CIRCUIT

CONTROL   SUBCODE Q TO W
7

{
B:CHANNEL L AND TOP OF BLOCK
M:CHANNEL L EXCEPT TOP OF BLOCK
W:CHANNEL R
}

PARITY BIT
CHANNEL STATUS
USER DATA
VALIDITY FLAG

SYNC	AUX	EXTENDED BIT	AUDIO DATA	V	U	C	P
4 BIT	4 BIT	4 BIT / LSB	16 BIT / MSB	1	1	1	1

SUB frame format

SUB FRAME   SUB FRAME

M	L CHANNEL	W	R CHANNEL	B	L CHANNEL	W	R CHANNEL	M	L CHANNEL

FRAME 191   FRAME 0   FRAME 1

Frame format

SOURCE CODING

Channel coding(Biphase mark modulation)

If Digital-OUT is not used to prevent spurious radiation, it
is possible to turn DOTX pin output "OFF" by setting mode
command of microcomputer interface.
Channel status clock precision can be set by ACCK command
of microcomputer interface.

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10-8.HFD

HFD is high frequency signal missing detect circuit.

HFD is "ON" at HF signal missing.

1) TLC voltage "hold"

2) LPF output "open"

3) PWM output "regular acceleration"

TLC voltage hold unit

The block diagram for this TLC voltage hold unit is shown in Fig.4 below.

This unit holds TLC voltage in stable condition and gives this voltage at HF signal missing.

This unit holds two kinds of TLC voltage. By this method, this unit does not hold TLC voltage at HF signal missing and this unit can follow a difference of TLC voltage with the Disc.
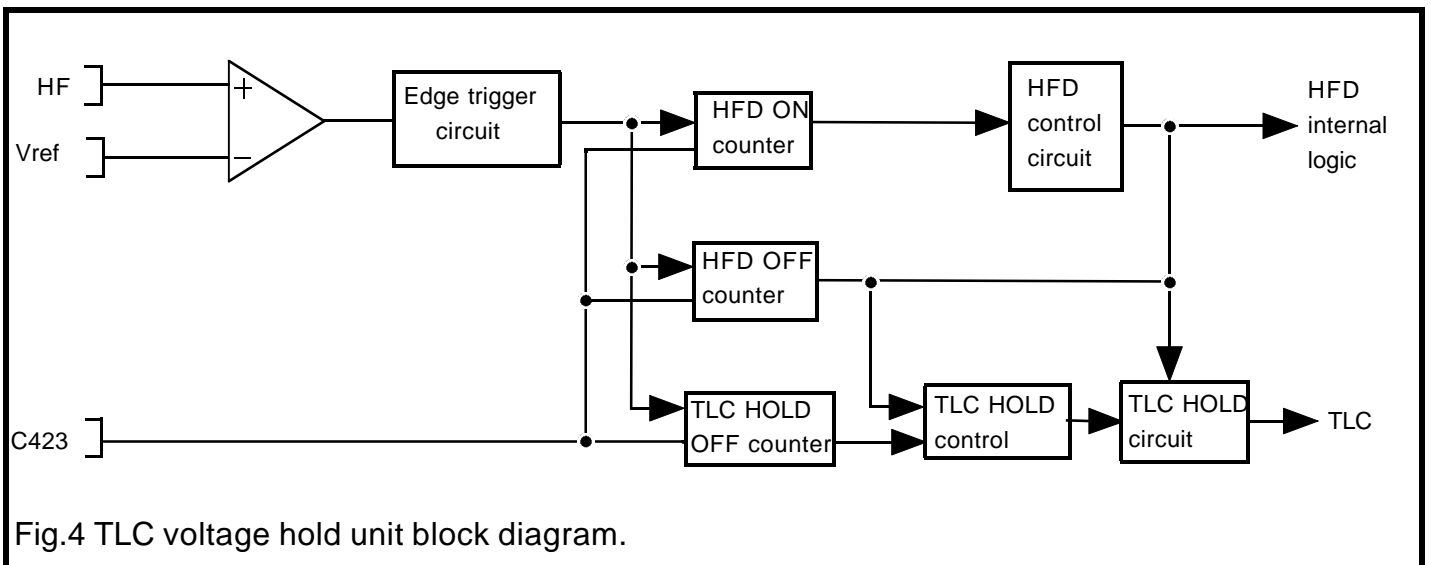

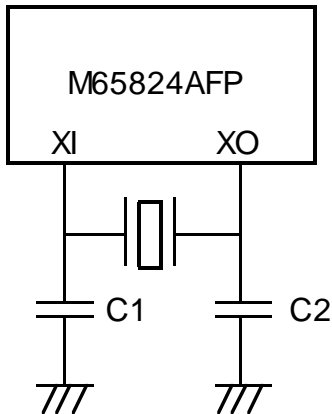Fig.4 TLC voltage hold unit block diagram.

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10-9. Oscillation circuit

(1)Internal oscillation mode
The oscillation circuit can be formed by connecting a crystal
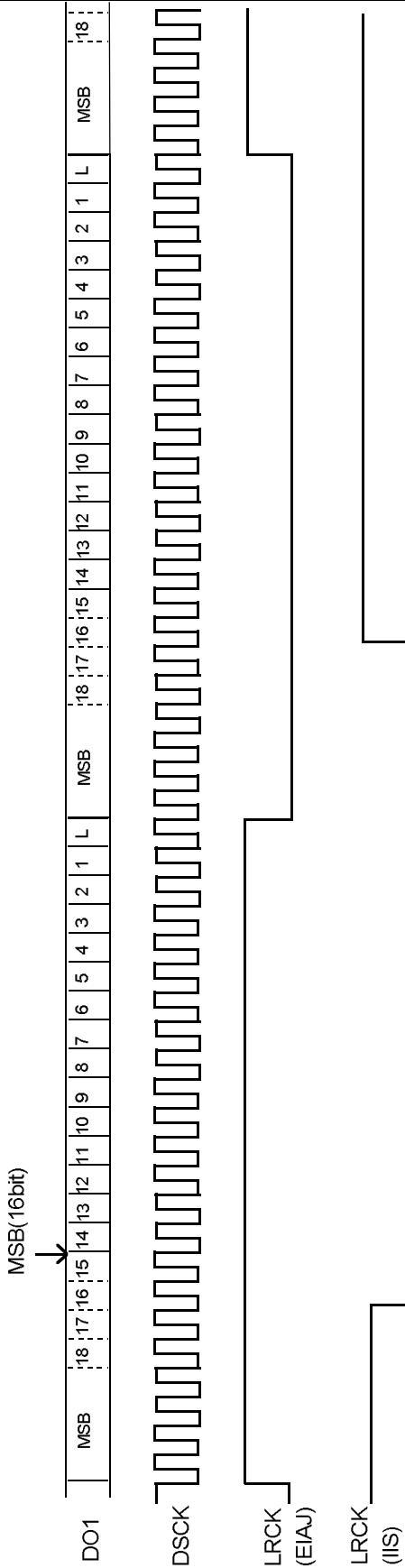oscillator(8.4672MHz)and load capacitors to pins XI and XO.

Oscillator	load capacitor value(Reference)
8.4672MHz	30pF

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10-10. D/A converter interface (External D/A mode)

Symbol	Parameter	Test conditions	Limits			UNIT
			Min	Typ	Max	
tr	rise time	CL=20pF(10%-90%)	-	-	15	nsec
tf	fall time	CL=20pF(10%-90%)	-	-	15	nsec

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11. System construction