



M68Z128W

3V, 1 Mbit (128Kb x8) Low Power SRAM with Output Enable

- LOW VOLTAGE: 3.0V (+0.6V / -0.3V)
- 128Kb x 8 LOW POWER SRAM with OUTPUT ENABLE
- EQUAL CYCLE and ACCESS TIMES: 70ns
- LOW V_{CC} DATA RETENTION: 1.4V
- TRI-STATE COMMON I/O
- LOW ACTIVE and STANDBY POWER
- INTENDED for USE with ST ZEROPOWER[®] and TIMEKEEPER[®] CONTROLLERS

DESCRIPTION

The M68Z128W is a 1 Mbit (1,048,576 bit) Fast CMOS SRAM, organized as 131,072 words by 8 bits. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 3.0V (+0.6V / -0.3V) supply, and all inputs and outputs are TTL compatible. This device has an automatic power-down feature, reducing the power consumption by over 99% when deselected. The M68Z128W is available in the standard 450mil-wide TSOP type 1 package.

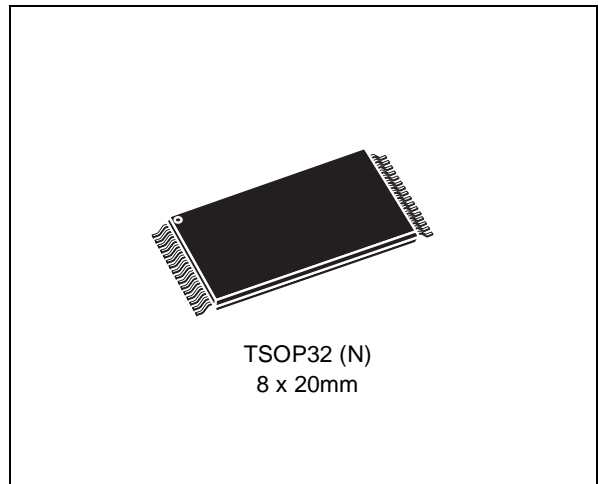


Figure 1. Logic Diagram

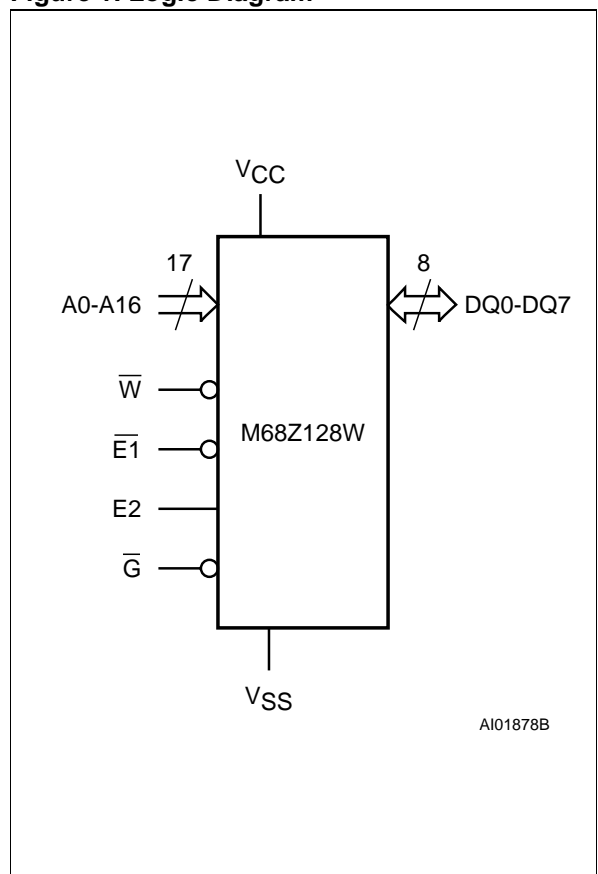


Table 1. Signal Names

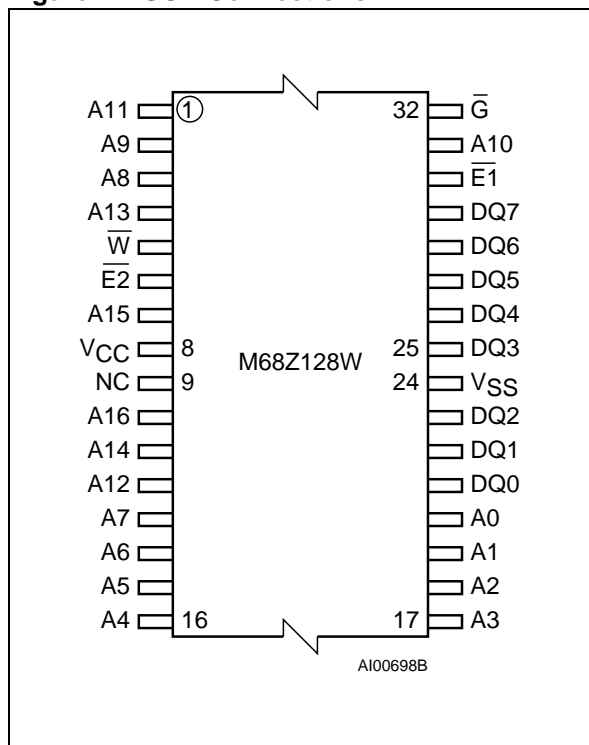
A0-A16	Address Inputs
DQ0-DQ7	Data Input/Output
$\bar{E}1$	Chip Enable 1
E2	Chip Enable 2
\bar{G}	Output Enable
\bar{W}	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T _A	Ambient Operating Temperature	0 to 70	°C
T _{STG}	Storage Temperature	-65 to 150	°C
V _{IO} (2)	Input or Output Voltage	-0.5 to V _{CC} + 0.5	V
V _{CC}	Supply Voltage	-0.5 to 4.6	V
I _O (3)	Output Current	20	mA
P _D	Power Dissipation	1	W

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
 2. Up to a maximum operating V_{CC} of 3.6V only.
 3. One output at a time, not to exceed 1 second duration.

Figure 2. TSOP Connections



READ MODE

The M68Z128W is in the Read mode whenever Write Enable (\overline{W}) is High with Output Enable (\overline{G}) Low, and both Chip Enables ($\overline{E1}$ and $\overline{E2}$) are asserted. This provides access to data from eight of

the 1,048,576 locations in the static memory array, specified by the 17 address inputs. Valid data will be available at the eight output pins within t_{AVQV} after the last stable address, providing \overline{G} is Low, $\overline{E1}$ is Low and $\overline{E2}$ is High. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{E1LQV}, t_{E2HQV}, or t_{GLQV}) rather than the address. Data out may be indeterminate at t_{E1LQX}, t_{E2HQX} and t_{GLQX}, but data lines will always be valid at t_{AVQV}.

WRITE MODE

The M68Z128W is in the Write mode whenever the \overline{W} and $\overline{E1}$ pins are Low, with $\overline{E2}$ High. Either the Chip Enable inputs ($\overline{E1}$ and $\overline{E2}$) or the Write Enable input (\overline{W}) must be de-asserted during Address transitions for subsequent write cycles. Write begins with the concurrence of both Chip Enables being active with \overline{W} low. Therefore, address setup time is referenced to Write Enable and both Chip Enables as t_{AVWL}, t_{AVE1L} and t_{AVE2H} respectively, and is determined by the latter occurring edge.

The Write cycle can be terminated by the earlier rising edge of $\overline{E1}$, \overline{W} , or the falling edge of $\overline{E2}$.

If the Output is enabled ($\overline{E1}$ = Low, $\overline{E2}$ = High and \overline{G} = Low), then \overline{W} will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVE1H} before the rising edge of $\overline{E1}$ or for t_{DVE2L} before the falling edge of $\overline{E2}$, whichever occurs first, and remain valid for t_{WHDX}, t_{E1HDX} or t_{E2LDX}.

Table 3. Operating Modes

Operation	$\overline{E1}$	E2	\overline{W}	\overline{G}	DQ0-DQ7	Power
Read	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Hi-Z	Active
Read	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Data Output	Active
Write	V_{IL}	V_{IH}	V_{IL}	X	Data Input	Active
Deselect	V_{IH}	X	X	X	Hi-Z	Standby
Deselect	X	V_{IL}	X	X	Hi-Z	Standby

Note: 1. X = V_{IH} or V_{IL} .

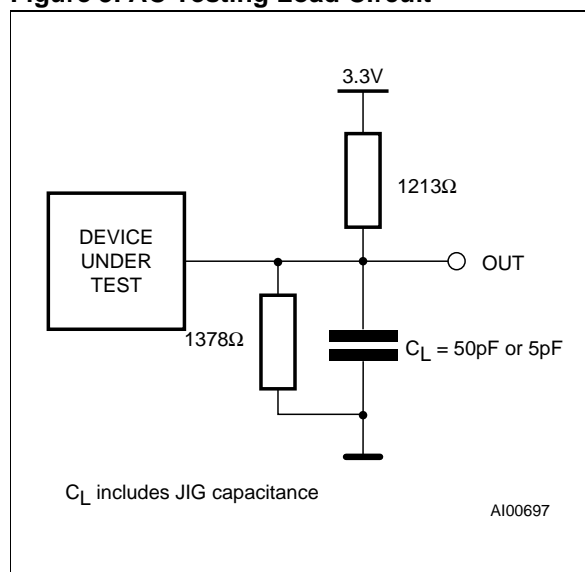
Table 4. AC Measurement Conditions

Input Rise and Fall Times	$\leq 15\text{ns}$
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note: Output Hi-Z is defined as the point where data is no longer driven.

OPERATIONAL MODE

The M68Z128W has a Chip Enable power down feature which invokes an automatic standby mode whenever either Chip Enable is de-asserted ($\overline{E1}$ = High or E2 = Low). An Output Enable (\overline{G}) signal provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus. Operational modes are determined by device control inputs \overline{W} , $\overline{E1}$, and E2 as summarized in the Operating Modes table.

Figure 3. AC Testing Load Circuit**Table 5. Capacitance ⁽¹⁾ ($T_A = 25\text{ }^\circ\text{C}$, $f = 1\text{ MHz}$)**

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance on all pins (except DQ)	$V_{IN} = 0V$		6	pF
$C_{OUT}^{(2)}$	Output Capacitance	$V_{OUT} = 0V$		8	pF

Note: 1. Sampled only, not 100% tested.
2. Outputs deselected.

Figure 4. Block Diagram

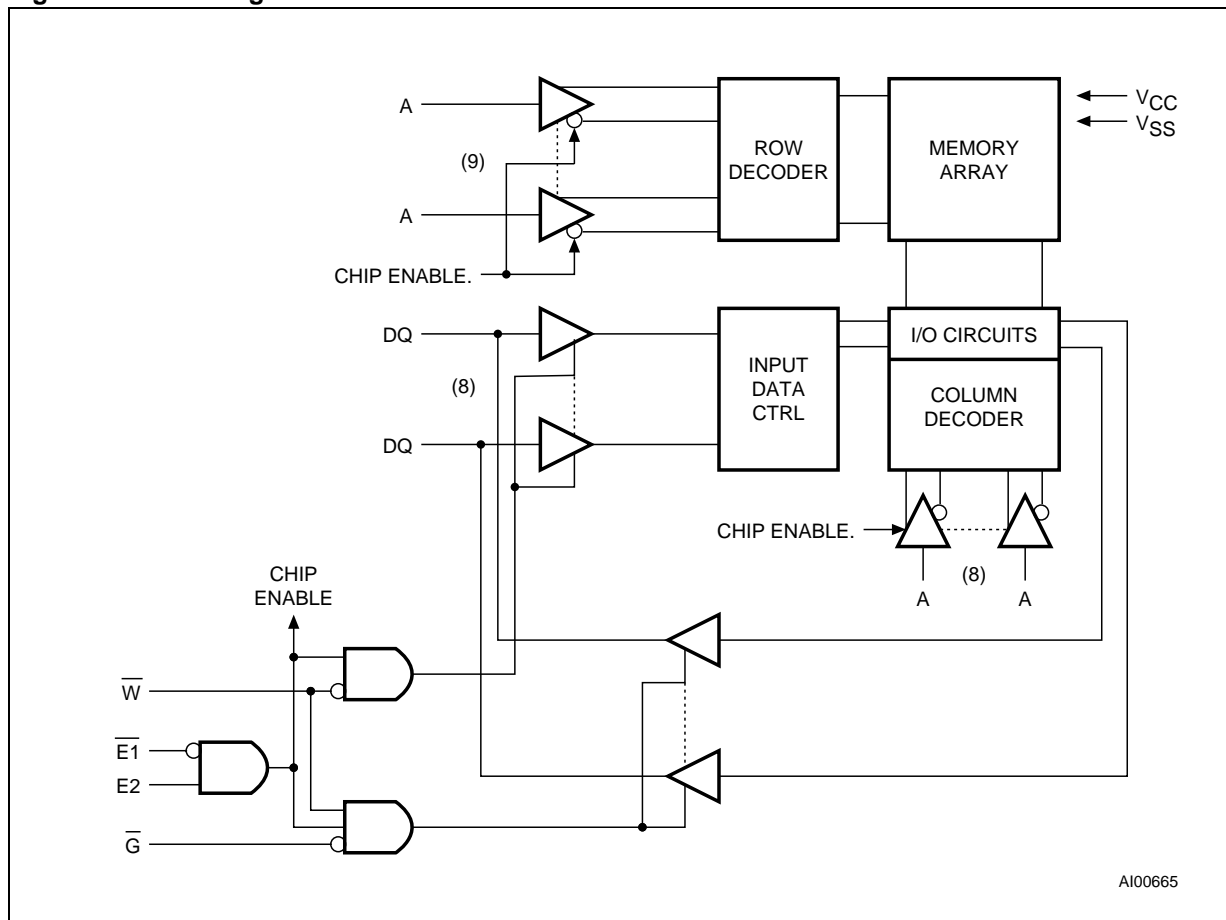


Table 6. DC Characteristics
($T_A = 0$ to 70°C ; $V_{CC} = 3.0\text{V} + 0.6\text{V} / -0.3\text{V}$)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$0\text{V} \leq V_{IN} \leq V_{CC}$			± 1	μA
I_{LO}	Output Leakage Current	$0\text{V} \leq V_{OUT} \leq V_{CC}$			± 1	μA
$I_{CC1}^{(1)}$	Supply Current	$V_{CC} = 3.6\text{V}, (-70)$		20	40	mA
$I_{CC2}^{(2)}$	Supply Current (Standby) TTL	$V_{CC} = 3.6\text{V}, \bar{E}1 = V_{IH}$ or $E2 = V_{IL}, f = 0$		15	300	μA
$I_{CC3}^{(3)}$	Supply Current (Standby) CMOS	$V_{CC} = 3.6\text{V}, \bar{E}1 \geq V_{CC} - 0.2\text{V}$ or $E2 \leq 0.2\text{V}, f = 0$		0.4	15	μA
V_{IL}	Input Low Voltage		-0.5		0.8	V
V_{IH}	Input High Voltage		2		$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$			0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -1\text{mA}$	2.4			V

Note: 1. Average AC current, Outputs open, cycling at t_{AVAV} minimum.
 2. All other Inputs at $V_{IL} \leq 0.8\text{V}$ or $V_{IH} \geq 2.0\text{V}$.
 3. All other Inputs at $V_{IL} \leq 0.2\text{V}$ or $V_{IH} \geq V_{CC} - 0.2\text{V}$.

Table 7. Read and Standby Modes AC Characteristics
 ($T_A = 0$ to 70°C ; $V_{CC} = 3.0\text{V} + 0.6\text{V} / -0.3\text{V}$)

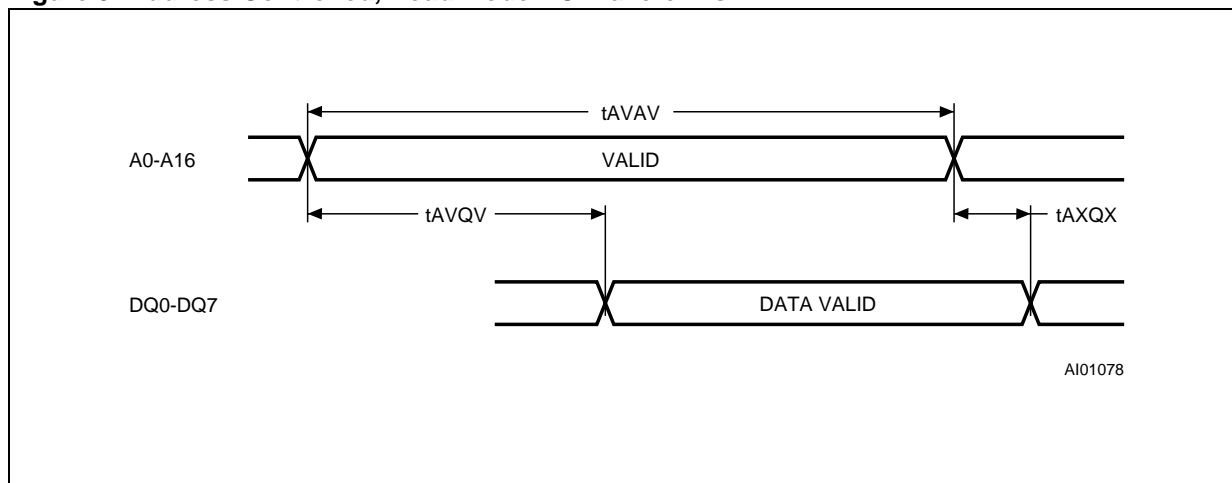
Symbol	Parameter	M68Z128W		Unit
		-70		
		Min	Max	
t_{AVAV}	Read Cycle Time	70		ns
$t_{AVQV}^{(1)}$	Address Valid to Output Valid		70	ns
$t_{E1LQV}^{(1)}$	Chip Enable 1 Low to Output Valid		70	ns
$t_{E2HQV}^{(1)}$	Chip Enable 2 High to Output Valid		70	ns
$t_{GLQV}^{(1)}$	Output Enable Low to Output Valid		35	ns
$t_{E1LQX}^{(3)}$	Chip Enable 1 Low to Output Transition	10		ns
$t_{E2HQX}^{(3)}$	Chip Enable 2 High to Output Transition	10		ns
$t_{GLQX}^{(3)}$	Output Enable Low to Output Transition	10		ns
$t_{E1HQZ}^{(2,3)}$	Chip Enable 1 High to Output Hi-Z	0	25	ns
$t_{E2LQZ}^{(2,3)}$	Chip Enable 2 Low to Output Hi-Z	0	25	ns
$t_{GHQZ}^{(2,3)}$	Output Enable High to Output Hi-Z	0	25	ns
$t_{AXQX}^{(1)}$	Address Transition to Output Transition	10		ns
t_{PU}	Chip Enable 1 Low or Chip Enable 2 High to Power Up	0		ns
t_{PD}	Chip Enable 1 High or Chip Enable 2 Low to Power Down		70	ns

Note: 1. $C_L = 50\text{pF}$ (see Figure 3).

2. $C_L = 5\text{pF}$ (see Figure 3).

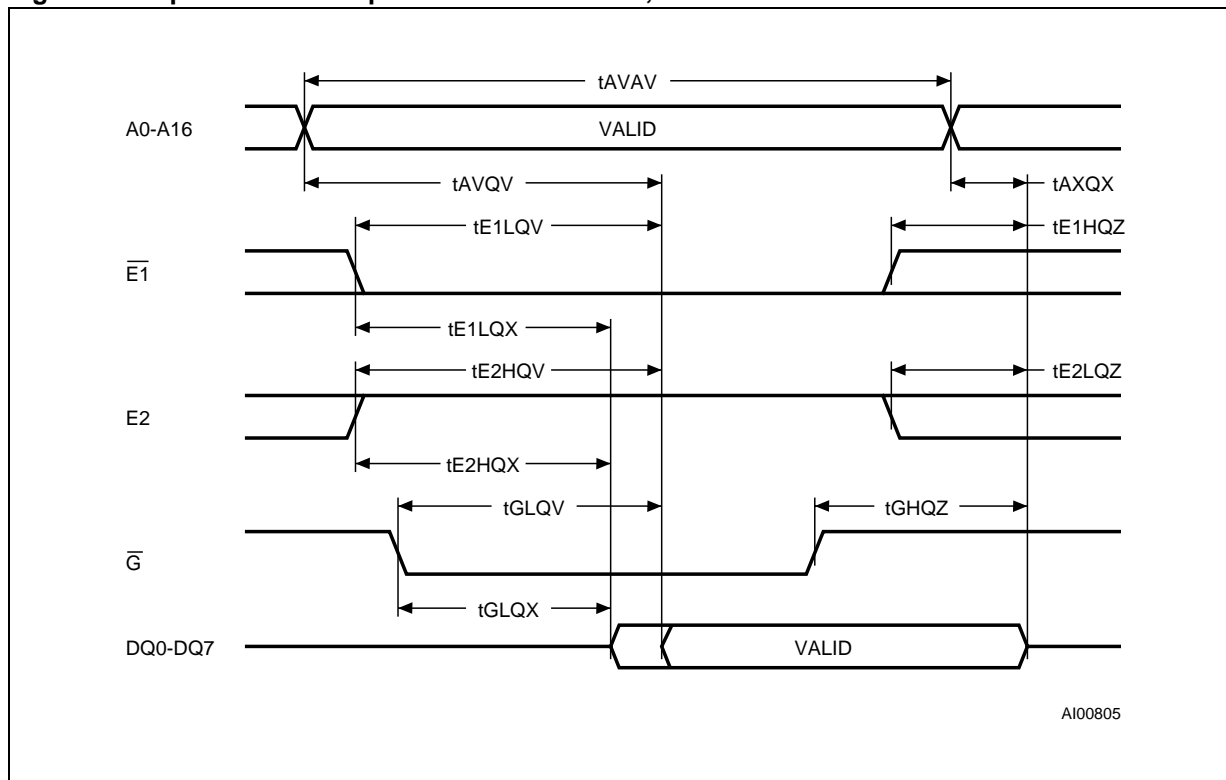
3. At any given temperature and voltage condition, $t_{E1HQZ} + t_{E2HQZ}$ is less than t_{E1LQX} and t_{E2LQX} , t_{GHQZ} is less than t_{GLQX} for any given device.

Figure 5. Address Controlled, Read Mode AC Waveforms



Note: $\bar{E}1 = \text{Low}$, $E2 = \text{High}$, $\bar{G} = \text{Low}$, $\bar{W} = \text{High}$.

Figure 6. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms.



Note: Write Enable (\overline{W}) = High.

Figure 7. Standby Mode AC Waveforms

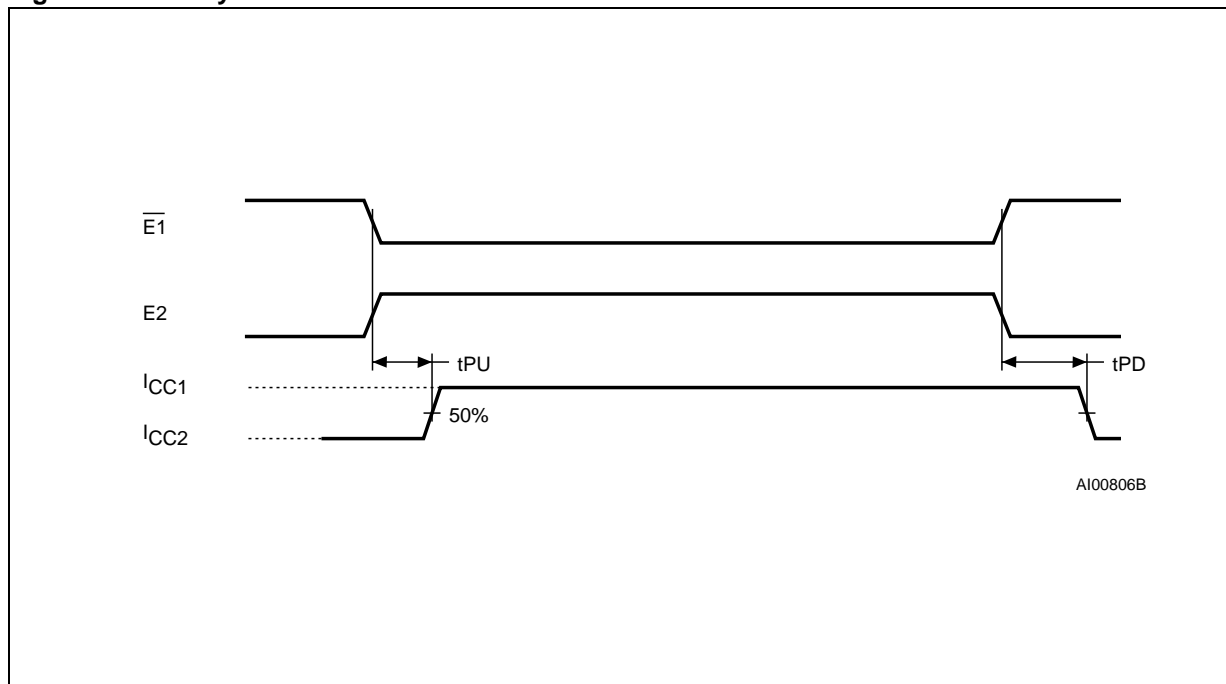


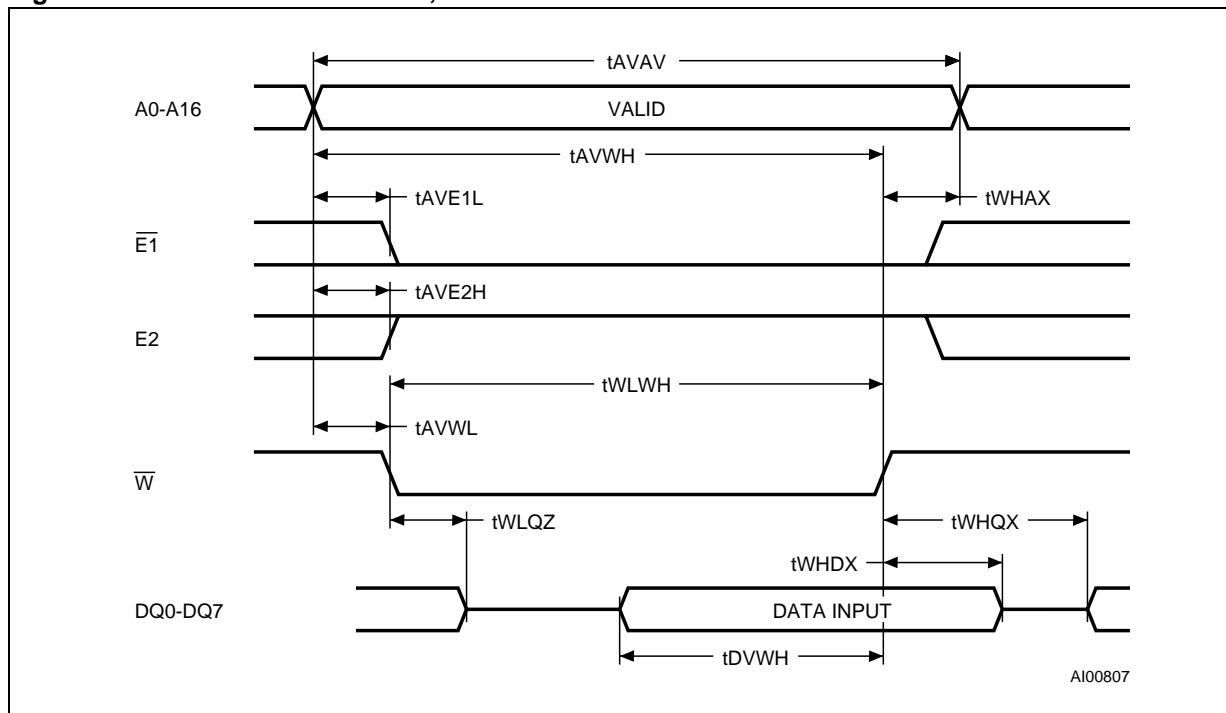
Table 8. Write Mode AC Characteristics
 ($T_A = 0$ to 70°C ; $V_{CC} = 3.0\text{V} + 0.6\text{V} / -0.3\text{V}$)

Symbol	Parameter	M68Z128W		Unit
		-70		
		Min	Max	
t_{AVAV}	Write Cycle Time	70		ns
t_{AVWL}	Address Valid to Write Enable Low	0		ns
t_{AVWH}	Address Valid to Write Enable High	60		ns
t_{AVE1H}	Address Valid to Chip Enable 1 High	60		ns
t_{AVE2L}	Address Valid to Chip Enable 2 Low	60		ns
t_{WLWH}	Write Enable Pulse Width	55		ns
t_{WHAX}	Write Enable High to Address Transition	0		ns
t_{WHDX}	Write Enable High to Input Transition	0		ns
$t_{WHQX}^{(2)}$	Write Enable High to Output Transition	0		ns
$t_{WLQZ}^{(1,2)}$	Write Enable Low to Output Hi-Z		25	ns
t_{AVE1L}	Address Valid to Chip Enable 1 Low	0		ns
t_{AVE2H}	Address Valid to Chip Enable 2 High	0		ns
t_{E1LE1H}	Chip Enable 1 Low to Chip Enable 1 High	60		ns
t_{E2HE2L}	Chip Enable 2 High to Chip Enable 2 Low	60		ns
t_{E1HAX}	Chip Enable 1 High to Address Transition	0		ns
t_{E2LAX}	Chip Enable 2 Low to Address Transition	0		ns
t_{DVWH}	Input Valid to Write Enable High	30		ns
t_{DVE1H}	Input Valid to Chip Enable 1 High	30		ns
t_{DVE2L}	Input Valid to Chip Enable 2 Low	30		ns

Note: 1. $C_L = 5\text{pF}$.

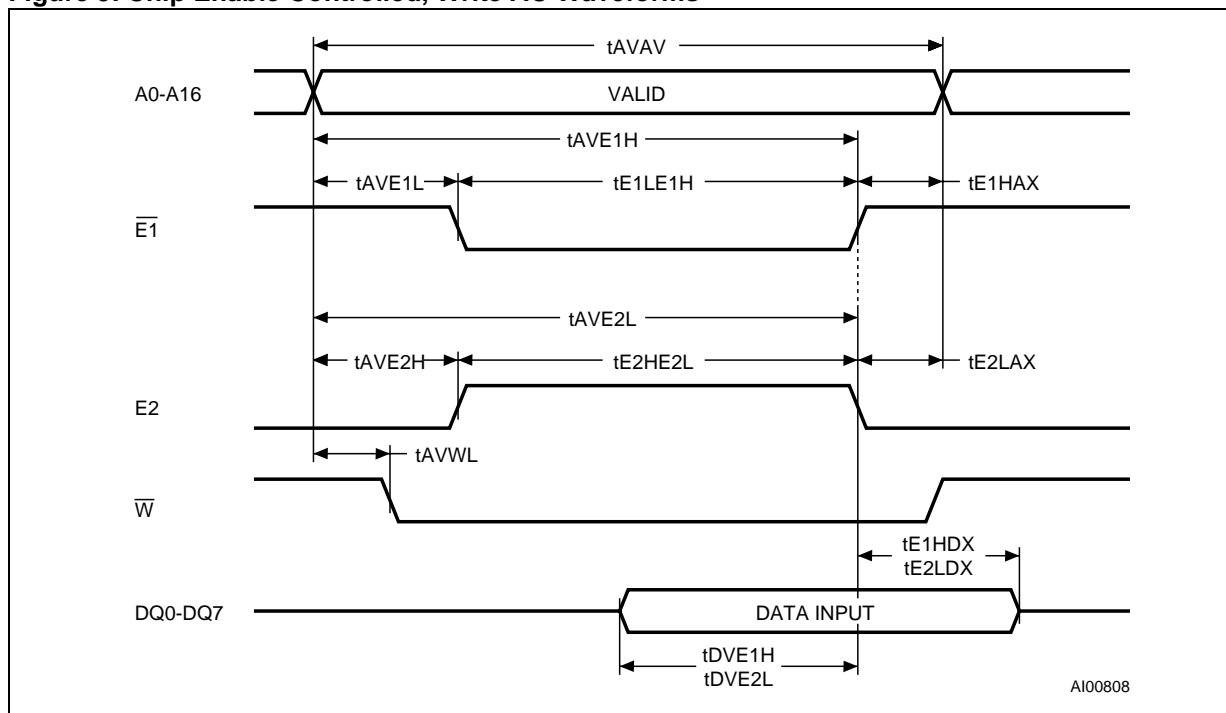
2. At any given temperature and voltage condition, t_{WHQX} is less than t_{WLQZ} for any given device.

Figure 8. Write Enable Controlled, Write AC Waveforms



Note: Output Enable (\overline{G}) = Low.

Figure 9. Chip Enable Controlled, Write AC Waveforms (1,2)



Note: 1. Output Enable (\overline{G}) = High.
 2. If $\overline{E1}$ goes High or $E2$ goes Low simultaneously with \overline{W} high, the output remains in a high-impedance state.

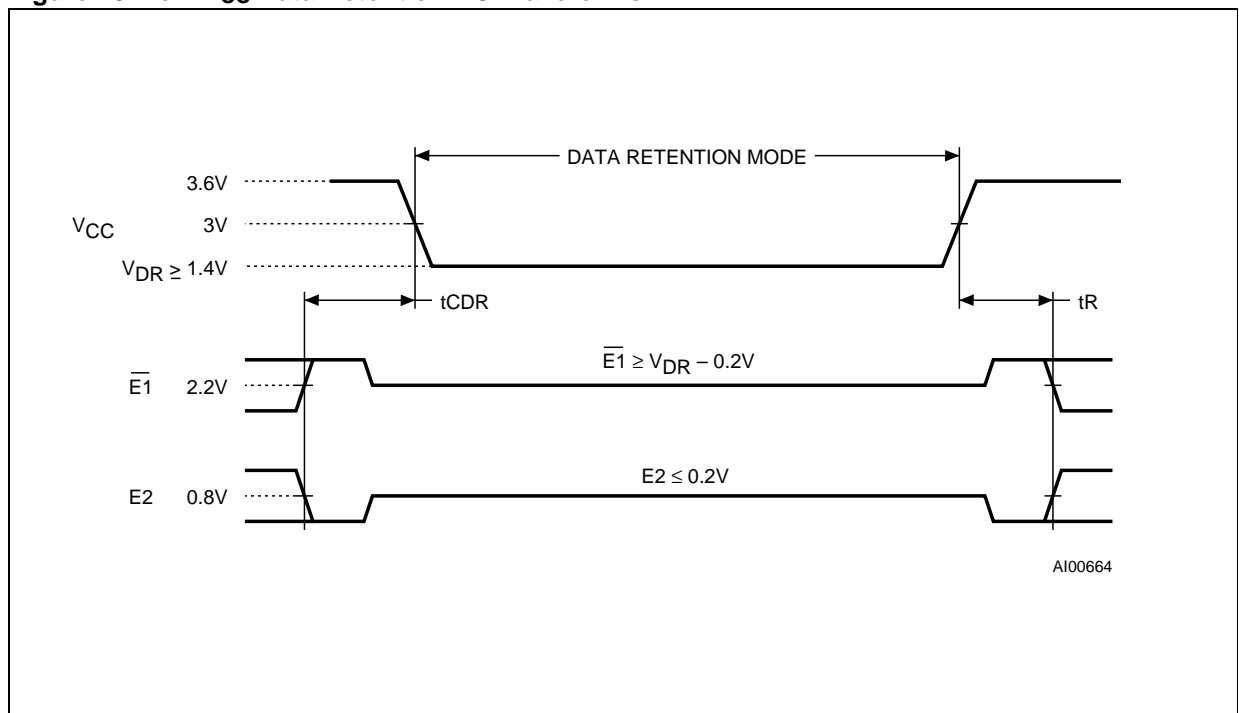
Table 9. Low V_{CC} Data Retention Characteristics
(T_A = 0 to 70°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I _{CCDR} ⁽¹⁾	Supply Current (Data Retention)	V _{CC} = 3V, $\overline{E1} \geq V_{CC} - 0.2V$, E2 ≤ 0.2V, f = 0		0.01	2	μA
V _{DR} ⁽¹⁾	Supply Voltage (Data Retention)	$\overline{E1} \geq V_{CC} - 0.2V$, E2 ≤ 0.2V, f = 0	1.4			V
t _{CDR} ^(1,2)	Chip Disable to Power Down	$\overline{E1} \geq V_{CC} - 0.2V$, E2 ≤ 0.2V, f = 0	0			ns
t _R ⁽²⁾	Operation Recovery Time		t _{AVAV}			ns

Note: 1. All other Inputs at V_{IH} ≥ V_{CC} - 0.2V or V_{IL} ≤ 0.2V.

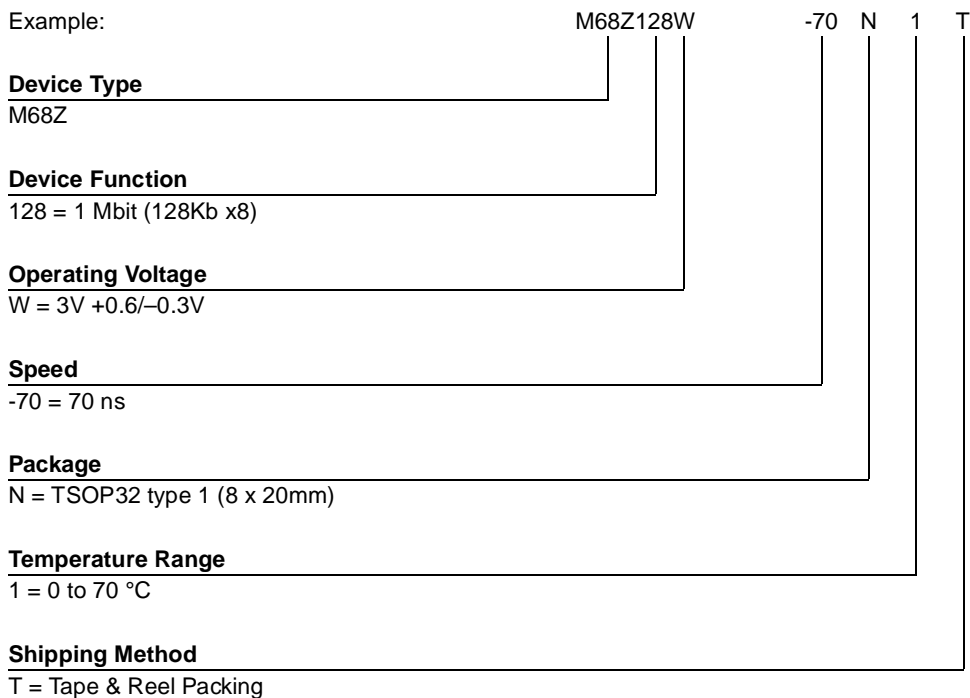
2. See Figure 10 for measurement points. Guaranteed but not tested. t_{AVAV} is Read cycle time.

Figure 10. Low V_{CC} Data Retention AC Waveforms



M68Z128W

Table 10. Ordering Information Scheme



For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

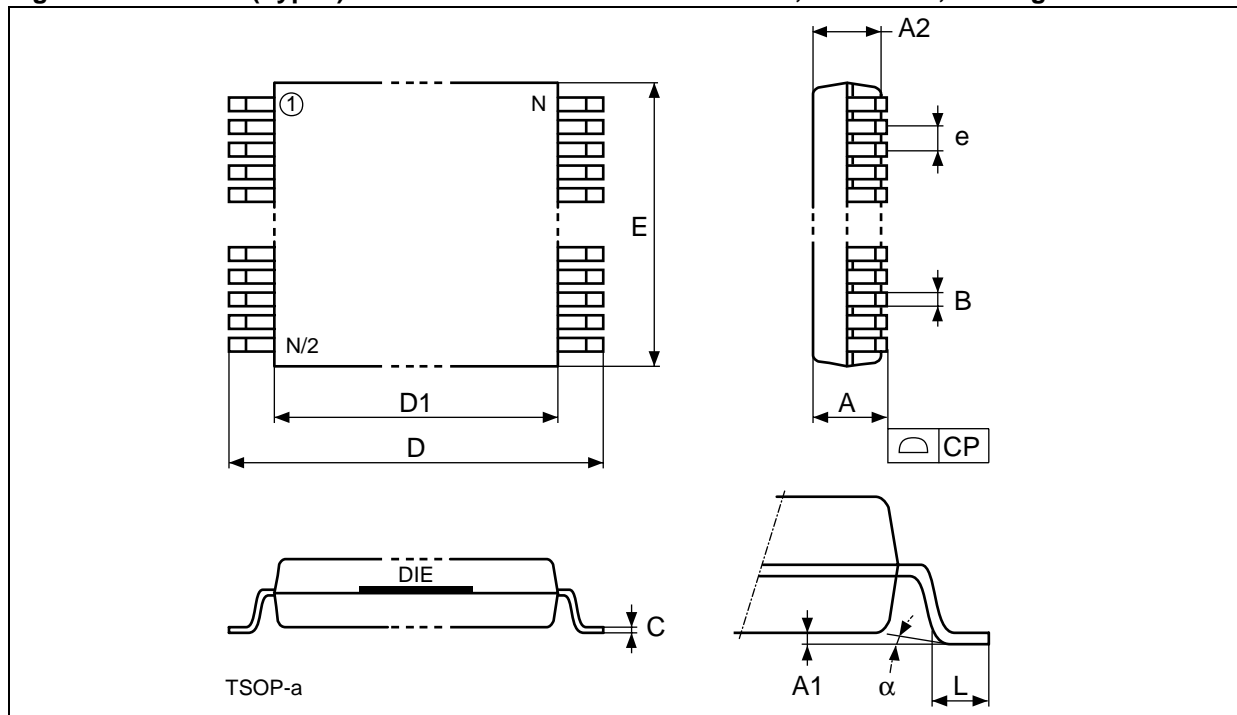
Table 11. Revision History

Date	Revision Details
November 1999	First Issue
03/20/00	TSOP32 Package Mechanical Data changed (Table 12)

Table 12. TSOP32 (Type I) - 32 lead Plastic Thin Small Outline, 8 x 20 mm, Package Mechanical Data

Symbol	mm			inch		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2		0.950	1.050		0.0374	0.0413
B		0.150	0.270		0.0059	0.0106
C		0.100	0.210		0.0039	0.0083
D		19.800	20.200		0.7795	0.7953
D1		18.300	18.500		0.7205	0.7283
e	0.500	–	–	0.0197	–	–
E		7.900	8.100		0.3110	0.3189
L		0.500	0.700		0.0197	0.0276
α		0°	5°		0°	5°
CP			0.100			0.0039
N		32			32	

Figure 11. TSOP32 (Type I) - 32 lead Plastic Thin Small Outline, 8 x 20 mm, Package Outline



Drawing is not to scale.

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