SP8401

Very Low Phase Noise 300MHz ÷10/11

Supersedes February 1992 edition

DS3230 - 3.1 April 1994

The SP8401 is a very low phase noise variable modulus divider. Special circuit techniques have been used to reduce the phase noise considerably below that produced by standard dividers. The modulus control input is CMOS or TTL compatible.

The SP8401 is packaged in a 28 pin plastic SO package to be compatible with the SP8400 and SP8402 devices.

FEATURES

- Very low Phase Noise (Typically -160dBc/Hz at 1kHz offset)
- Supply Voltage 5V

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	6.5V
Output Current	20mA
Storage Temperature Range	-55°C to +125°C
Maximum Clock Input Voltage	2.5V p-p

ORDERING INFORMATION

SP8401 KG MPES(Commercial Grade)

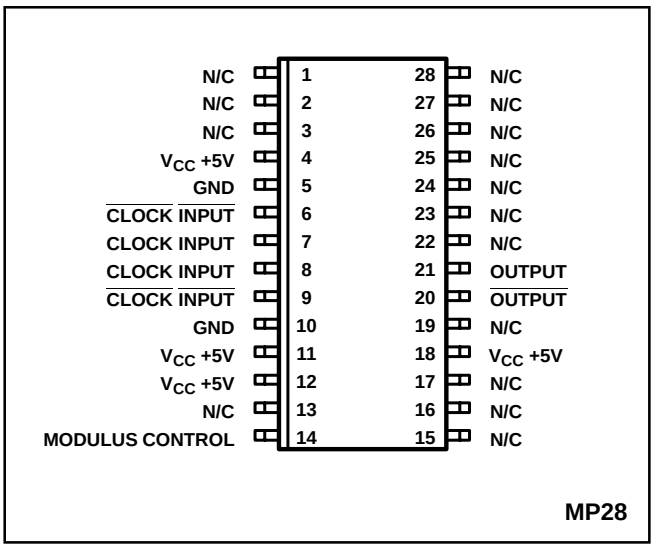


Fig.1 Pin connections - top view

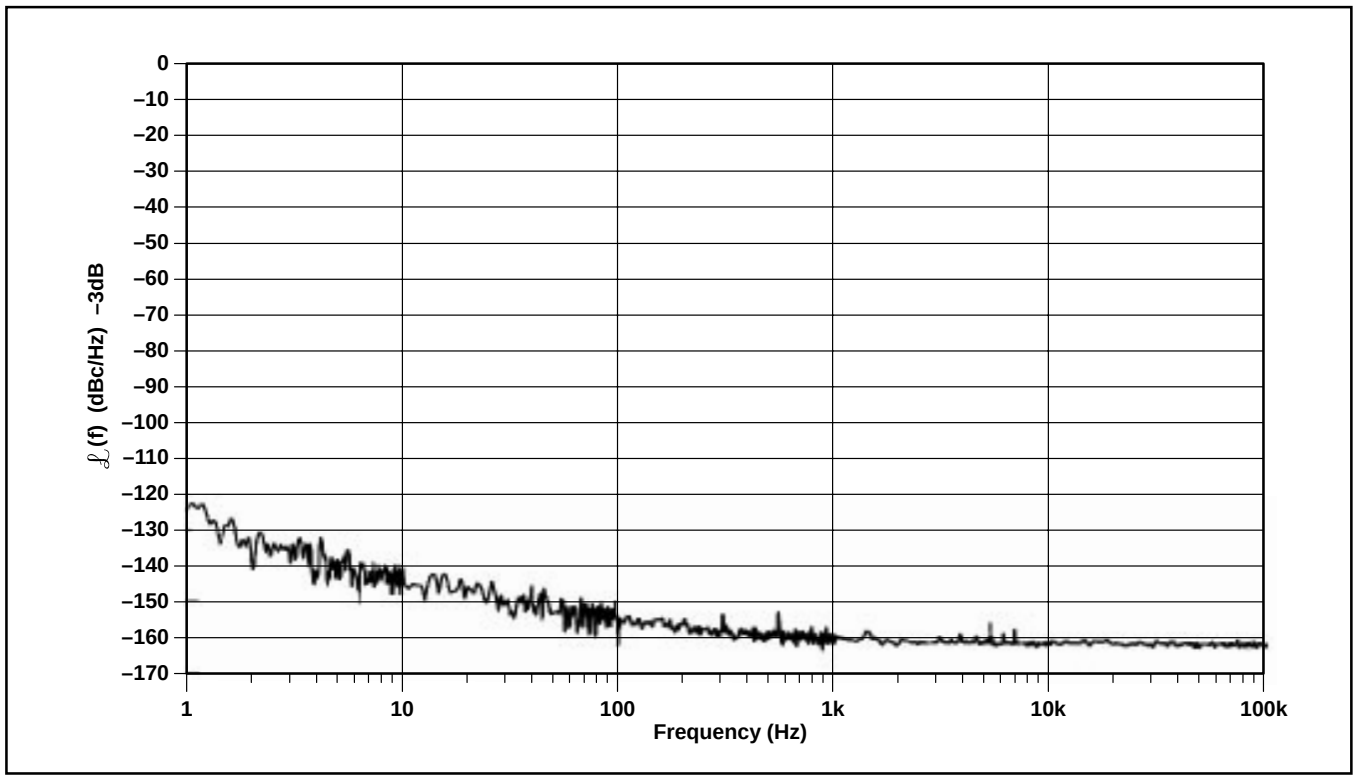


Fig.2 Typical single sideband phase noise measured at 300MHz

ELECTRICAL CHARACTERISTICS

Guaranteed over: Supply voltage V_{CC} = +4.75V to +5.25V Temperature T_{amb} = -10°C to +75°C
Tested at +4.75V and +5.25V at T_{amb} = +25°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	4, 11, 12, 18	50	57	64	mA	Output loaded with 300R See Fig.5
Output voltage swing	20, 21	340	440		mV	p-p @ 330MHz input ÷ 11 mode Output loaded with 300R
Input sensitivity 50MHz to 300MHz	7, 8			140 (-4)	mV dBm	RMS Sine wave into 50 Ohms (dBm equivalent) See Fig.3
Modulus Control Inputs						
Logic high voltage	14	2.2			V	÷ 10 mode
Low low voltage	14			0.8		÷ 11 mode
Input current	14			180	µA	Modulus control input voltage 5V
Set up time t_s	14		4		ns	
Release time t_r	14		4		ns	

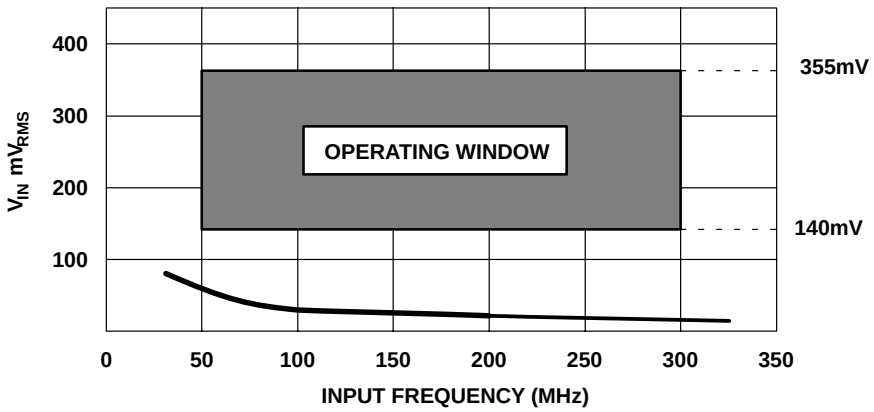


Fig.3 Typical input sensitivity

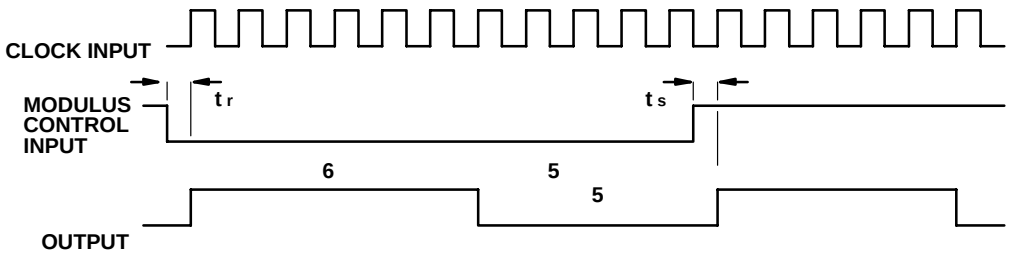


Fig.4 Timing diagram

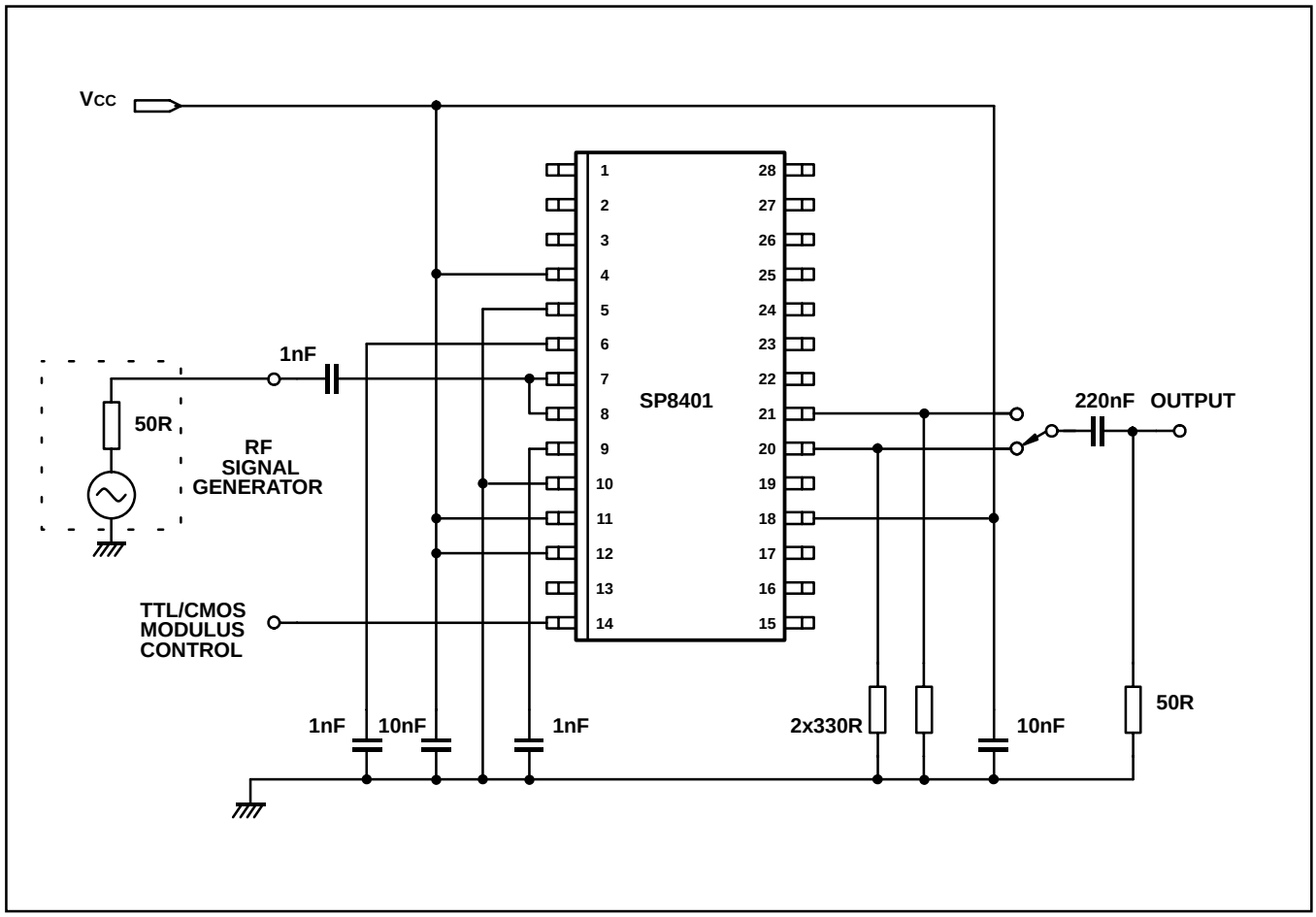
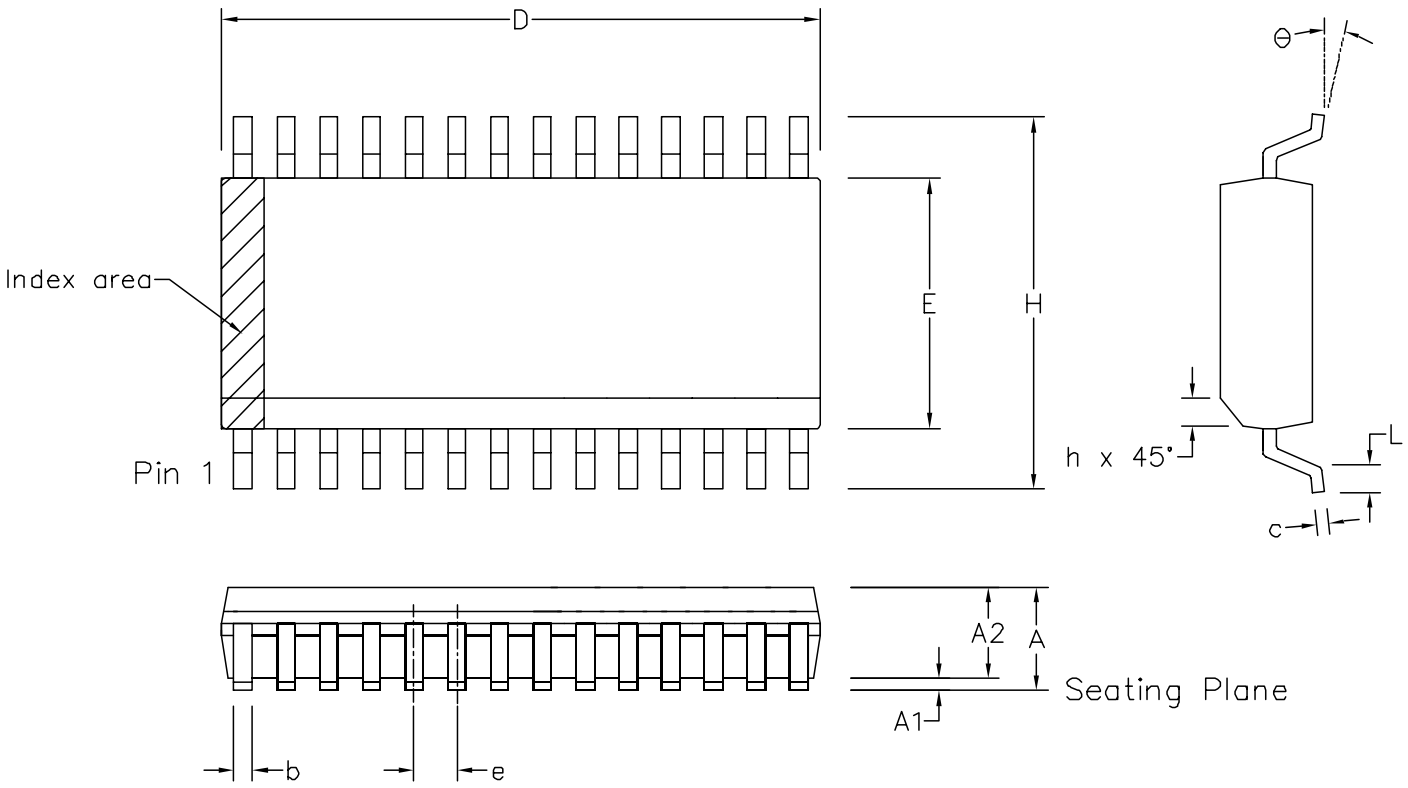


Fig.4 Test circuit



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	2.35		2.65		0.093		0.104
A1	0.10		0.30		0.004		0.012
A2	2.25		2.35		0.089		0.092
D	17.70		18.10		0.697		0.713
H	10.00		10.65		0.394		0.419
E	7.40		7.60		0.291		0.299
L	0.40		1.27		0.016		0.050
e	1.27 BSC.				0.050 BSC.		
b	0.33		0.51		0.013		0.020
c	0.23		0.32		0.009		0.013
Θ	0°		8°		0°		8°
h	0.25		0.75		0.010		0.029
	Pin features						
N	28						
Conforms to JEDEC MS-013AE Iss. C							

Notes:
1. The chamfer on the body is optional. If it not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion/intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

ORIGINATING SITE: SWINDON

ISSUE	1	2				MITEL SEMICONDUCTOR
ACN	006746	201943				
DATE	7APR95	27FEB97				
APPROVED						

Title: Package Outline Drawing for 28 lds SOIC(W)-0.300" Body Width (MP)

Drawing Number
GPD00017

http://www.mitelsemi.com

World Headquarters - Canada
Tel: +1 (613) 592 2122
Fax: +1 (613) 592 6909

North America
Tel: +1 (770) 486 0194
Fax: +1 (770) 631 8213

Asia/Pacific
Tel: +65 333 6193
Fax: +65 333 6192

Europe, Middle East, and Africa (EMEA)
Tel: +44 (0) 1793 518528
Fax: +44 (0) 1793 518581