

# DATA SHEET

## **TDA1519C**

**22 W BTL or 2 × 11 W  
stereo power amplifier**

Product specification  
Supersedes data of 2000 Mar 08  
File under Integrated Circuits, IC01

2001 Aug 24

## 22 W BTL or 2 × 11 W stereo power amplifier

## TDA1519C

### FEATURES

- Requires very few external components for Bridge-Tied Load (BTL) operation
- Stereo or BTL application
- High output power
- Low offset voltage at output (important for BTL applications)
- Fixed gain
- Good ripple rejection
- Mute/standby switch
- Load dump protection
- AC and DC short-circuit safe to ground and  $V_P$
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs ( $V_P = 0$  V)
- No switch-on/switch-off plops
- Protected against electrostatic discharge
- Low thermal resistance
- Identical inputs (inverting and non-inverting)
- Pin compatible with TDA1519B (TDA1519C and TDA1519CSP).

### GENERAL DESCRIPTION

The TDA1519C is an integrated class-B dual output amplifier in a 9-lead plastic single in-line power package or 20-lead heatsink small outline package.

For the TDA1519CTH (SOT418-2), the heatsink is positioned on top of the package, which allows an external heatsink to be mounted on top. The heatsink of the TDA1519CTD (SOT397-1) is facing the PCB, allowing the heatsink to be soldered onto the copper area of the PCB.

### ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1519C	SIL9P	plastic single in-line power package; 9 leads	SOT131-2
TDA1519CSP	SMS9P	plastic surface mounted single in-line power package; 9 leads	SOT354-1
TDA1519CTD	HSOP20	plastic, heatsink small outline package; 20 leads	SOT397-1
TDA1519CTH	HSOP20	plastic, heatsink small outline package; 20 leads; low stand-off height	SOT418-2

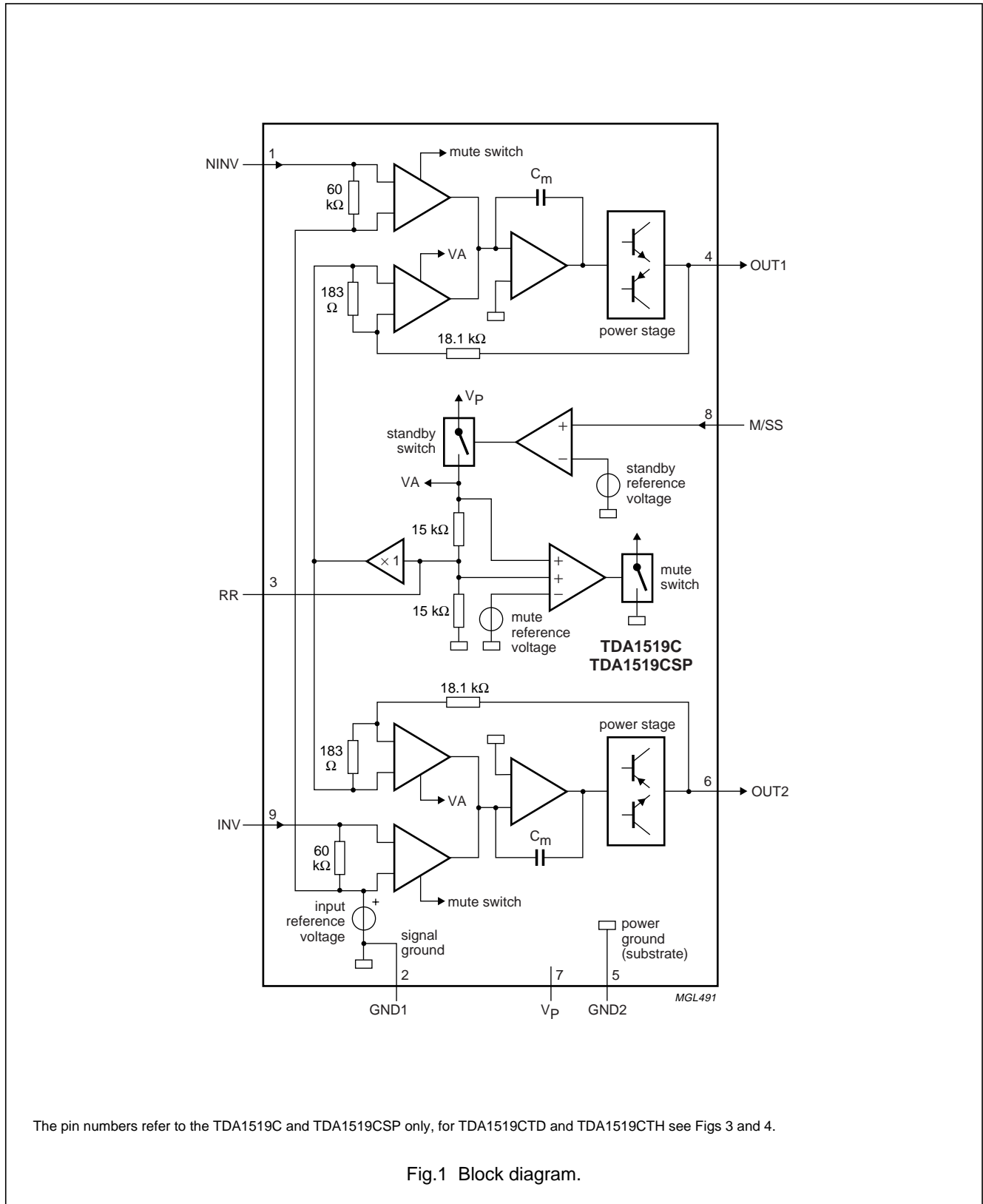
**22 W BTL or 2 × 11 W  
stereo power amplifier**
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**QUICK REFERENCE DATA**

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supply</b>						
$V_P$	supply voltage	operating	6.0	14.4	17.5	V
		non-operating	–	–	30	V
		load dump protected	–	–	45	V
$I_{ORM}$	repetitive peak output current		–	–	4	A
$I_{q(tot)}$	total quiescent current		–	40	80	mA
$I_{stb}$	standby current		–	0.1	100	$\mu$ A
$I_{sw(on)}$	switch-on current		–	–	40	$\mu$ A
<b>Inputs</b>						
$ Z_i $	input impedance	BTL	25	–	–	k $\Omega$
		stereo	50	–	–	k $\Omega$
<b>Stereo application</b>						
$P_o$	output power	THD = 10%	–	6	–	W
		$R_L = 4 \Omega$	–	11	–	W
		$R_L = 2 \Omega$	–	–	–	–
$\alpha_{cs}$	channel separation		40	–	–	dB
$V_{n(o)(rms)}$	noise output voltage (RMS value)		–	150	–	$\mu$ V
<b>BTL application</b>						
$P_o$	output power	THD = 10%; $R_L = 4 \Omega$	–	22	–	W
SVRR	supply voltage ripple rejection	$R_S = 0 \Omega$	–	–	–	–
		$f_i = 100 \text{ Hz}$	34	–	–	dB
		$f_i = 1 \text{ to } 10 \text{ kHz}$	48	–	–	dB
$ \Delta V_{OO} $	DC output offset voltage		–	–	250	mV
$T_j$	junction temperature		–	–	150	$^{\circ}$ C

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BLOCK DIAGRAM



The pin numbers refer to the TDA1519C and TDA1519CSP only, for TDA1519CTD and TDA1519CTH see Figs 3 and 4.

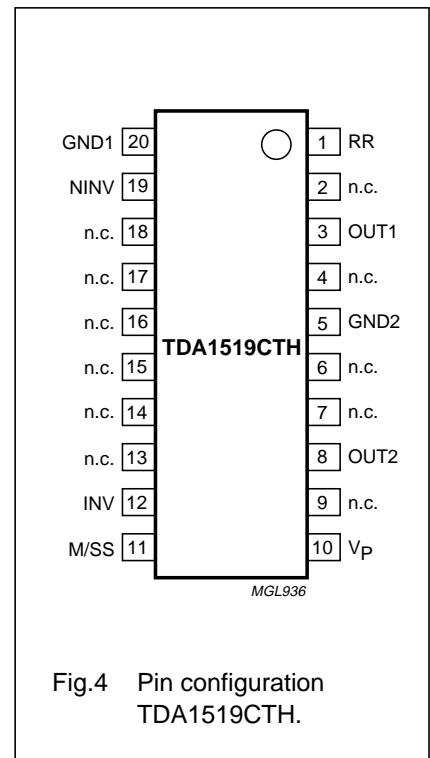
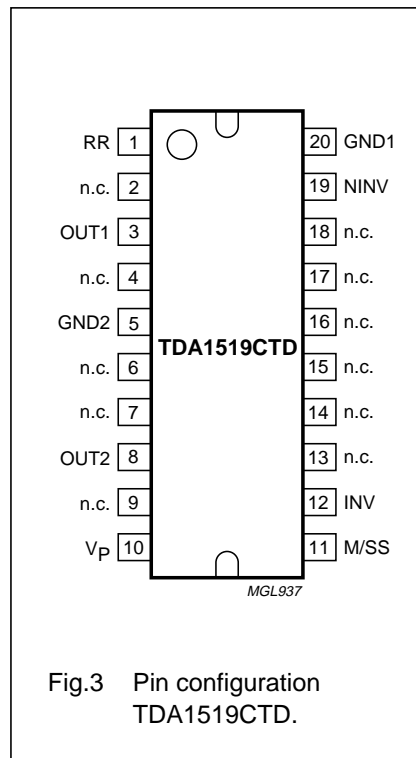
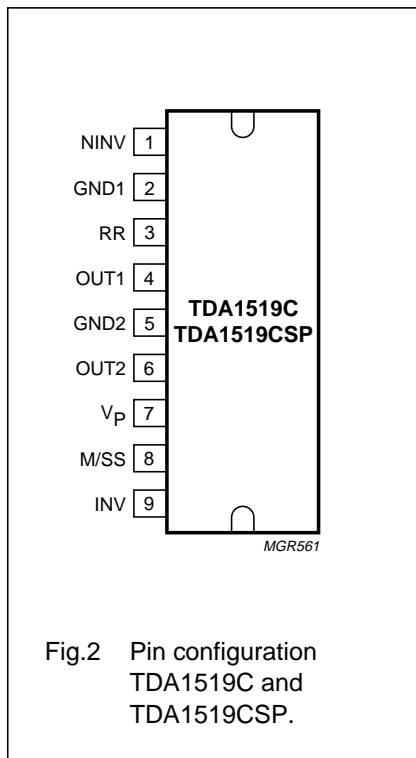
Fig.1 Block diagram.

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PINNING

SYMBOL	PIN			DESCRIPTION
	TDA1519C; TDA1519CSP	TDA1519CTD	TDA1519CTH	
NINV	1	19	19	non-inverting input
GND1	2	20	20	ground 1 (signal)
RR	3	1	1	supply voltage ripple rejection
OUT1	4	3	3	output 1
GND2	5	5	5	ground 2 (substrate)
OUT2	6	8	8	output 2
V <sub>P</sub>	7	10	10	positive supply voltage
M/SS	8	11	11	mute/standby switch input
INV	9	12	12	inverting input
n.c.	–	2, 4, 6, 7, 9 and 13 to 18	2, 4, 6, 7, 9 and 13 to 18	not connected



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**FUNCTIONAL DESCRIPTION**

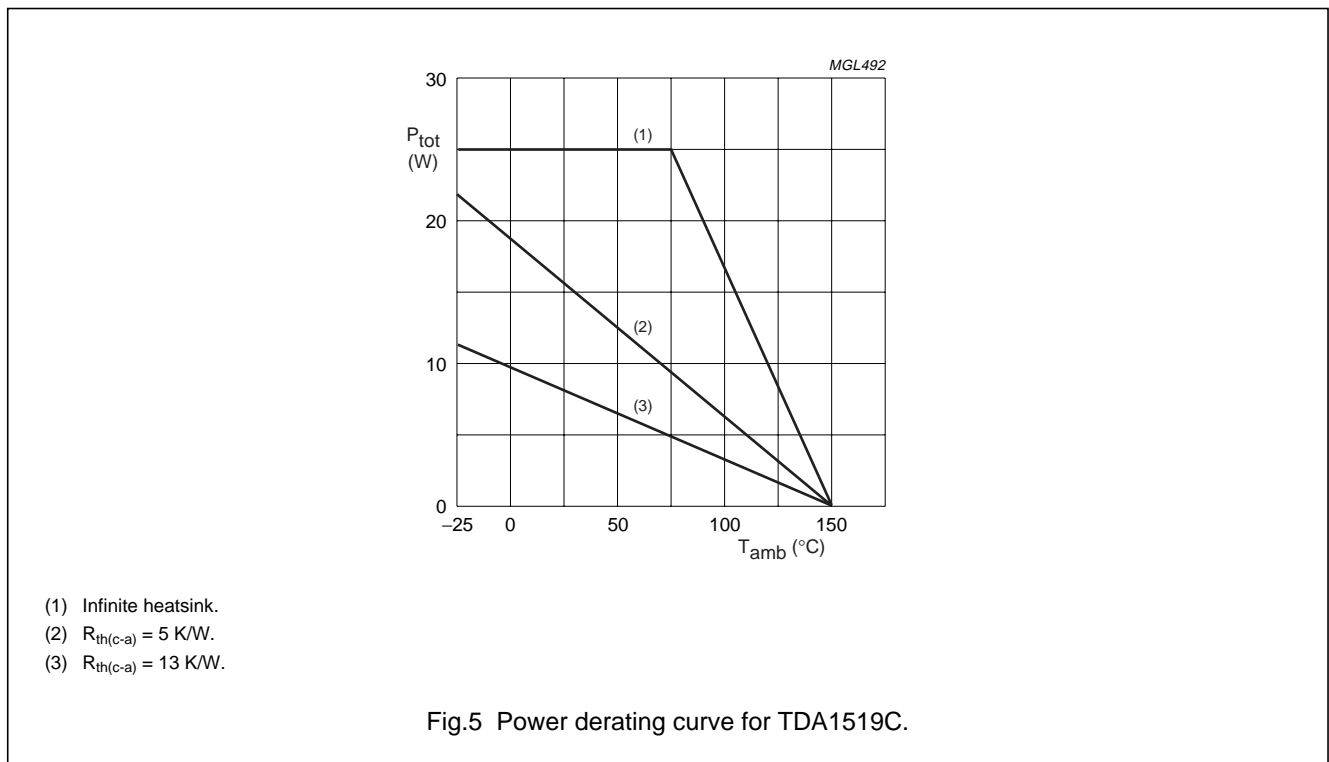
The TDA1519C contains two identical amplifiers with differential input stages. The gain of each amplifier is fixed at 40 dB. A special feature of this device is the mute/standby switch which has the following features:

- Low standby current (<100 µA)
- Low mute/standby switching current (allows for low-cost supply switch)
- Mute condition.

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>P</sub>	supply voltage	operating	–	17.5	V
		non-operating	–	30	V
		load dump protected; during 50 ms; t <sub>r</sub> ≥ 2.5 ms	–	45	V
V <sub>sc</sub>	AC and DC short-circuit-safe voltage		–	17.5	V
V <sub>rp</sub>	reverse polarity voltage		–	6	V
E <sub>o</sub>	energy handling capability at outputs	V <sub>P</sub> = 0 V	–	200	mJ
I <sub>OSM</sub>	non-repetitive peak output current		–	6	A
I <sub>ORM</sub>	repetitive peak output current		–	4	A
P <sub>tot</sub>	total power dissipation	see Fig.5	–	25	W
T <sub>j</sub>	junction temperature		–	150	°C
T <sub>stg</sub>	storage temperature		–55	+150	°C



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### THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient; TDA1519C, TDA1519CTH and TDA1519CTD	in free air	40	K/W
$R_{th(j-c)}$	thermal resistance from junction to case; TDA1519C, TDA1519CTH and TDA1519CTD		3	K/W

### DC CHARACTERISTICS

$V_P = 14.4$  V;  $T_{amb} = 25$  °C; measured in circuit of Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supply</b>						
$V_P$	supply voltage	note 1	6.0	14.4	17.5	V
$I_{q(tot)}$	total quiescent current		–	40	80	mA
$V_O$	DC output voltage	note 2	–	6.95	–	V
$ \Delta V_{OO} $	DC output offset voltage		–	–	250	mV
<b>Mute/standby switch</b>						
$V_{sw(on)}$	switch-on voltage level		8.5	–	–	V
$V_{mute}$	mute voltage level		3.3	–	6.4	V
$V_{stb}$	standby voltage level		0	–	2	V
<b>Mute/standby condition</b>						
$V_o$	output voltage	mute mode; $V_i = 1$ V (maximum); $f_i = 20$ Hz to 15 kHz	–	–	20	mV
$ \Delta V_{OO} $	DC output offset voltage	mute mode	–	–	250	mV
$I_{stb}$	standby current	standby mode	–	–	100	μA
$I_{sw(on)}$	switch-on current		–	12	40	μA

### Notes

- The circuit is DC adjusted at  $V_P = 6$  to 17.5 V and AC operating at  $V_P = 8.5$  to 17.5 V.
- At  $V_P = 17.5$  to 30 V, the DC output voltage is  $\leq 0.5V_P$ .

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### AC CHARACTERISTICS

$V_P = 14.4\text{ V}$ ;  $R_L = 4\ \Omega$ ;  $f = 1\text{ kHz}$ ;  $T_{\text{amb}} = 25\text{ °C}$ ; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Stereo application</b> (see Fig.6)						
$P_o$	output power	note 1				
		THD = 0.5%	4	5	–	W
		THD = 10%	5.5	6.0	–	W
		$R_L = 2\ \Omega$ ; note 1				
		THD = 0.5%	7.5	8.5	–	W
		THD = 10%	10	11	–	W
THD	total harmonic distortion	$P_o = 1\text{ W}$	–	0.1	–	%
$f_{ro(l)}$	low frequency roll-off	–3 dB; note 2	–	45	–	Hz
$f_{ro(h)}$	high frequency roll-off	–1 dB	20	–	–	kHz
$G_{V(cl)}$	closed-loop voltage gain		39	40	41	dB
SVRR	supply voltage ripple rejection	on; notes 3 and 4	40	–	–	dB
		on; notes 3 and 5	45	–	–	dB
		mute; notes 3 and 6	45	–	–	dB
		standby; notes 3 and 6	80	–	–	dB
$ Z_i $	input impedance		50	60	75	k $\Omega$
$V_{n(o)(rms)}$	noise output voltage (RMS value)	note 7				
		on; $R_S = 0\ \Omega$	–	150	–	$\mu\text{V}$
		on; $R_S = 10\text{ k}\Omega$	–	250	500	$\mu\text{V}$
		mute; note 8	–	120	–	$\mu\text{V}$
$\alpha_{cs}$	channel separation	$R_S = 10\text{ k}\Omega$	40	–	–	dB
$ \Delta G_{V(ub)} $	channel unbalance		–	0.1	1	dB
<b>BTL application</b> (see Fig.7)						
$P_o$	output power	note 1				
		THD = 0.5%	15	17	–	W
		THD = 10%	20	22	–	W
		$V_P = 13.2\text{ V}$ ; note 1				
		THD = 0.5%	–	13	–	W
		THD = 10%	–	17.5	–	W
THD	total harmonic distortion	$P_o = 1\text{ W}$	–	0.1	–	%
$B_p$	power bandwidth	THD = 0.5%; $P_o = -1\text{ dB}$ ; with respect to 15 W	–	35 to 15000	–	Hz
$f_{ro(l)}$	low frequency roll-off	–1 dB; note 2	–	45	–	Hz
$f_{ro(h)}$	high frequency roll-off	–1 dB	20	–	–	kHz
$G_{V(cl)}$	closed-loop voltage gain		45	46	47	dB



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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SVRR	supply voltage ripple rejection	on; notes 3 and 4	34	–	–	dB
		on; notes 3 and 5	48	–	–	dB
		mute; notes 3 and 6	48	–	–	dB
		standby; notes 3 and 6	80	–	–	dB
$ Z_i $	input impedance		25	30	38	k $\Omega$
$V_{n(o)(rms)}$	noise output voltage (RMS value)	note 7				
		on; $R_S = 0 \Omega$	–	200	–	$\mu V$
		on; $R_S = 10 k\Omega$	–	350	700	$\mu V$
		mute; note 8	–	180	–	$\mu V$

**Notes**

- Output power is measured directly at the output pins of the device.
- Frequency response externally fixed.
- Ripple rejection measured at the output with a source impedance of 0  $\Omega$  (maximum ripple amplitude of 2 V).
- Frequency  $f = 100$  Hz.
- Frequency between 1 and 10 kHz.
- Frequency between 100 Hz and 10 kHz.
- Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
- Noise output voltage independent of  $R_S$  ( $V_i = 0$  V).

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APPLICATION INFORMATION

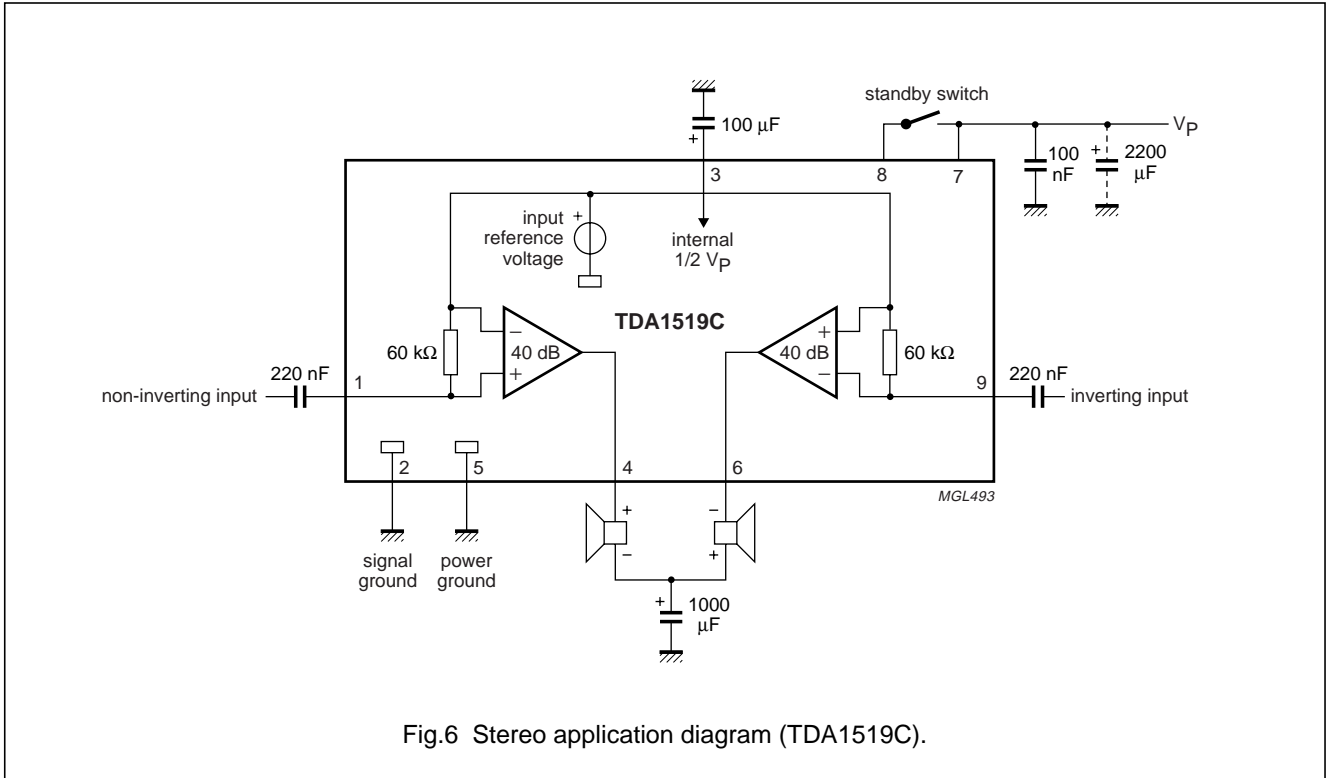


Fig.6 Stereo application diagram (TDA1519C).

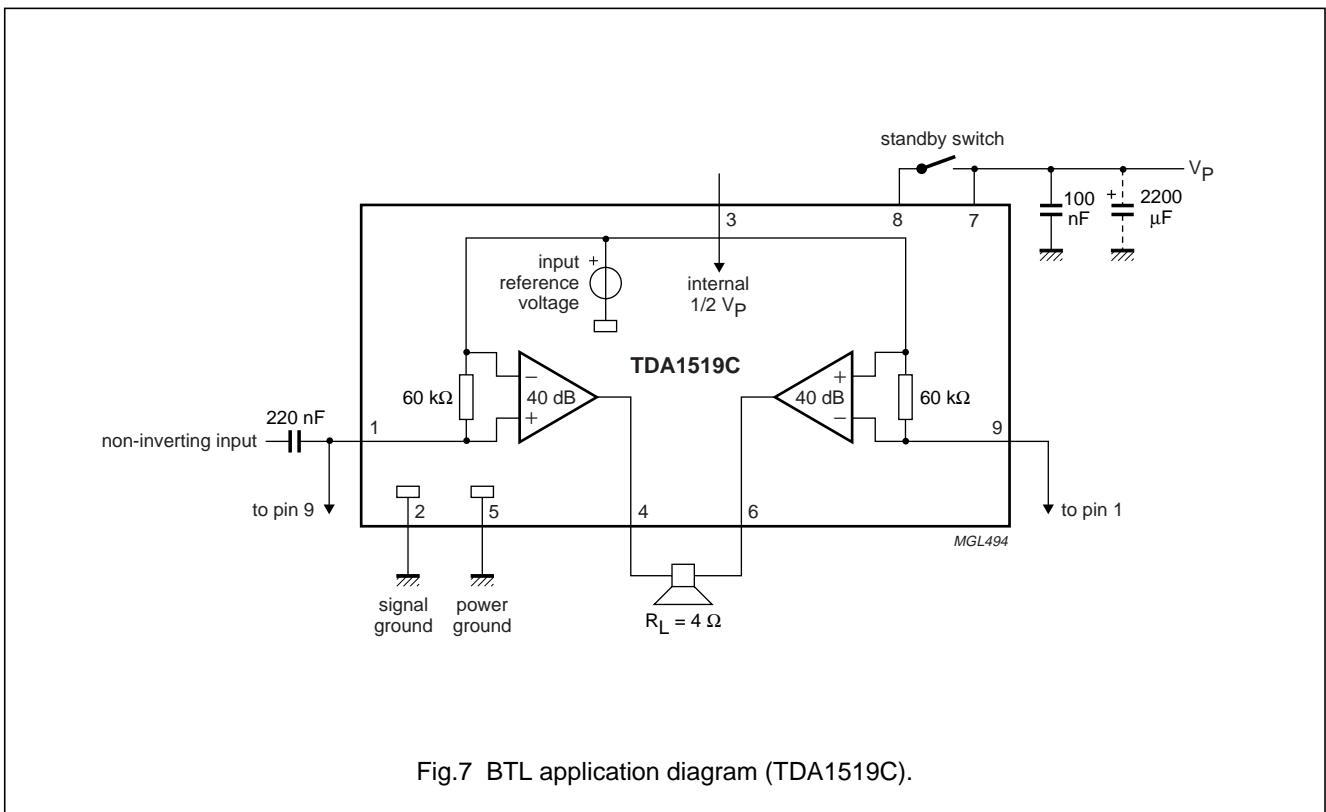


Fig.7 BTL application diagram (TDA1519C).

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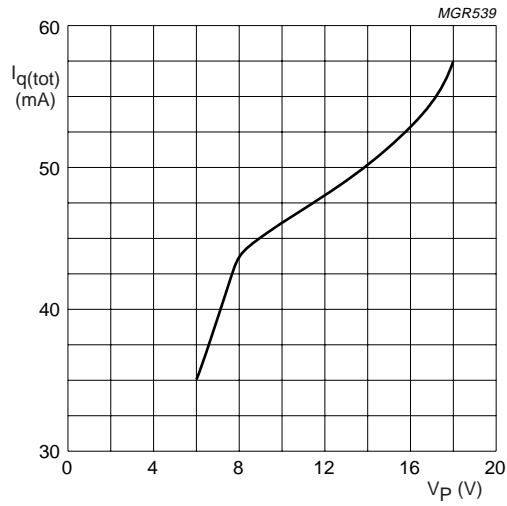
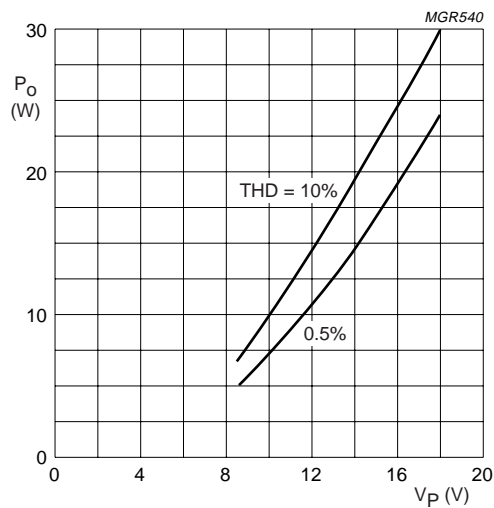


Fig.8 Total quiescent current as a function of the supply voltage.

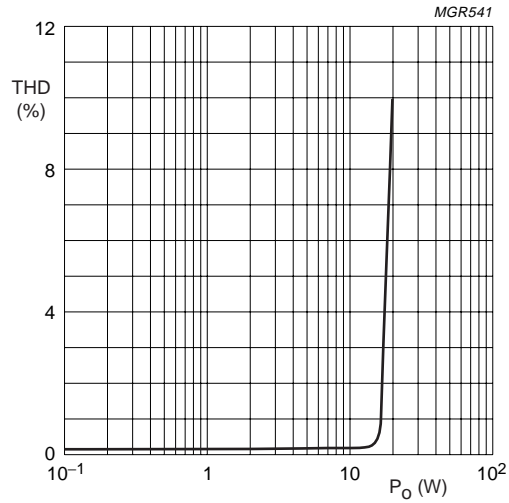


BTL application.  
 $R_L = 4 \Omega$ .  
 $f_i = 1 \text{ kHz}$ .

Fig.9 Output power as a function of the supply voltage.

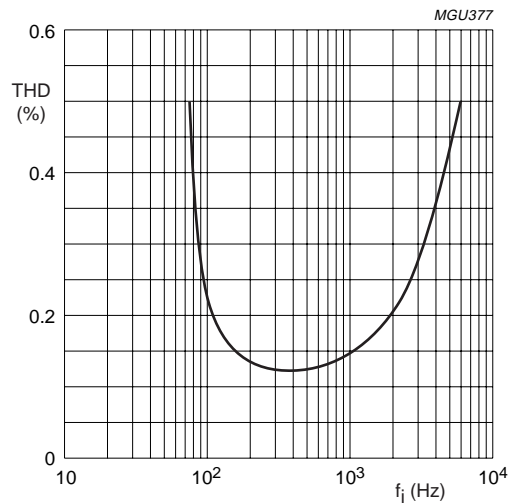
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BTL application.  
RL = 4 Ω.  
fi = 1 kHz.

Fig.10 Total harmonic distortion as a function of the output power.



BTL application.  
RL = 4 Ω.  
Po = 1 W.

Fig.11 Total harmonic distortion as a function of the operating frequency.

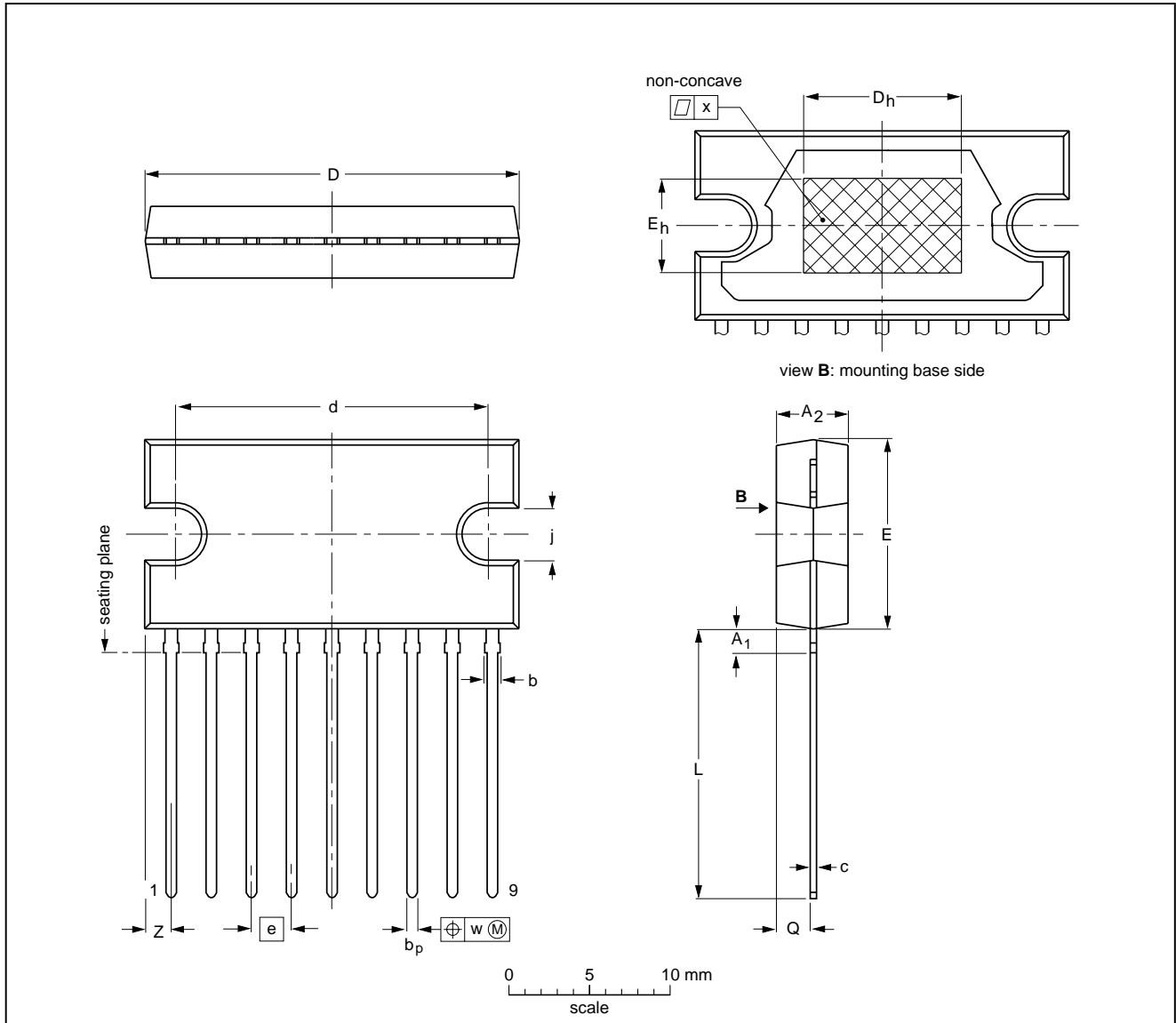
22 W BTL or 2 × 11 W  
stereo power amplifier

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PACKAGE OUTLINES

SIL9P: plastic single in-line power package; 9 leads

SOT131-2



DIMENSIONS (mm are the original dimensions)

UNIT	A <sub>1</sub> max.	A <sub>2</sub>	b max.	b <sub>p</sub>	c	D <sup>(1)</sup>	d	D <sub>h</sub>	E <sup>(1)</sup>	e	E <sub>h</sub>	j	L	Q	w	x	z <sup>(1)</sup>
mm	2.0	4.6 4.4	1.1	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	6	3.4 3.1	17.2 16.5	2.1 1.8	0.25	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

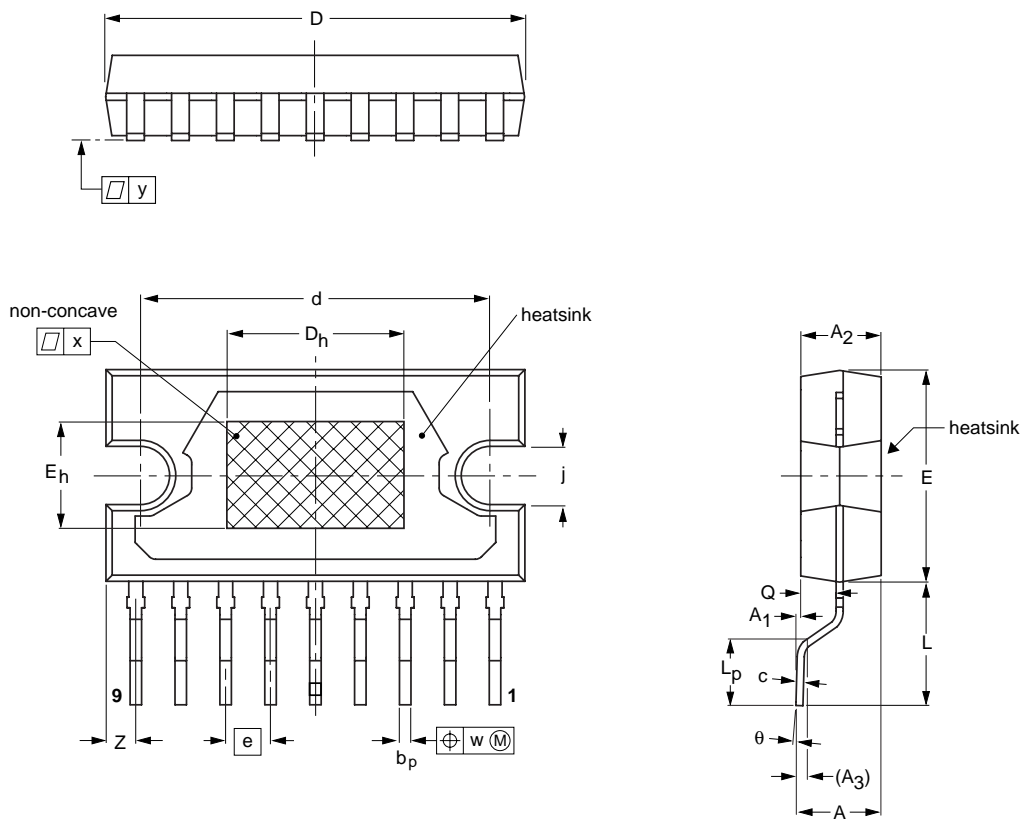
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT131-2						95-03-11 99-12-17

22 W BTL or 2 × 11 W  
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SMS9P: plastic surface mounted single in-line power package; 9 leads

SOT354-1



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	d	D <sub>h</sub>	E <sup>(1)</sup>	e	E <sub>h</sub>	j	L	L <sub>p</sub>	Q	w	x	y	Z <sup>(1)</sup>	θ
mm	4.9 4.2	0.35 0.05	4.6 4.4	0.25	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	6	3.4 3.1	7.4 6.6	3.4 2.8	2.1 1.9	0.25	0.03	0.15	2.00 1.45	3° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

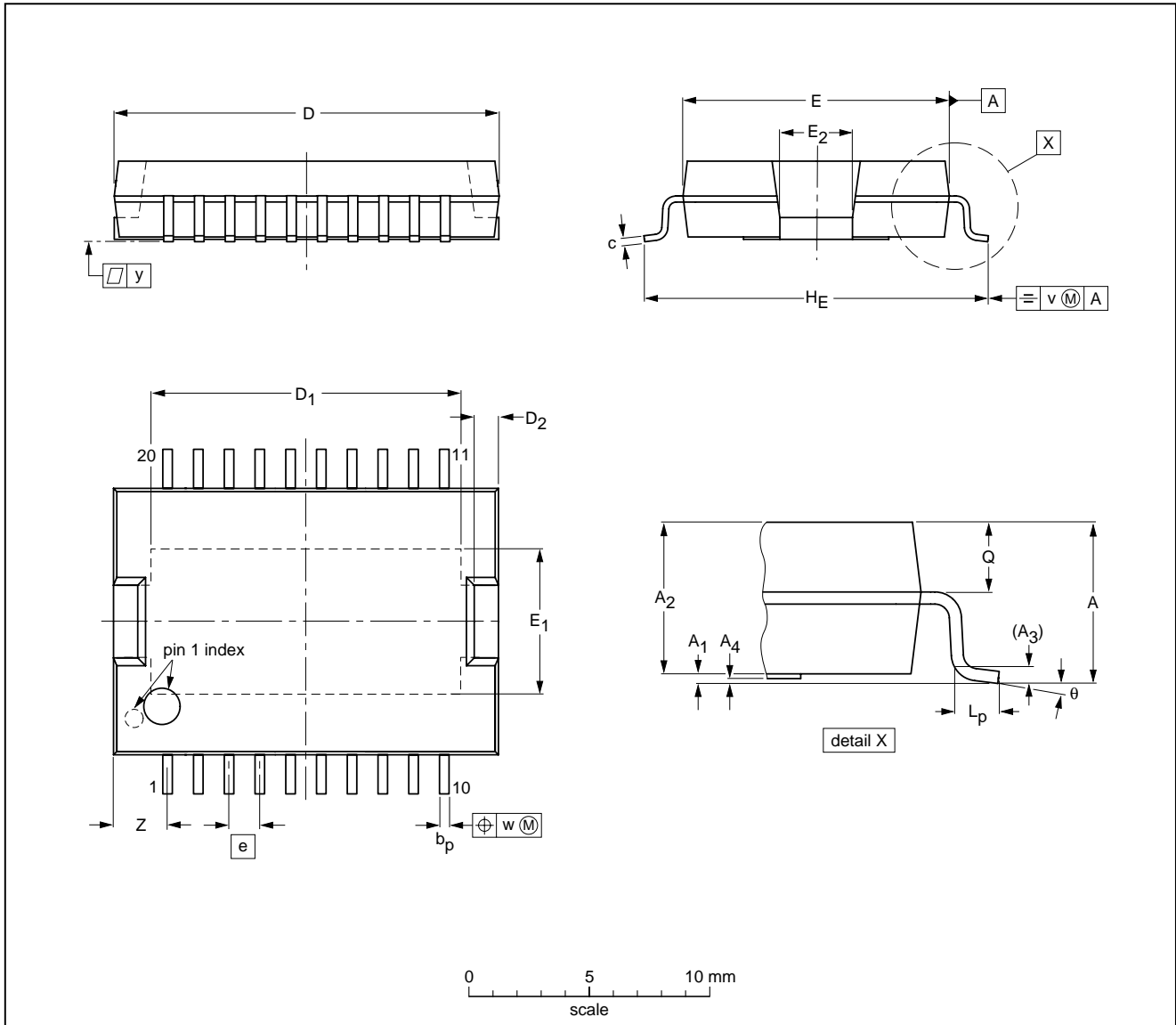
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	IEC	JEDEC	EIAJ			
SOT354-1						98-10-08 99-12-17

22 W BTL or 2 × 11 W  
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HSOP20: plastic, heatsink small outline package; 20 leads

SOT397-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	A <sub>4</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	D <sub>1</sub>	D <sub>2</sub>	E <sup>(1)</sup>	E <sub>1</sub>	E <sub>2</sub>	e	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y	Z	θ
mm	3.6	0.3 0.1	3.3 3.0	0.35	0.1 0	0.53 0.40	0.32 0.23	16.0 15.8	13.0 12.6	1.1 0.9	11.1 10.9	6.2 5.8	2.9 2.5	1.27	14.5 13.9	1.1 0.8	1.5 1.4	0.25	0.25	0.1	2.5 2.0	8° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

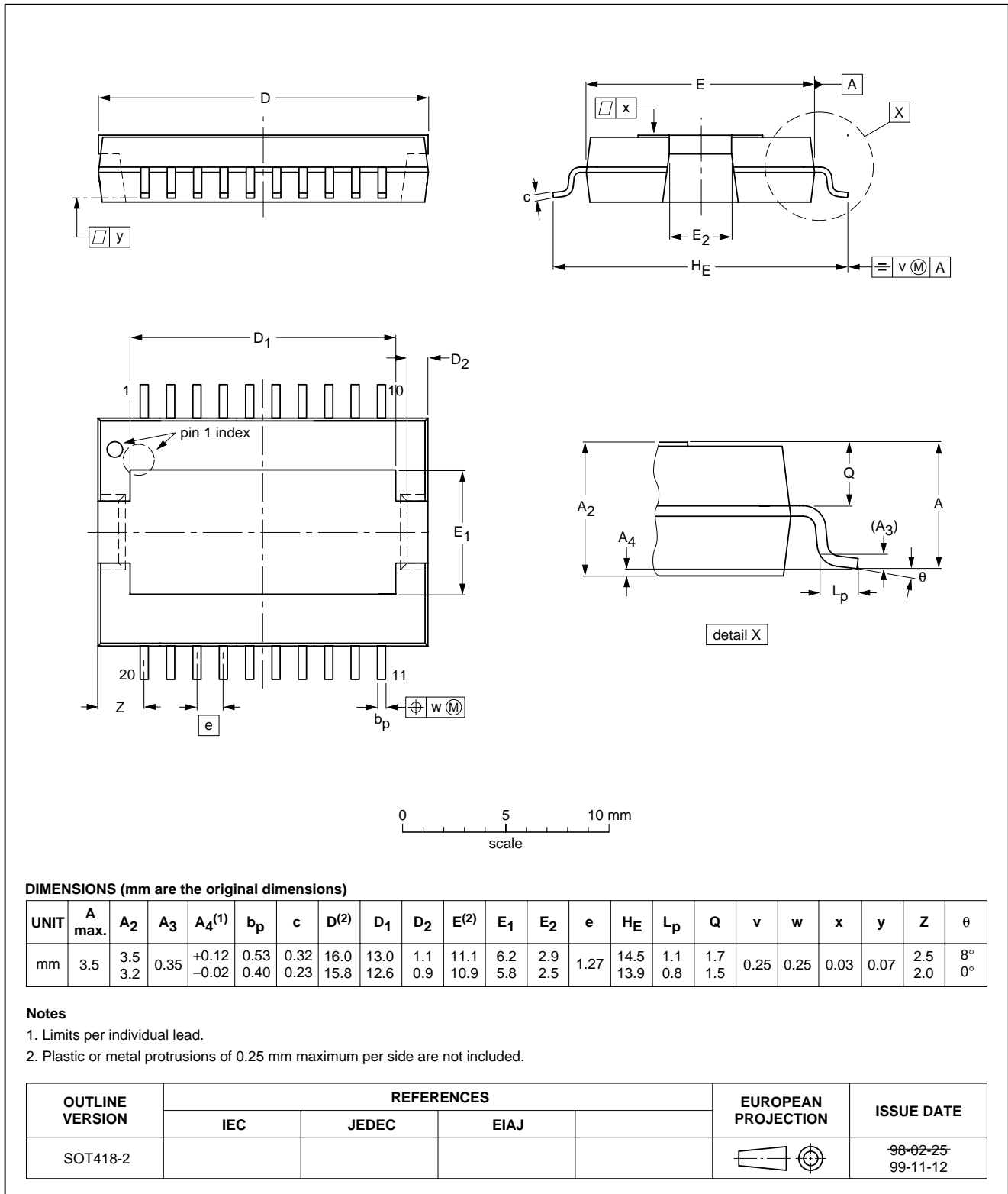
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT397-1						97-11-03 99-11-12

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HSOP20: plastic, heatsink small outline package; 20 leads; low stand-off height

SOT418-2





## 22 W BTL or 2 × 11 W stereo power amplifier

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### SOLDERING

#### Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

#### Through-hole mount packages

##### SOLDERING BY DIPPING OR BY SOLDER WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg(max)}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

##### MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

#### Surface mount packages

##### REFLOW SOLDERING

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

##### WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

##### MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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TDA1519C

### Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE	SOLDERING METHOD		
		WAVE	REFLOW <sup>(1)</sup>	DIPPING
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable <sup>(2)</sup>	–	suitable
Surface mount	BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable	–
	HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable <sup>(3)</sup>	suitable	–
	PLCC <sup>(4)</sup> , SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended <sup>(4)(5)</sup>	suitable	–
	SSOP, TSSOP, VSO	not recommended <sup>(6)</sup>	suitable	–

### Notes

- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the “*Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*”.
- For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
- These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

## 22 W BTL or 2 × 11 W stereo power amplifier

TDA1519C

### DATA SHEET STATUS

DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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### Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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