Data Sheet | December 1998 | File Number 535.5

2MHz, Micropower Operational Amplifier

The CA3078 and CA3078A are high gain monolithic operational amplifiers which can deliver milliamperes of current yet only consume microwatts of standby power. Their operating points are externally adjustable and frequency compensation may be accomplished with one external capacitor. The CA3078 and CA3078A provide the designer with the opportunity to tailor the frequency response and improve the slew rate without sacrificing power. Operation with a single 1.5V battery is a practical reality with these devices.

The CA3078A is a premium device having a supply voltage range of V± = 0.75V to V± = 15V. The CA3078 has the same lower supply voltage limit but the upper limit is V+ = +6V and V- = -6V.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
CA3078AE	-55 to 125	8 Ld PDIP	E8.3
CA3078AM (3078A)	-55 to 125	8 Ld SOIC	M8.15
CA3078AM96 (3078A)	-55 to 125	8 Ld SOIC Tape and Reel	M8.15
CA3078AT	-55 to 125	8 Pin Metal Can	T8.C
CA3078E	0 to 70	8 Ld PDIP	E8.3
CA3078M (3078)	0 to 70	8 Ld SOIC	M8.15
CA3078T	0 to 70	8 Pin Metal Can	T8.C

Features

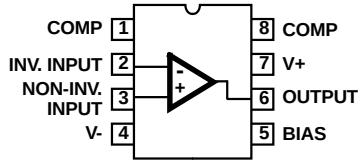
- Low Standby Power . . . . . As Low As 700nW
- Wide Supply Voltage Range. . . . . ±0.75V to ±15V
- High Peak Output Current . . . . . 6.5mA (Min)
- Adjustable Quiescent Current
- Output Short Circuit Protection

Applications

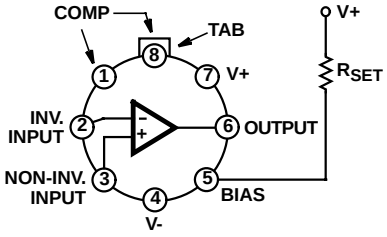
- Portable Electronics
- Telemetry
- Medical Electronics
- Intrusion Alarms
- Instrumentation

Pinouts

CA3078 (PDIP, SOIC)
TOP VIEW

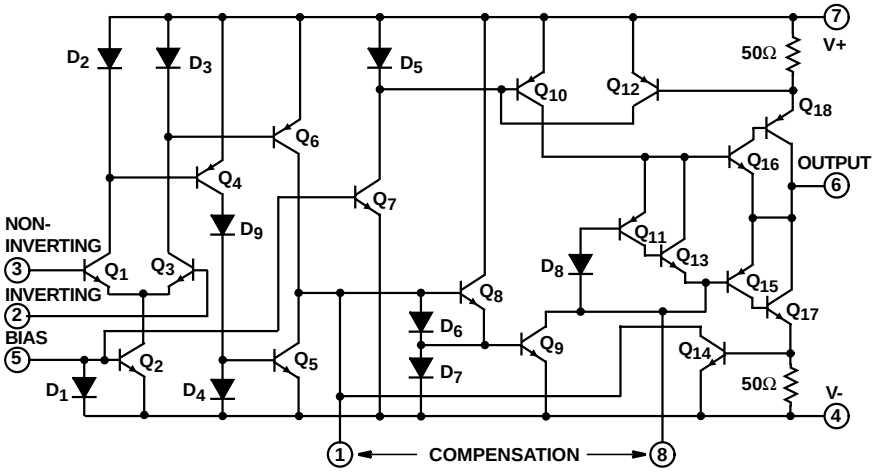


CA3078 (METAL CAN)
TOP VIEW



NOTE: Case Voltage = Floating

Schematic Diagram



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminal)
- CA3078 . . . . . .14V
- CA3078A 36V

Differential Input Voltage 6V
Input Voltage . . . . . V+ to V-
Input Current 0.1mA
Output Short Circuit Duration (Note 1). . . . . No Limitation

Operating Conditions

Temperature Range
- CA3078 . . . . . 0^oC to 70^oC
- CA3078A . . . . . -55^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
PDIP Package	130	N/A
SOIC Package	165	N/A
Metal Can Package	175	100

Maximum Junction Temperature (Metal Can Package). . . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range. . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Short circuit may be applied to ground or to either supply.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications For Equipment Design

PARAMETER	TEST CONDITIONS			CA3078 LIMITS					CA3078A LIMITS					UNITS
				R_{SET} = 1MΩ					R_{SET} = 5.1MΩ					
				T_A = 25°C			T_A = 0°C to 70°C		T_A = 25°C			T_A = -55°C to 125°C		
	V+ and V-	R_S (kΩ)	R_L (kΩ)	MIN	TYP	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IO}	±6V	≤10	-	-	1.3	4.5	-	5	-	0.70	3.5	-	4.5	mV
I_{IO}		-	-	-	6	32	-	40	-	0.50	2.5	-	5.0	nA
I_{IB}		-	-	-	60	170	-	200	-	7	12	-	50	nA
A_{OL}		-	≥10	88	92	-	86	-	92	100	-	90	-	dB
I_Q		-	-	-	100	130	-	150	-	20	25	-	45	µA
P_D		-	-	-	1200	1560	-	1800	-	240	300	-	540	µW
V_{OM}		-	≥10	±5.1	±5.3	-	±5	-	±5.1	±5.3	-	±5	-	V
V_{ICR}		≤10	-	-	-5.5 to +5.8	-	-5 to +5	-	-	-5.5 to +5.8	-	-5 to +5	-	V
CMRR		≤10	-	80	110	-	-	-	80	115	-	-	-	dB
$I_{OM}+$ or $I_{OM}-$		-	-	-	12	-	6.5	30	-	12	-	6.5	30	mA
$\Delta V_{IO}/\Delta V+$		≤10	-	76	93	-	-	-	76	105	-	-	-	µV/V
$\Delta V_{IO}/\Delta V-$		≤10	-	76	93	-	-	-	76	105	-	-	-	µV/V
									R_{SET} = 13MΩ					
V_{IO}	±15V	≤10	-	-	-	-	-	-	-	1.4	3.5	-	4.5	mV
A_{OL}		-	≥10	-	-	-	-	-	92	100	-	88	-	dB
I_Q		-	-	-	-	-	-	-	-	20	30	-	50	µA
P_D		-	-	-	-	-	-	-	-	600	750	-	1350	µW
V_{OM}		-	≥10	-	-	-	-	-	±13.7	±14.1	-	±13.5	-	V
CMRR		≤10	-	-	-	-	-	-	80	106	-	-	-	dB
I_{IB}		-	-	-	-	-	-	-	-	7	14	-	55	nA
I_{IO}		-	-	-	-	-	-	-	-	0.50	2.7	-	5.5	nA

Electrical Specifications $T_A = 25^oC$, Typical Values Intended Only for Design Guidance

PARAMETER	CA3078		CA3078A		UNITS
	V+ = +1.3V, V- = -1.3V R_{SET} = 2MΩ	V+ = +0.75V, V- = -0.75V R_{SET} = 10MΩ	V+ = +1.3V, V- = -1.3V R_{SET} = 2MΩ	V+ = +0.75V, V- = -0.75V R_{SET} = 10MΩ	
V_{IO}	1.3	1.5	0.7	0.9	mV
I_{IO}	1.7	0.5	0.3	0.054	nA
I_{IB}	9	1.3	3.7	0.45	nA
A_{OL}	80	60	84	65	dB
I_Q	10	1	10	1	µA
P_D	26	1.5	26	1.5	µW
V_{OP-P}	1.4	0.3	1.4	0.3	V
V_{ICR}	-0.8 to +1.1	-0.2 to +0.5	-0.8 to +1.1	-0.2 to +0.5	V
CMRR	100	90	100	90	dB
$I_{OM}\pm$	12	0.5	12	0.5	mA
$\Delta V_{IO}/\Delta V\pm$	20	50	20	50	µV/V

Electrical Specifications $T_A = 25^oC$ and $V_{SUPPLY} = \pm 6V$, Typical Values Intended Only for Design Guidance

PARAMETER	TEST CONDITIONS	CA3078	CA3078A		UNITS
		R_{SET} = 1MΩ	R_{SET} = 5.1MΩ	R_{SET} = 1MΩ	
$\Delta V_{IO}/\Delta T_A$	$R_S \leq 10k\Omega$	6	5	6	$\mu V/^oC$
$\Delta I_{IO}/\Delta T_A$	$R_S \leq 10k\Omega$	70	6.3	70	$pA/^oC$
GBWP	A_V = 100, C_1 = 10pF	2	0.3	2	MHz
SR	See Figures 23, 24	0.04	0.027	0.04	V/µs
		1.5	0.5	1.5	V/µs
t_R	10% to 90% Rise Time	2.5	3	2.5	µs
R_I	-	0.87	7.4	1.7	MΩ
R_O	-	0.8	1	0.8	kΩ
e_N(10Hz)	R_S = 0	25	40	-	$nV/\sqrt{Hz}$
i_N(10Hz)	R_S = 1MΩ	1	0.25	-	$pA/\sqrt{Hz}$

Test Circuits

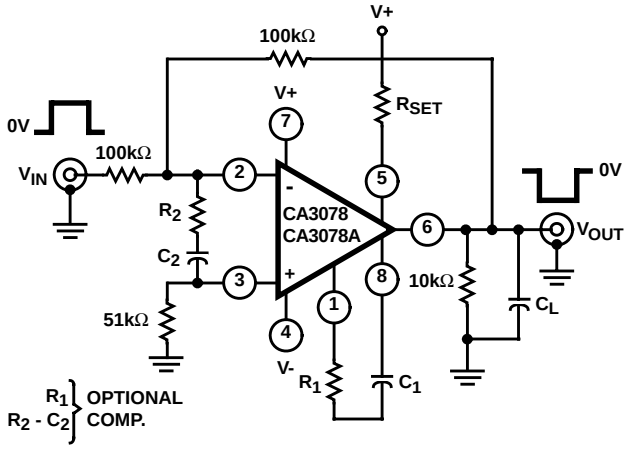


FIGURE 1. TRANSIENT RESPONSE AND SLEW RATE, UNITY GAIN (INVERTING) TEST CIRCUIT

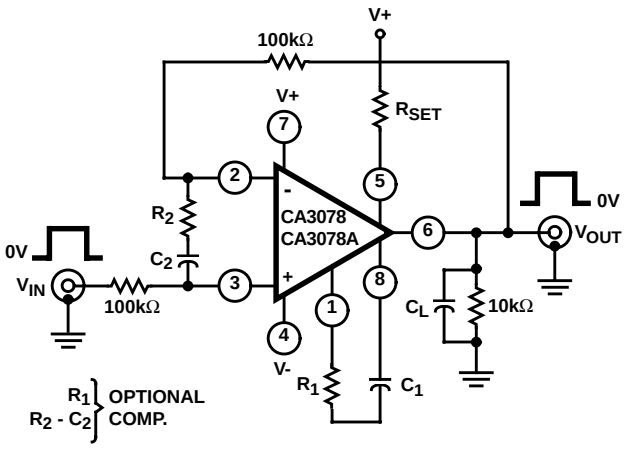
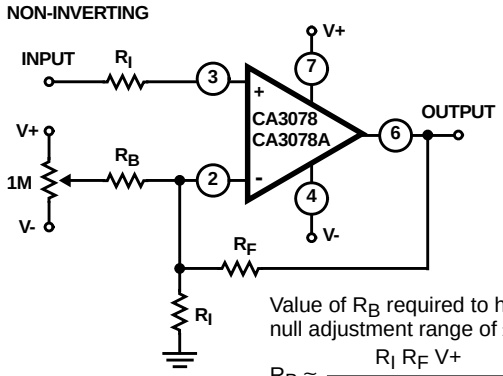


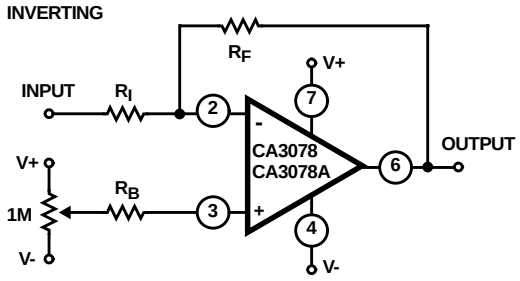
FIGURE 2. SLEW RATE, UNITY GAIN (NON-INVERTING) TEST CIRCUIT



Value of R_B required to have a null adjustment range of ±7.5mV

$$R_B \approx \frac{R_I R_F V+}{(R_I + R_F)\ 7.5 \times 10^{-3}}$$

assuming $R_B >> \frac{R_I R_F}{R_I + R_F}$



Value of R_B required to have a null adjustment range of ±7.5mV

$$R_B \approx \frac{R_I V+}{7.5 \times 10^{-3}}$$

assuming $R_B >> R_I$

FIGURE 3. OFFSET VOLTAGE NULL CIRCUITS

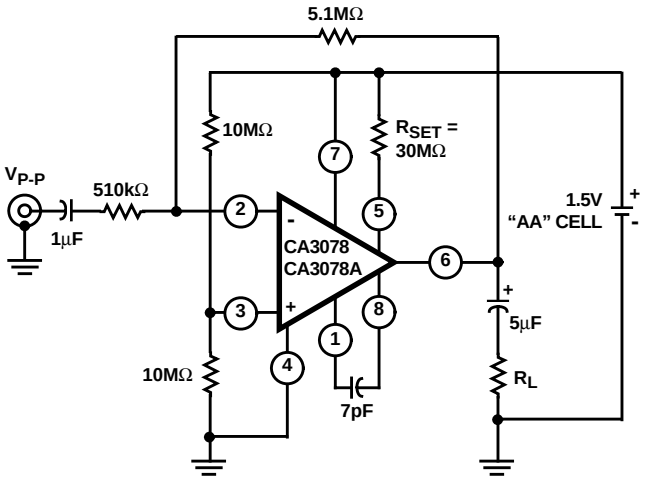


FIGURE 4. INVERTING 20dB AMPLIFIER CIRCUIT

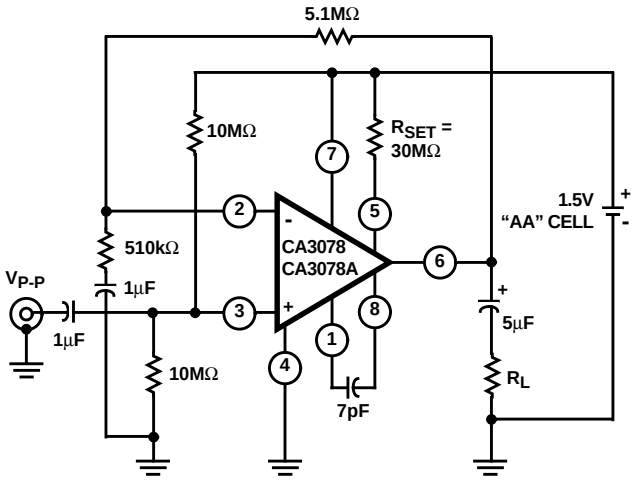


FIGURE 5. NON-INVERTING 20dB AMPLIFIER CIRCUIT

TABLE 1. UNITY GAIN SLEW RATE vs COMPENSATION - CA3078 AND CA3078A

V_{SUPPLY} = ±6V, Output Voltage (V_O) = ±5V, Load Resistance (R_L) = 10kΩ, Transient Response: 10% overshoot for an output voltage of 100mV, Ambient Temperature (T_A) = 25°C

COMPENSATION TECHNIQUE	UNITY GAIN (INVERTING) FIGURE 1					UNITY GAIN (NON-INVERTING) FIGURE 2				
	R_1	C_1	R_2	C_2	SLEW RATE	R_1	C_1	R_2	C_2	SLEW RATE
	kΩ	pF	kΩ	µF	V/µs	kΩ	pF	kΩ	µF	V/µs
CA3078 - I_Q = 100µA										
Single Capacitor	0	750	∞	0	0.0085	0	1500	∞	0	0.0095
Resistor and Capacitor	3.5	350	∞	0	0.04	5.3	500	∞	0	0.024
Input	∞	0	0.25	0.306	0.67	∞	0	0.311	0.45	0.67
CA3078A - I_Q = 20µA										
Single Capacitor	0	300	∞	0	0.0095	0	800	∞	0	0.003
Resistor and Capacitor	14	100	∞	0	0.027	34	125	∞	0	0.02
Input	∞	0	0.644	0.156	0.29	∞	0	0.77	0.4	0.4

Application Information

Compensation Techniques

The CA3078A and CA3078 can be phase compensated with one or two external components depending upon the closed loop gain, power consumption, and speed desired. The recommended compensation is a resistor in series with a capacitor connected from Terminal 1 to Terminal 8. Values of the resistor and capacitor required for compensation as a function of closed loop gain are shown in Figures 25 and 26. These curves represent the compensation necessary at quiescent currents of 100µA and 20µA, respectively, for a transient response with 10% overshoot. Figures 23 and 24 show the slew rates that can be obtained with the two different compensation techniques. Higher speeds can be achieved with input compensation, but this increases noise output. Compensation can also be accomplished with a single capacitor connected from Terminal 1 to Terminal 8, with speed being sacrificed for simplicity. Table 1 gives an indication of slew rates that can be obtained with various compensation techniques at quiescent currents of 100µA and 20µA.

Single Supply Operation

The CA3078A and CA3078 can operate from a single supply with a minimum total supply voltage of 1.5V. Figures 4 and 5 show the CA3078A or CA3078 in inverting and non-inverting 20dB amplifier configurations utilizing a 1.5V type “AA” cell for a supply. The total consumption for either circuit is approximately 675nW. The output voltage swing in this configuration is 300mV_{P-P} with a 20kΩ load.

Typical Performance Curves

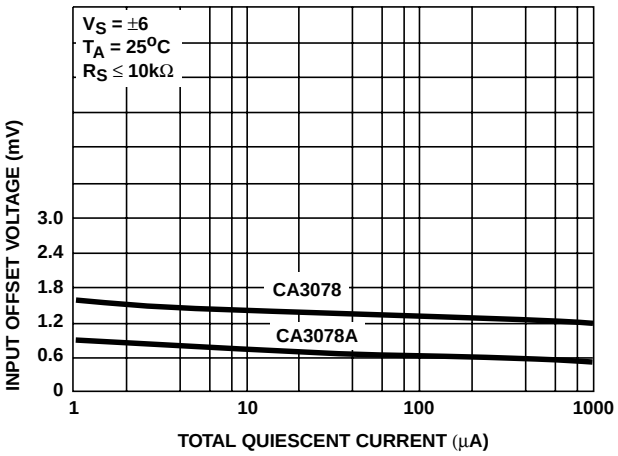


FIGURE 6. INPUT OFFSET VOLTAGE vs TOTAL QUIESCENT CURRENT

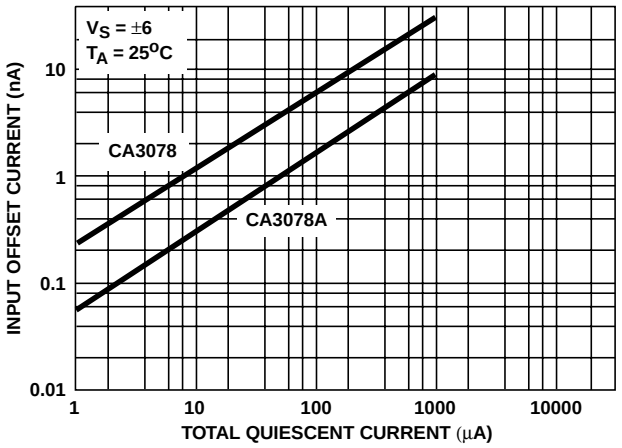


FIGURE 7. INPUT OFFSET CURRENT vs TOTAL QUIESCENT CURRENT

Typical Performance Curves (Continued)

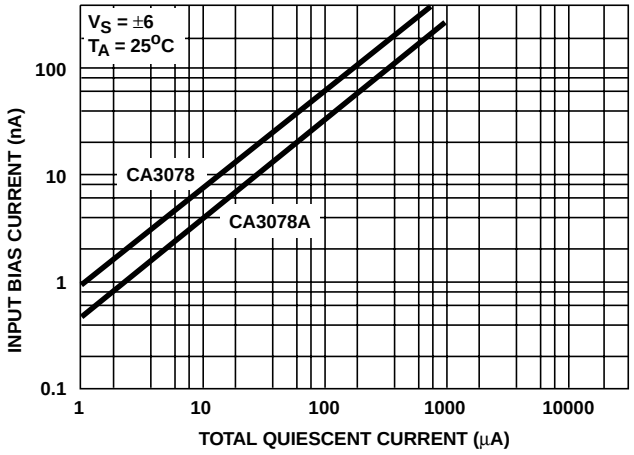


FIGURE 8. INPUT BIAS CURRENT vs TOTAL QUIESCENT CURRENT

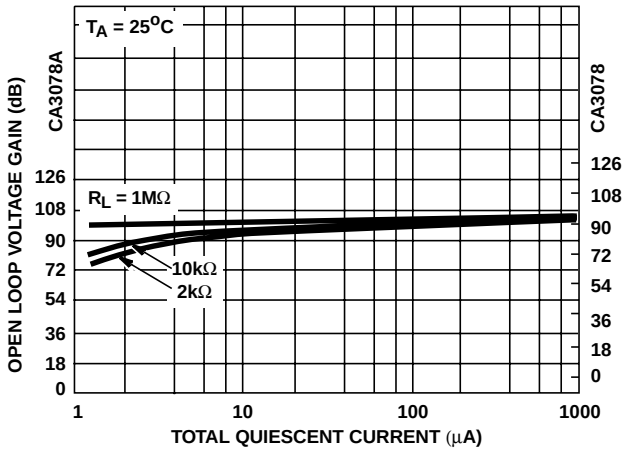


FIGURE 9. OPEN LOOP VOLTAGE GAIN vs TOTAL QUIESCENT CURRENT

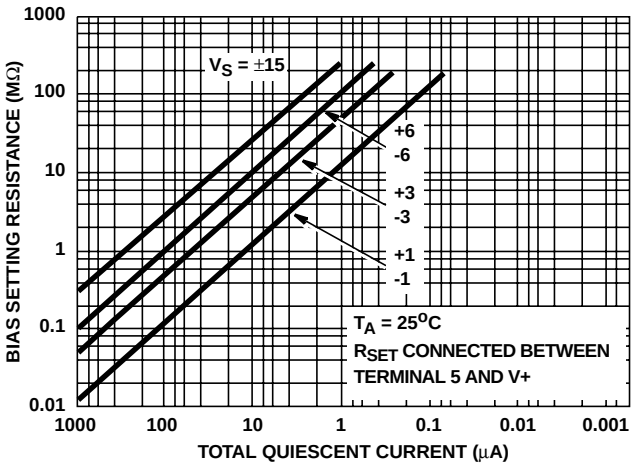


FIGURE 10. BIAS SETTING RESISTANCE vs TOTAL QUIESCENT CURRENT

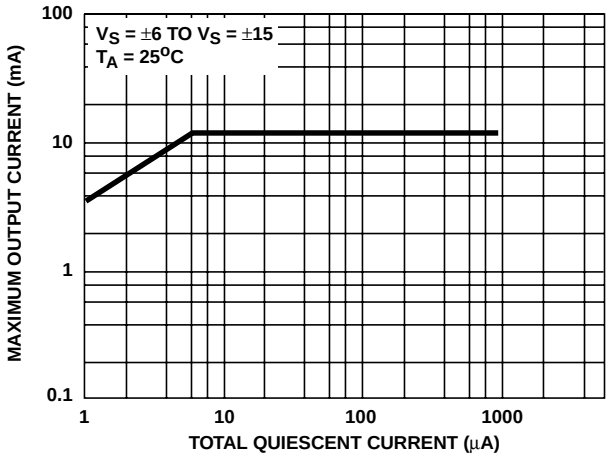


FIGURE 11. MAXIMUM OUTPUT CURRENT vs TOTAL QUIESCENT CURRENT

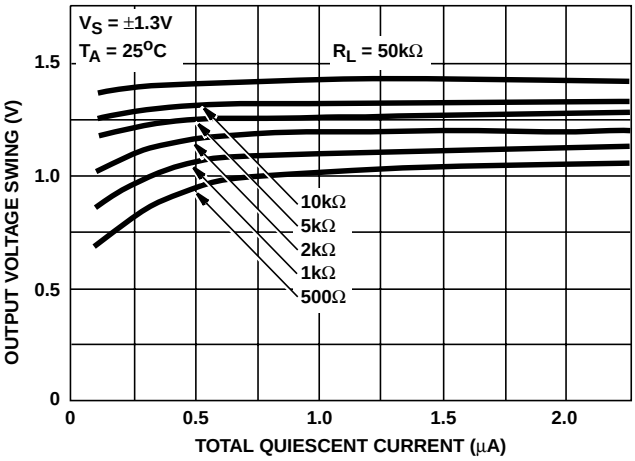


FIGURE 12. OUTPUT VOLTAGE SWING vs TOTAL QUIESCENT CURRENT

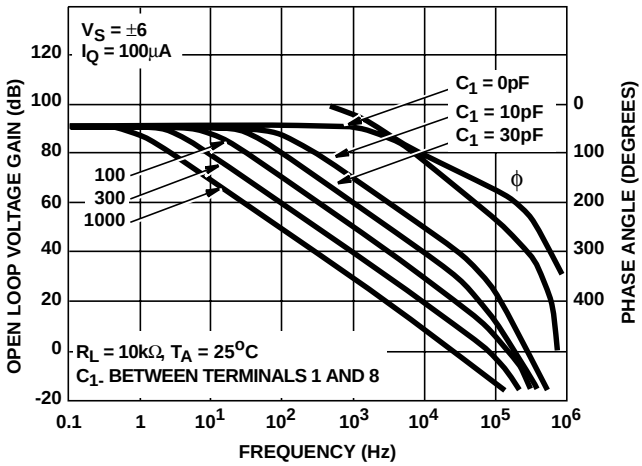


FIGURE 13. OPEN LOOP VOLTAGE GAIN vs FREQUENCY

Typical Performance Curves (Continued)

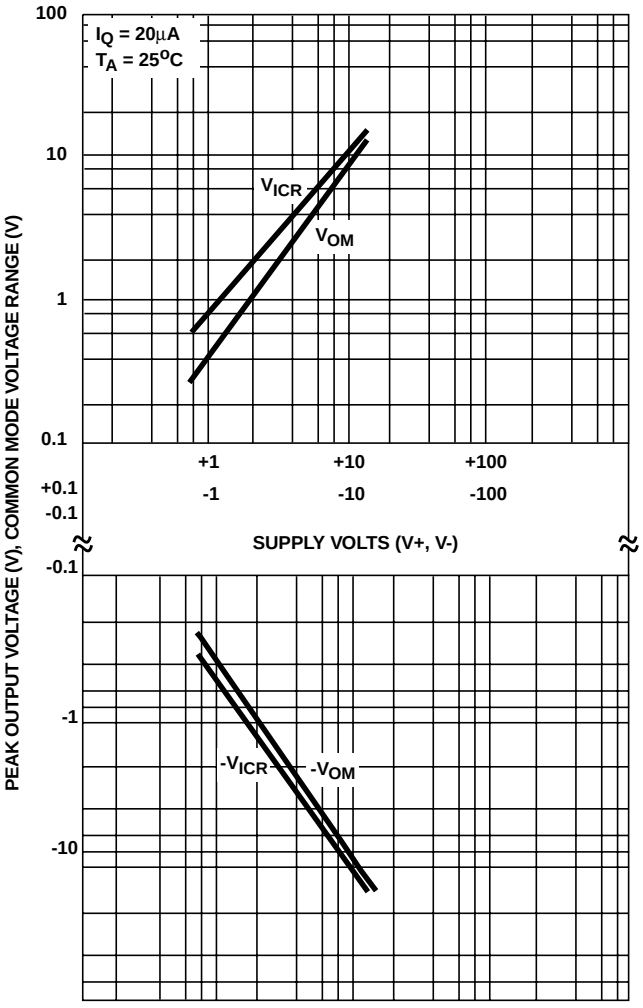


FIGURE 14. OUTPUT AND COMMON MODE VOLTAGE vs SUPPLY VOLTAGE

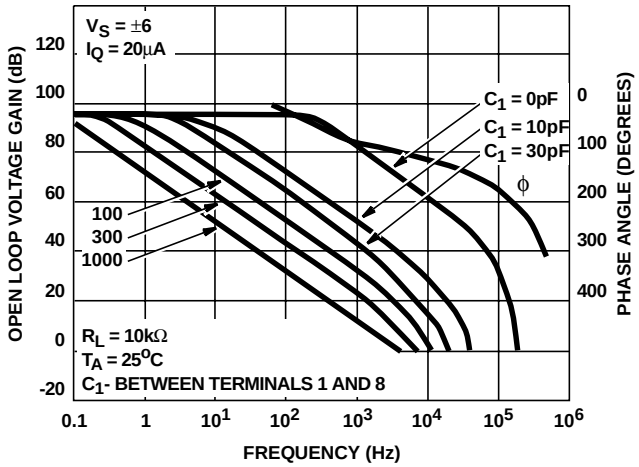


FIGURE 15. OPEN LOOP VOLTAGE GAIN vs FREQUENCY

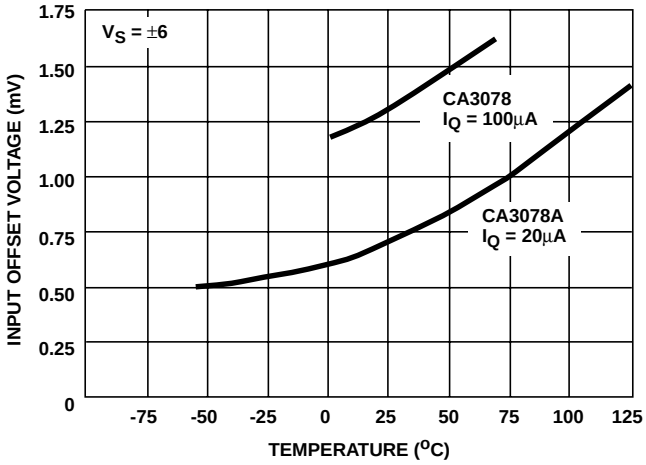


FIGURE 16. INPUT OFFSET VOLTAGE vs TEMPERATURE

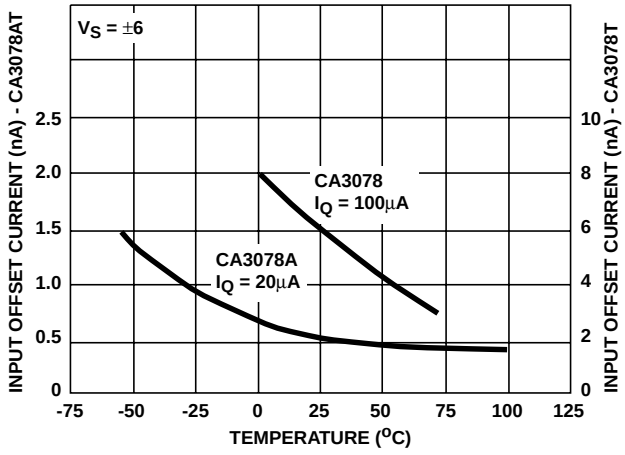


FIGURE 17. INPUT OFFSET CURRENT vs TEMPERATURE

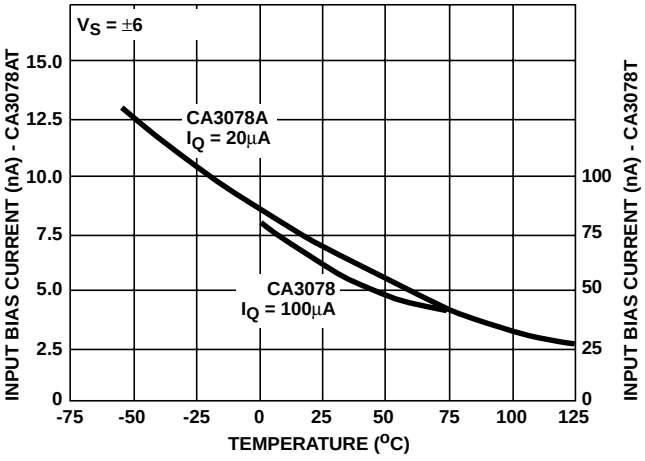


FIGURE 18. INPUT BIAS CURRENT vs TEMPERATURE

Typical Performance Curves (Continued)

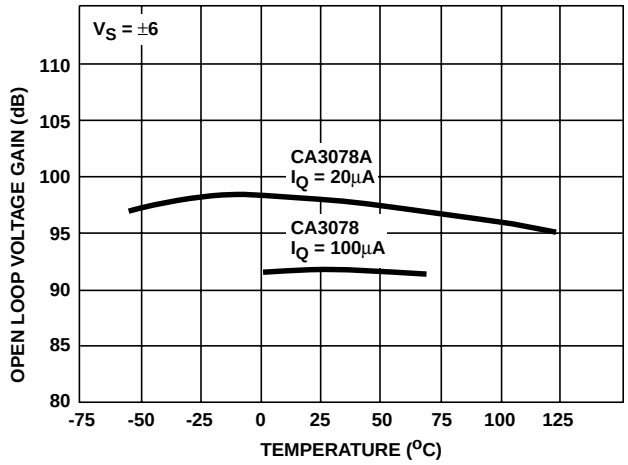


FIGURE 19. OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

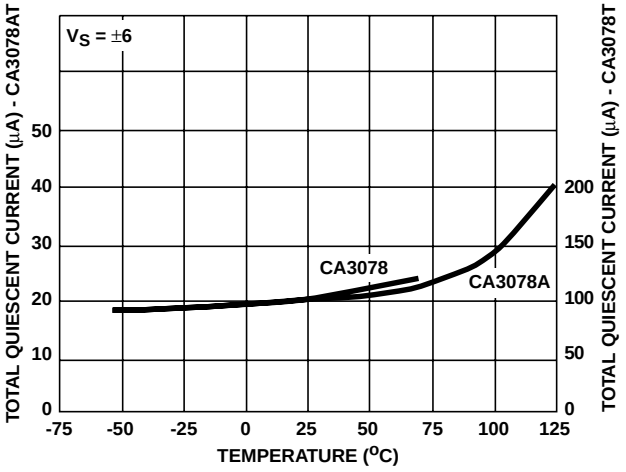


FIGURE 20. TOTAL QUIESCENT CURRENT vs TEMPERATURE

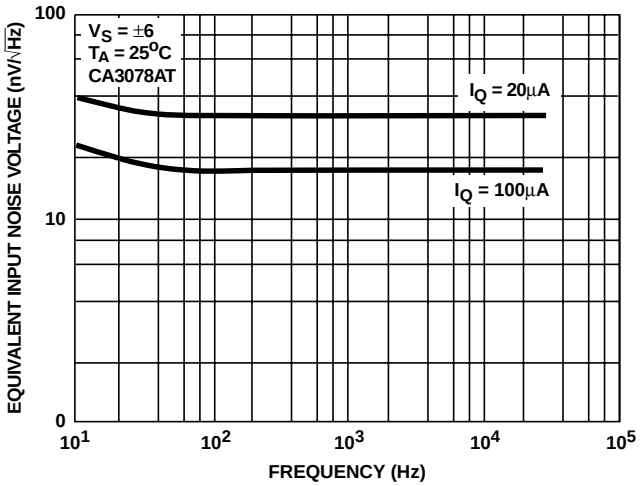


FIGURE 21. EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

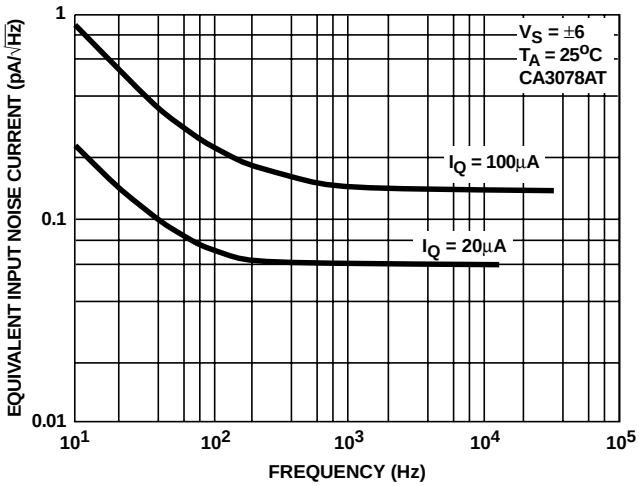
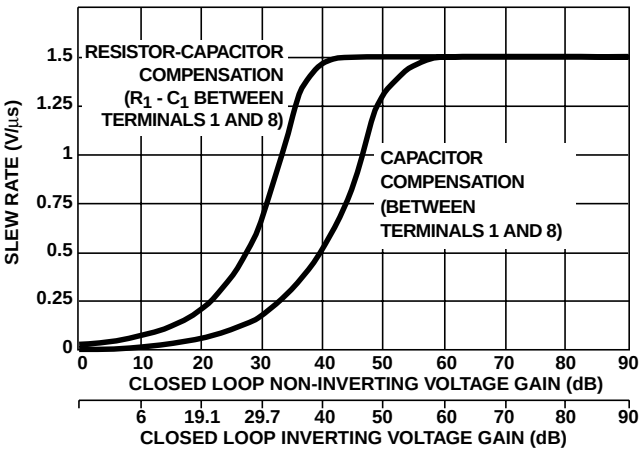


FIGURE 22. EQUIVALENT INPUT NOISE CURRENT vs FREQUENCY

Typical Performance Curves (Continued)



Supply Volts: V+ = +6, V- = -6

Quiescent Current (I_Q) = 100µA

Ambient Temperature (T_A) = 25°C

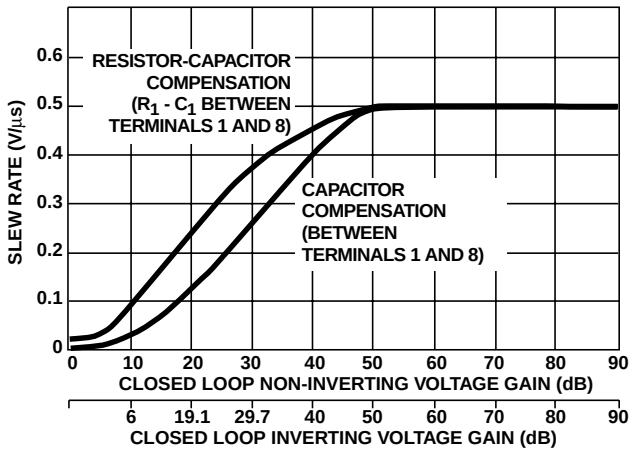
Load Impedance: R_L = 10kΩ, C_L = 100pF

Feedback Resistance (R_F) = 0.1MΩ

Output Voltage (V_{OP-P}) = 10V

R_1 determined for transient response with 10% overshoot on a 100mV output signal (R_1 x C_1 = 2.5 x 10^{-6})

FIGURE 23. SLEW RATE vs CLOSED LOOP GAIN FOR IQ = 100mA - CA3078



Supply Volts: V+ = +6, V- = -6

Quiescent Current (I_Q) = 20µA

Ambient Temperature (T_A) = 25°C

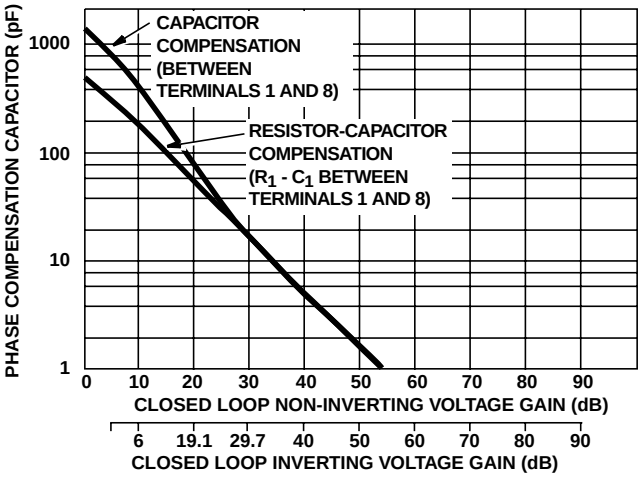
Load Impedance: R_L = 10kΩ, C_L = 100pF

Feedback Resistance (R_F) = 0.1MΩ

Output Voltage (V_{OP-P}) = 10V

R_1 determined for transient response with 10% overshoot on a 100mV output signal (R_1 x C_1 = 2 x 10^{-6})

FIGURE 24. SLEW RATE vs CLOSED LOOP GAIN FOR IQ = 20mA - CA3078A



Supply Volts: V+ = +6, V- = -6

Quiescent Current (I_Q) = 100µA

Ambient Temperature (T_A) = 25°C

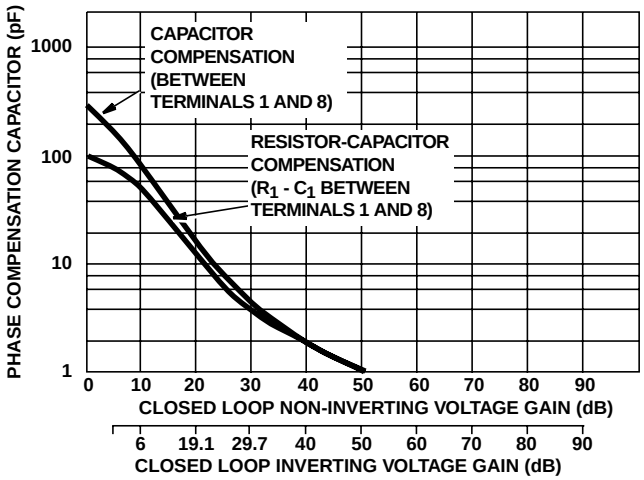
Load Impedance: R_L = 10kΩ, C_L = 100pF

Feedback Resistance (R_F) = 0.1MΩ

Output Voltage (V_{OP-P}) = 100mV

R_1 determined for transient response with 10% overshoot on a 100mV output signal (R_1 x C_1 = 2.5 x 10^{-6})

FIGURE 25. PHASE COMPENSATION CAPACITANCE vs CLOSED LOOP GAIN - CA3078



Supply Volts: V+ = +6, V- = -6

Quiescent Current (I_Q) = 20µA

Ambient Temperature (T_A) = 25°C

Load Impedance: R_L = 10kΩ, C_L = 100pF

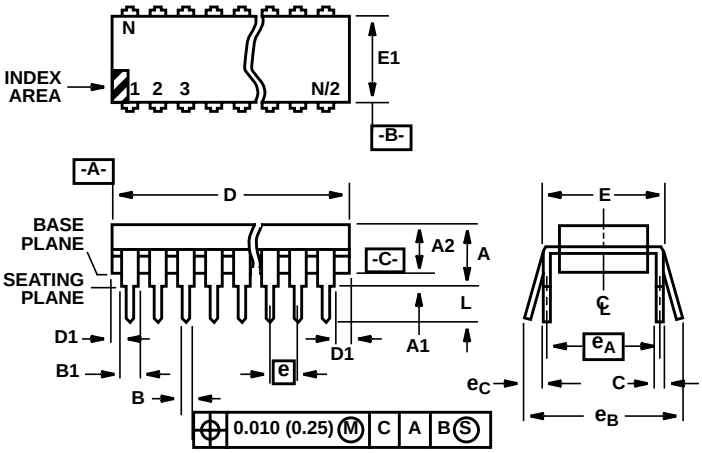
Feedback Resistance (R_F) = 0.1MΩ

Output Voltage (V_{OP-P}) = 100mV

R_1 determined for transient response with 10% overshoot on a 100mV output signal (R_1 x C_1 = 2 x 10^{-6})

FIGURE 26. PHASE COMPENSATION CAPACITANCE vs CLOSED LOOP GAIN - CA3078A

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

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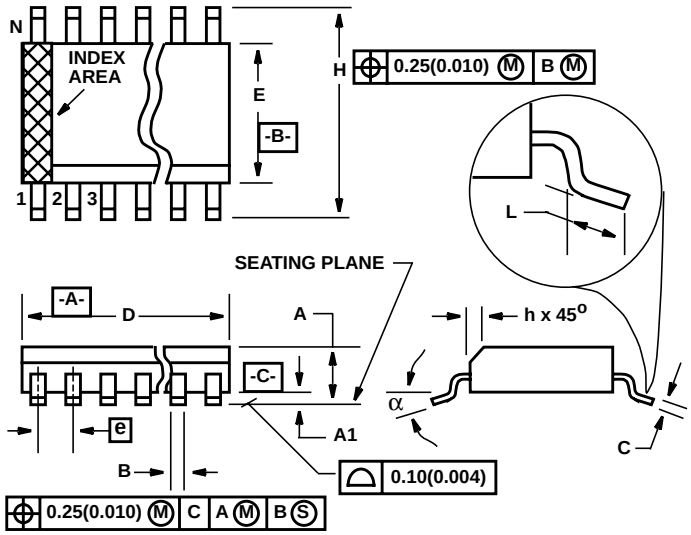
Small Outline Plastic Packages (SOIC)



NOTES:

11. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
12. Dimensioning and tolerancing per ANSI Y14.5M-1982.
13. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
14. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
15. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
16. “L” is the length of terminal for soldering to a substrate.
17. “N” is the number of terminal positions.
18. Terminal numbers are shown for reference only.
19. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
20. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0^o	8^o	0^o	8^o	-

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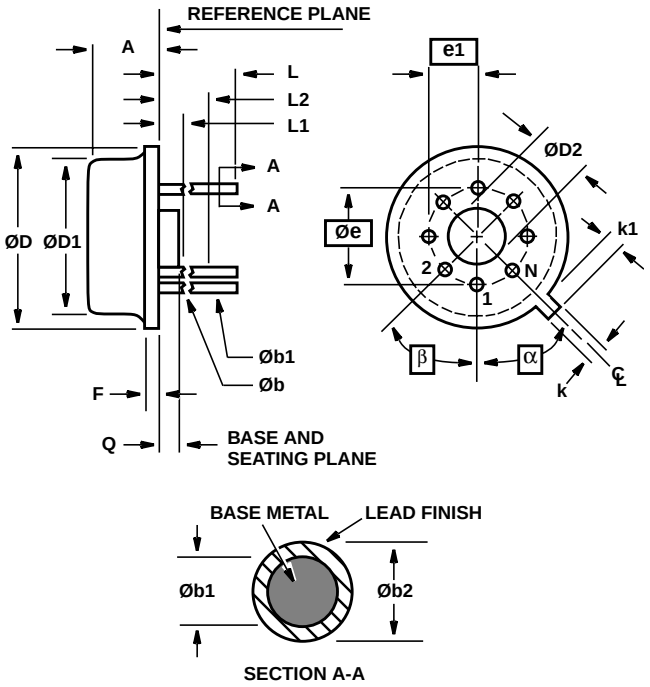
Metal Can Packages (Can)



T8.C **MIL-STD-1835 MACY1-X8 (A1)**
8 LEAD METAL CAN PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	-
Øb	0.016	0.019	0.41	0.48	1
Øb1	0.016	0.021	0.41	0.53	1
Øb2	0.016	0.024	0.41	0.61	-
ØD	0.335	0.375	8.51	9.40	-
ØD1	0.305	0.335	7.75	8.51	-
ØD2	0.110	0.160	2.79	4.06	-
e	0.200 BSC		5.08 BSC		-
e1	0.100 BSC		2.54 BSC		-
F	-	0.040	-	1.02	-
k	0.027	0.034	0.69	0.86	-
k1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L1	-	0.050	-	1.27	1
L2	0.250	-	6.35	-	1
Q	0.010	0.045	0.25	1.14	-
α	45^{o} BSC		45^{o} BSC		3
β	45^{o} BSC		45^{o} BSC		3
N	8		8		4

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NOTES:

1. (All leads) Øb applies between L1 and L2. Øb1 applies between L2 and 0.500 from the reference plane. Diameter is uncontrolled in L1 and beyond 0.500 from the reference plane.
2. Measured from maximum diameter of the product.
3. α is the basic spacing from the centerline of the tab to terminal 1 and β is the basic spacing of each lead or lead position (N -1 places) from α, looking at the bottom of the package.
4. N is the maximum number of terminal positions.
5. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
6. Controlling dimension: INCH.

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Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (321) 724-7000
FAX: (321) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029