

# CXK5V8512TM -85LLX/10LLX

## 65536-word × 8-bit High Speed CMOS Static RAM

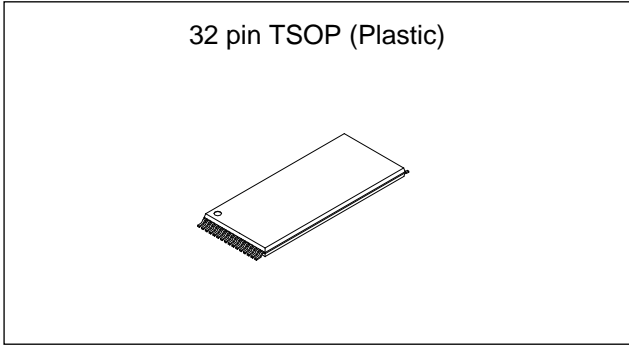
**Description**

The CXK5V8512TM is a high speed CMOS static RAM organized as 65536-words by 8-bits.

A polysilicon TFT cell technology realized extremely low stand-by current and higher data retention stability.

Operating on a single 3.3V supply, and special feature are low power consumption, high speed.

The CXK5V8512TM is a suitable RAM for portable equipment with battery back up.



**Features**

- Extended operating temperature range: -25 to +85°C
- Fast access time:
 

	(Access time)
-85LLX	85ns (Max.)
-10LLX	100ns (Max.)
- Low standby current: 14µA (Max.)
- Low data retention current: 12µA (Max.)
- Single 3.3V supply: 3.3V ± 0.3V
- Low voltage data retention: 2.0V (Min.)
- Package  
8mm × 20mm 32 pin TSOP package

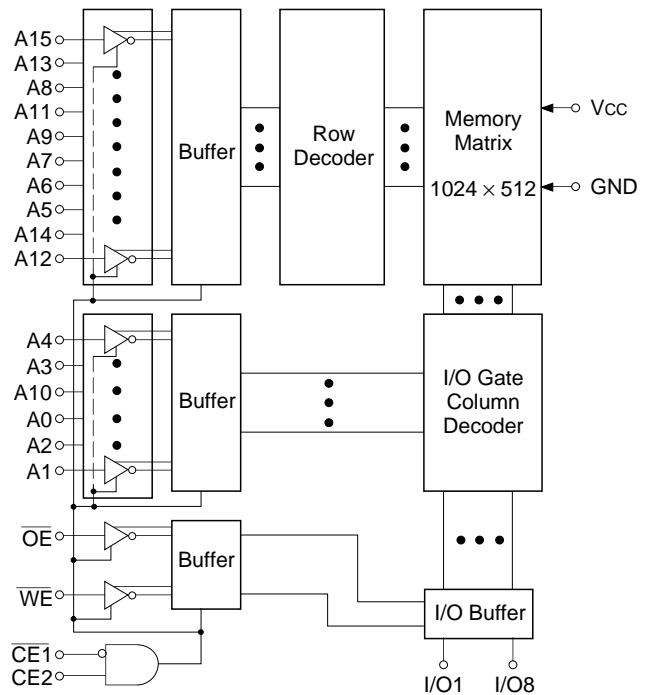
**Function**

65536-word × 8-bit static RAM

**Structure**

Silicon gate CMOS IC

**Block Diagram**



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Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A15	Address input
I/O1 to I/O8	Data input output
$\overline{CE1}$ , CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	Power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	Vcc	-0.5 to +4.6	V
Input voltage	V <sub>IN</sub>	-0.5* to Vcc + 0.5	V
Input and output voltage	V <sub>I/O</sub>	-0.5* to Vcc + 0.5	V
Allowable power dissipation	P <sub>D</sub>	0.7	W
Operating temperature	T <sub>opr</sub>	-25 to +85	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	°C
Soldering temperature · time	T <sub>solder</sub>	235 · 10	°C · s

\* V<sub>IN</sub>, V<sub>I/O</sub> = -3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O pin	Vcc Current
H	×	×	×	Not selected	High Z	I <sub>SB1</sub> , I <sub>SB2</sub>
×	L	×	×	Not selected	High Z	I <sub>SB1</sub> , I <sub>SB2</sub>
L	H	H	H	Output disable	High Z	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC3</sub>
L	H	L	H	Read	Data out	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC3</sub>
L	H	×	L	Write	Data in	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC3</sub>

×: "H" or "L"

DC Recommended Operating Conditions

(Ta = -25 to +85°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	3.0	3.3	3.6	V
Input high voltage	V <sub>IH</sub>	2.2	—	Vcc + 0.3	V
Input low voltage	V <sub>IL</sub>	-0.3*	—	0.6	V

\* V<sub>IL</sub> = -3.0V Min. for pulse width less than 50ns.

## Electrical Characteristics

## • DC Characteristics

(V<sub>CC</sub> = 3.3V ± 0.3V, GND = 0V, T<sub>a</sub> = -25 to +85°C)

Item	Symbol	Test conditions	Min.	Typ.*	Max.	Unit	
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = GND to V <sub>CC</sub>	-1	—	+1	μA	
Output leakage current	I <sub>LO</sub>	$\overline{CE1} = V_{IH}$ or $\overline{CE2} = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ V <sub>I/O</sub> = GND to V <sub>CC</sub>	-1	—	+1	μA	
Operating power supply current	I <sub>CC1</sub>	$\overline{CE1} = V_{IL}$ , $\overline{CE2} = V_{IH}$ V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OUT</sub> = 0mA	—	1	3	mA	
Average operating current	I <sub>CC2</sub>	Min. cycle duty = 100% I <sub>OUT</sub> = 0mA	85LLX	—	30	40	mA
			10LLX	—	25	35	
	I <sub>CC3</sub>	Cycle time 1μs duty = 100% I <sub>OUT</sub> = 0mA $\overline{CE1} \leq 0.2V$ $\overline{CE2} \geq V_{CC} - 0.2V$ V <sub>IL</sub> ≤ 0.2V V <sub>IH</sub> ≥ V <sub>CC</sub> - 0.2V	—	5	10	mA	
Standby current	I <sub>SB1</sub>	CE2 ≤ 0.2V or { $\overline{CE1} \geq V_{CC} - 0.2V$ $\overline{CE2} \geq V_{CC} - 0.2V$	-25 to +85°C	—	—	14	μA
			-25 to +70°C	—	—	7	
			+25°C	—	0.24	—	
	I <sub>SB2</sub>	$\overline{CE1} = V_{IH}$ or $\overline{CE2} = V_{IL}$	—	0.12	1.4	mA	
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -2.0mA	2.4	—	—	V	
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.0mA	—	—	0.4	V	

\* V<sub>CC</sub> = 3.3V, T<sub>a</sub> = 25°C

**I/O capacitance**

(Ta = 25°C, f = 1MHz)

Item	Symbol	Test conditons	Min.	Typ.	Max.	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V	—	—	8	pF
I/O capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0V	—	—	10	pF

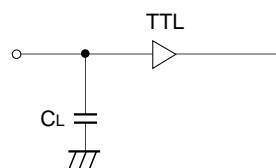
**Note)** This parameter is sampled and is not 100% tested.

**AC Characteristics**

• **AC test conditions** (V<sub>CC</sub> = 3.3V ± 0.3V, Ta = -25 to +85°C)

Item		Conditions
Input pulse high level		V <sub>IH</sub> = 2.2V
Input pulse low level		V <sub>IL</sub> = 0.6V
Input rise time		t <sub>r</sub> = 5ns
Input fall time		t <sub>f</sub> = 5ns
Input and output reference level		1.4V
Output load conditions	-85LLX	C <sub>L</sub> * = 30pF, 1TTL
	-10LLX	C <sub>L</sub> * = 100pF, 1TTL

• Test circuit



\* C<sub>L</sub> includes scope and jig capacitances.

• **Read cycle** ( $\overline{WE} = "H"$ ) (V<sub>CC</sub> = 3.3V ± 0.3V, GND = 0V, T<sub>a</sub> = -25 to +85°C)

Item	Symbol	-85LLX		-10LLX		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t <sub>RC</sub>	85	—	100	—	ns
Address access time	t <sub>AA</sub>	—	85	—	100	ns
Chip enable access time ( $\overline{CE1}$ )	t <sub>CO1</sub>	—	85	—	100	ns
Chip enable access time (CE2)	t <sub>CO2</sub>	—	85	—	100	ns
Output enable to output valid	t <sub>OE</sub>	—	40	—	50	ns
Output hold from address change	t <sub>OH</sub>	10	—	10	—	ns
Chip enable to output in low Z ( $\overline{CE1}$ , CE2)	t <sub>LZ1</sub> , t <sub>LZ2</sub>	10	—	10	—	ns
Output enable to output in low Z ( $\overline{OE}$ )	t <sub>OLZ</sub>	5	—	5	—	ns
Chip disable to output in high Z ( $\overline{CE1}$ , CE2)	t <sub>HZ1</sub> <sup>*</sup> , t <sub>HZ2</sub> <sup>*</sup>	—	35	—	40	ns
Output disable to output in high Z ( $\overline{OE}$ )	t <sub>OHZ</sub> <sup>*</sup>	—	30	—	35	ns

\* t<sub>HZ1</sub>, t<sub>HZ2</sub> and t<sub>OHZ</sub> are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

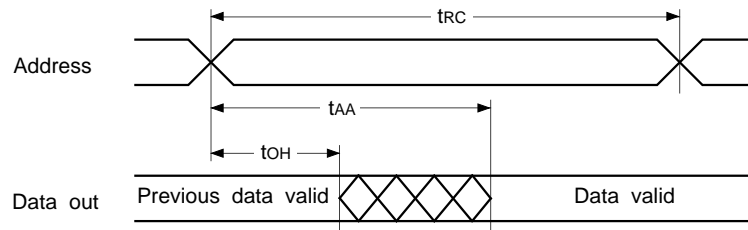
• **Write cycle** (V<sub>CC</sub> = 3.3V ± 0.3V, GND = 0V, T<sub>a</sub> = -25 to +85°C)

Item	Symbol	-85LLX		-10LLX		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t <sub>WC</sub>	85	—	100	—	ns
Address valid to end of write	t <sub>AW</sub>	70	—	80	—	ns
Chip enable to end of write	t <sub>CW</sub>	70	—	80	—	ns
Data to write time overlap	t <sub>DW</sub>	35	—	40	—	ns
Data hold from write time	t <sub>DH</sub>	0	—	0	—	ns
Write pulse width	t <sub>WP</sub>	60	—	70	—	ns
Address setup time	t <sub>AS</sub>	0	—	0	—	ns
Write recovery time ( $\overline{WE}$ )	t <sub>WR</sub>	5	—	5	—	ns
Write recovery time ( $\overline{CE1}$ , CE2)	t <sub>WR1</sub>	5	—	5	—	ns
Output active from end of write	t <sub>OW</sub>	5	—	5	—	ns
Write to output in high Z	t <sub>WHZ</sub> <sup>*</sup>	—	35	—	40	ns

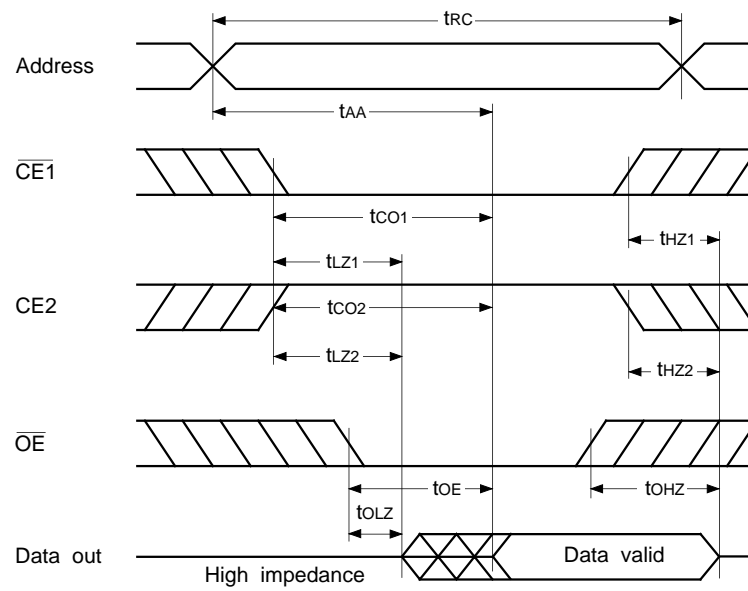
\* t<sub>WHZ</sub> is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

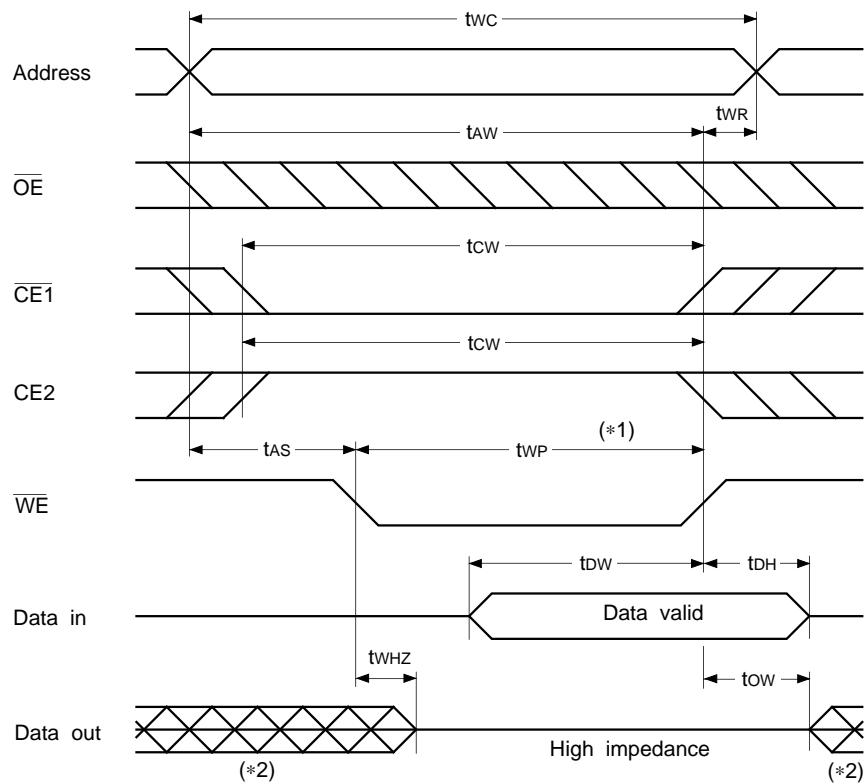
- Read cycle (1) :  $\overline{CE1} = \overline{OE} = V_{IL}$ ,  $CE2 = V_{IH}$ ,  $\overline{WE} = V_{IH}$



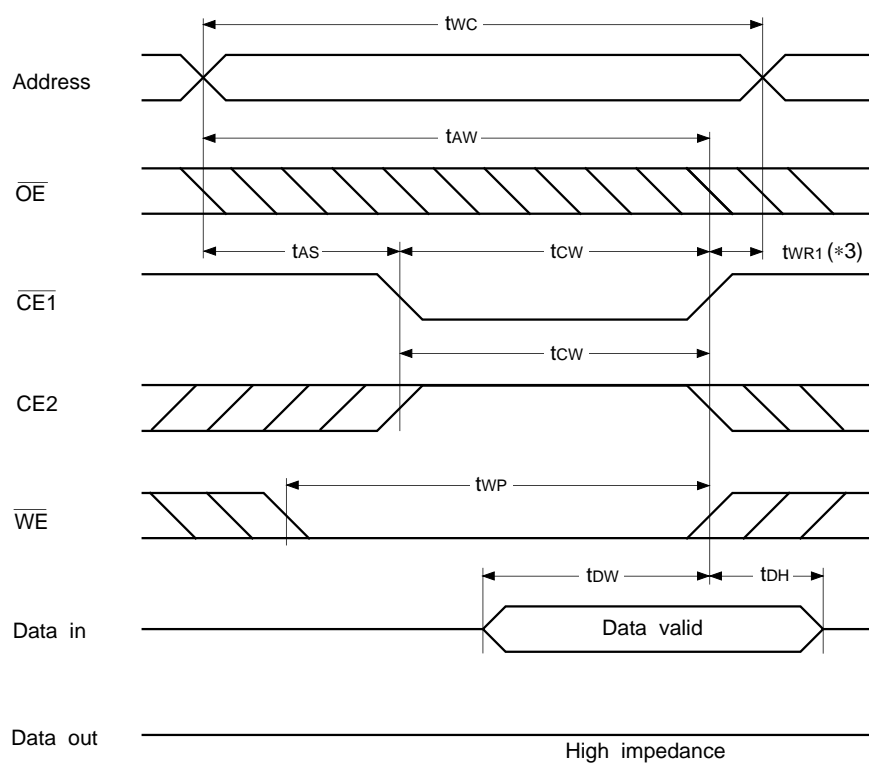
- Read cycle (2) :  $\overline{WE} = V_{IH}$



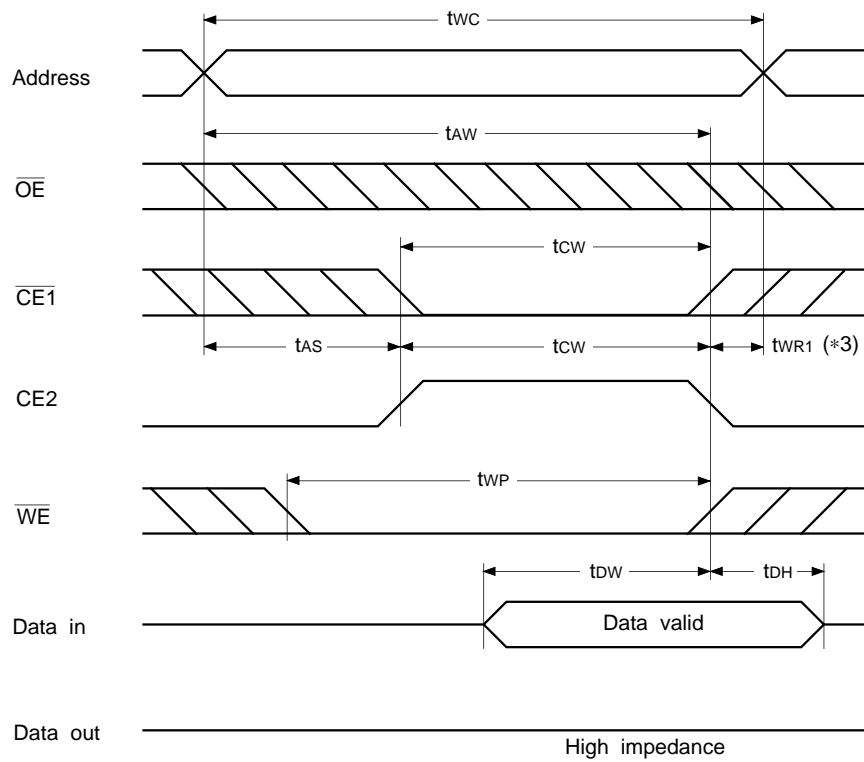
• Write cycle (1) :  $\overline{WE}$  control



• Write cycle (2) :  $\overline{CE1}$  control



• Write cycle (3) : CE2 control

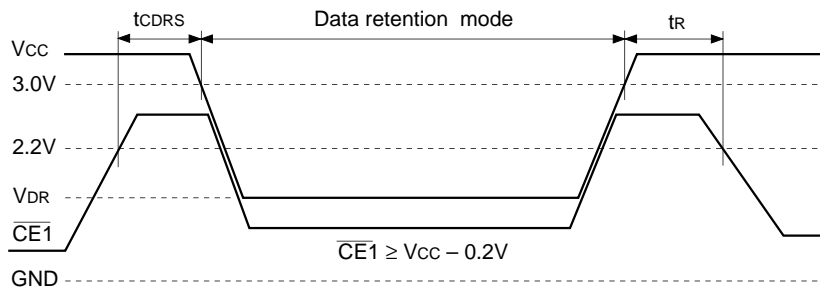


- \*1 Write is executed when both  $\overline{CE1}$  and  $\overline{WE}$  are at low and CE2 is at high simultaneously.
- \*2 Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.
- \*3  $t_{WR1}$  is tested from either the rising edge of  $\overline{CE1}$  or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

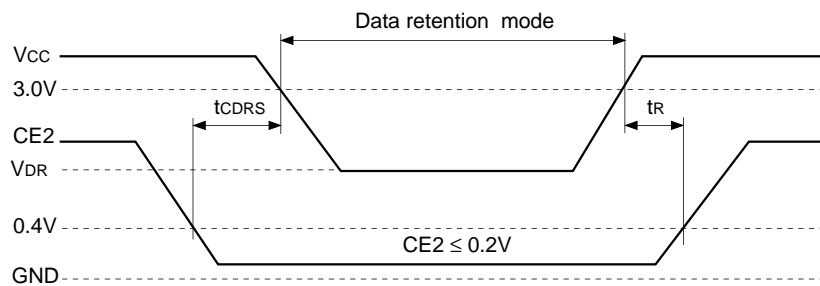


**Data retention waveform**

• **Low supply voltage data retention waveform (1) ( $\overline{CE1}$  control)**



• **Low supply voltage data retention waveform (2) (CE2 control)**



**Data Retention Characteristics**

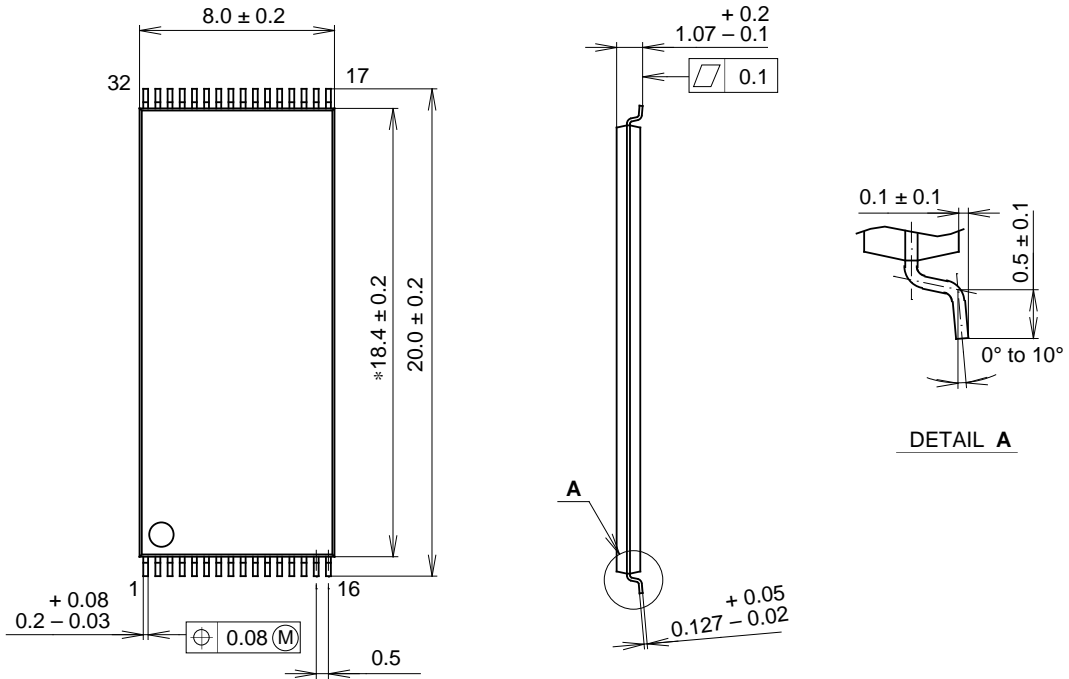
( $T_a = -25$  to  $+85^\circ\text{C}$ )

Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit	
Data retention voltage	$V_{DR}$	*	2.0	—	3.6	V	
Data retention current	$I_{CCDR1}$	$V_{CC} = 3.0V^*$	$-25$ to $+85^\circ\text{C}$	—	—	12	$\mu\text{A}$
			$-25$ to $+70^\circ\text{C}$	—	—	6	
			$+25^\circ\text{C}$	—	0.2	—	
	$I_{CCDR2}$	$V_{CC} = 2.0$ to $3.6V$	—	0.24	14	$\mu\text{A}$	
Data retention setup time	$t_{CDRS}$	Chip disable to data retention mode	0	—	—	ns	
Recovery time	$t_R$		5	—	—	ms	

\*  $\overline{CE1} \geq V_{CC} - 0.2V$ ,  $CE2 \geq V_{CC} - 0.2V$  ( $\overline{CE1}$  control) or  $CE2 \leq 0.2V$  (CE2 control)

Package Outline Unit: mm

32PIN TSOP (I) (PLASTIC)



NOTE: Dimension "\*" does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	TSOP (I) -32P-L01	PACKAGE MATERIAL	EPOXY / PHENOL RESIN
EIAJ CODE	TSOP (I) 032-P-0820-A	LEAD TREATMENT	SOLDER PLATING
JEDEC CODE	_____	LEAD MATERIAL	42 ALLOY
		PACKAGE WEIGHT	_____