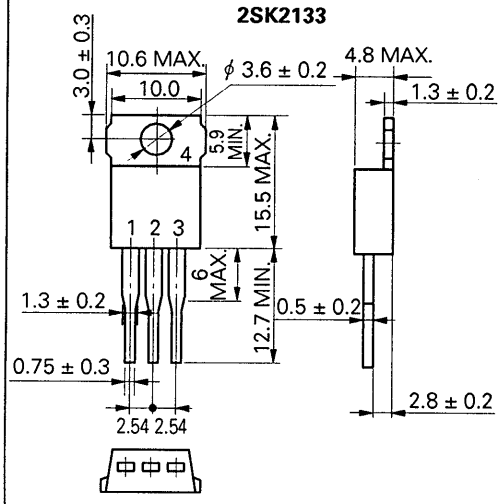
NEC

MOS FIELD EFFECT POWER TRANSISTORS
2SK2133, 2SK2133-Z

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

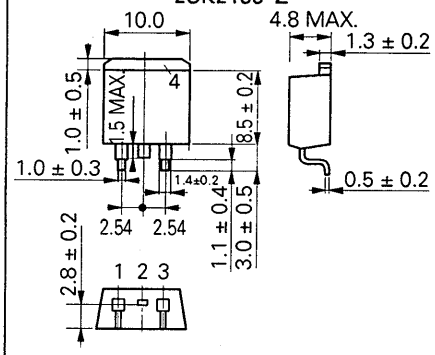
PACKAGE DIMENSIONS
(Unit : mm)

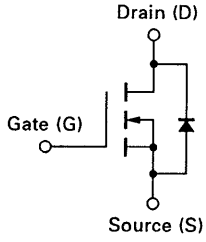
2SK2133



MP-25 (TO-220AB)

2SK2133-Z





1. Gate
2. Drain
3. Source
4. Fin (Drain)

(Diode in the figure is the parasitic diode)

DESCRIPTION

The 2SK2133, 2SK2133-Z are N-channel Power MOS Field Effect Transistors designed for high voltage switching applications.

FEATURES

- Low On-state Resistance
  $R_{DS(on)}$ = 0.21 Ω MAX. (V_{GS} = 10 V, I_D = 8.0 A)
- Low C_{iss} C_{iss} = 1 090 pF TYP.
- High Avalanche Capability Ratings

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures			
Storage Temperature		−55 to +150	°C
Channel Temperature		150	°C MAX.
Maximum Power Dissipation			
Total Power Dissipation (T_a = 25 °C)		1.5	W
Total Power Dissipation (T_c = 25 °C)		75	W
Maximum Voltages and Currents (T_a = 25 °C)			
V_{DSS}	Drain to Source Voltage	250	V
V_{GSS}	Gate to Source Voltage	±30	V
$I_{D(DS)}$	Drain Current (DC)	±16	A
$I_{D(pulse)}$*	Drain Current (pulse)	±64	A
Maximum Avalanche Capability Ratings**			
I_{AS}	Single Avalanche Current	16	A
E_{AS}	Single Avalanche Energy	320	mJ

* PW ≦ 10 μs, Duty Cycle ≦ 1 %

** Starting T_{ch} = 25 °C, R_G = 25 Ω, V_{GS} = 20 V → 0

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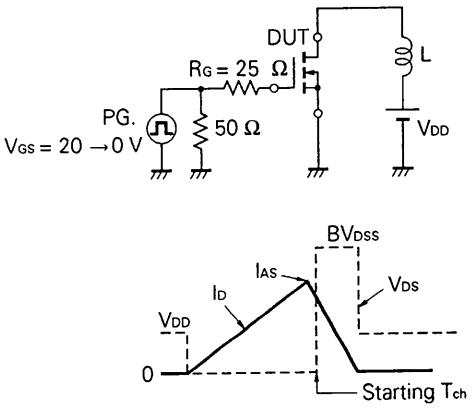
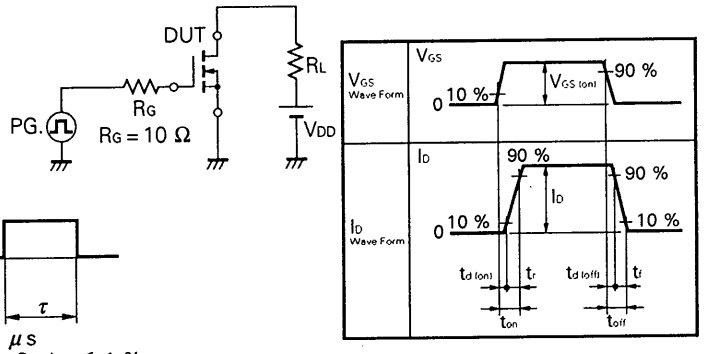
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drian to Source On-state Resistance	R_{DS} (on)		0.21	0.26	Ω	V_{GS} = 10 V, I_D = 8.0 A
Gate to Source Cutoff Voltage	V_{GS} (off)	2.0		4.0	V	V_{DS} = 10 V, I_D = 1 mA
Forward Transfer Admittance	$\|y_{fs}\|$	4.0			S	V_{DS} = 10 V, I_D = 8.0 A
Drain Leakage Current	I_{DSS}			100	μA	V_{DS} = 250 V, V_{GS} = 0
Gate to Source Leakage Current	I_{GSS}			±10	μA	V_{GS} = ±30 V, V_{DS} = 0
Input Capacitance	C_{iss}		1 090		pF	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz
Output Capacitance	C_{oss}		420		pF	
Reverse Transfer Capacitance	C_{rss}		80		pF	
Turn-On Delay Time	$t_{d(on)}$		20		ns	V_{GS} = 10 V V_{DD} = 150 V I_D = 8.0 A, R_G = 10 Ω R_L = 18.75 Ω
Rise Time	t_r		40		ns	
Turn-Off Delay Time	$t_{d(off)}$		60		ns	
Fall Time	t_f		20		ns	
Total Gate Charge	Q_G		25		nC	V_{GS} = 10 V I_D = 16 A V_{DD} = 200 V
Gate to Source Charge	Q_{GS}		8.0		nC	
Gate to Drain Charge	Q_{GD}		14		nC	
Diode Forward Voltage	$V_{F(S-D)}$		1.0		V	I_F = 16 A, V_{GS} = 0
Reverse Recovery Time	t_{rr}		400		ns	I_F = 16 A di / dt = 50 A / μs
Reverse Recovery Charge	Q_{rr}		2.0		μC	

Test Circuit 1 : Avalanche Capability

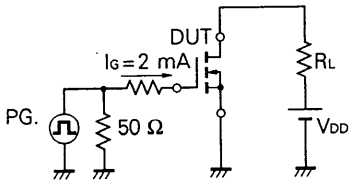


Test Circuit 2 : Switching Time



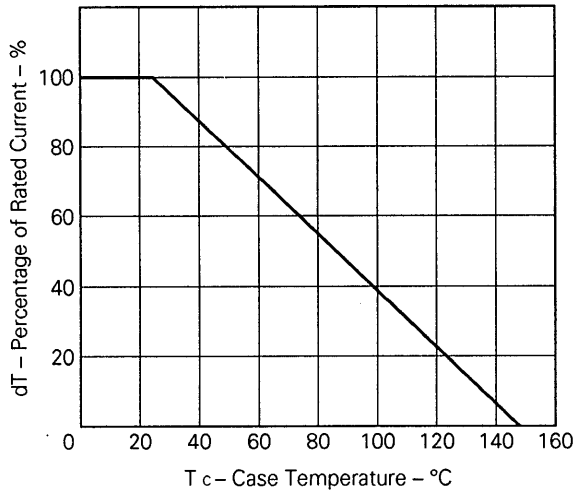
τ = 1 μs
Duty Cycle ≦ 1 %

Test Circuit 3 : Gate Charge

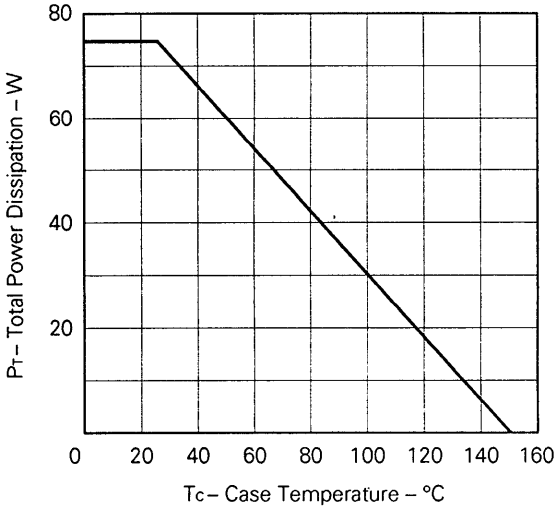


TYPICAL CHARACTERISTICS (T_a = 25 °C)

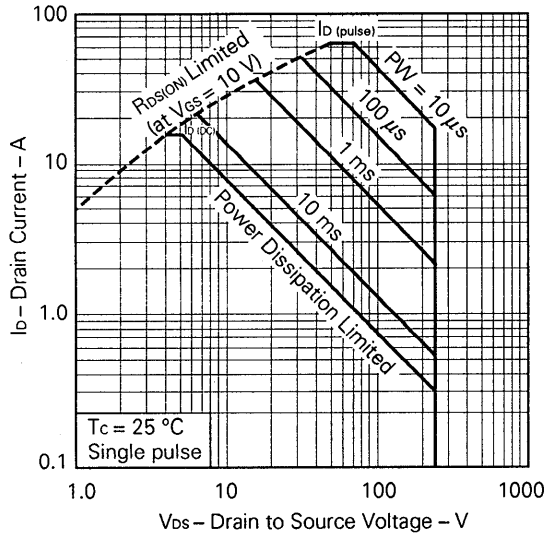
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



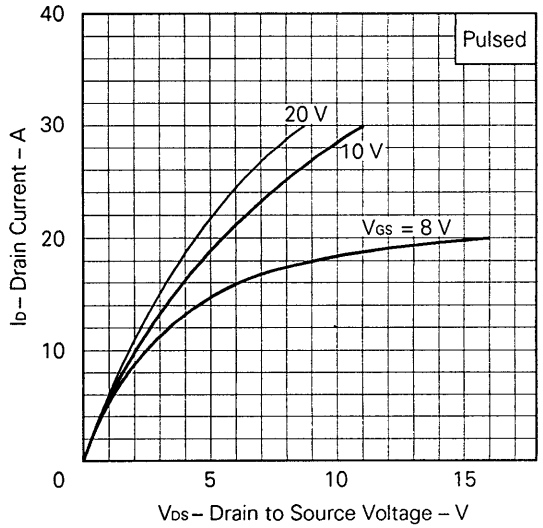
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



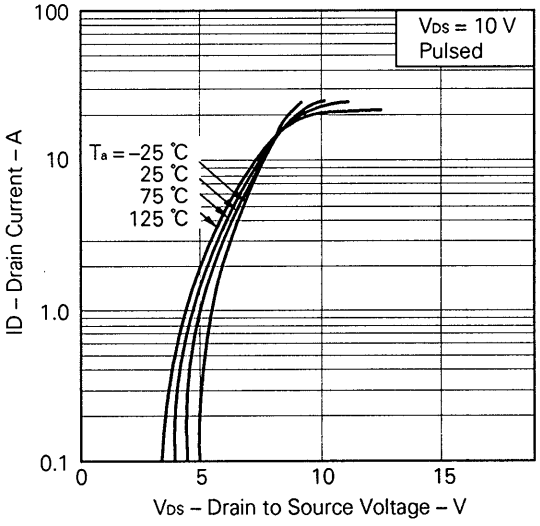
FORWARD BIAS SAFE OPERATING AREA



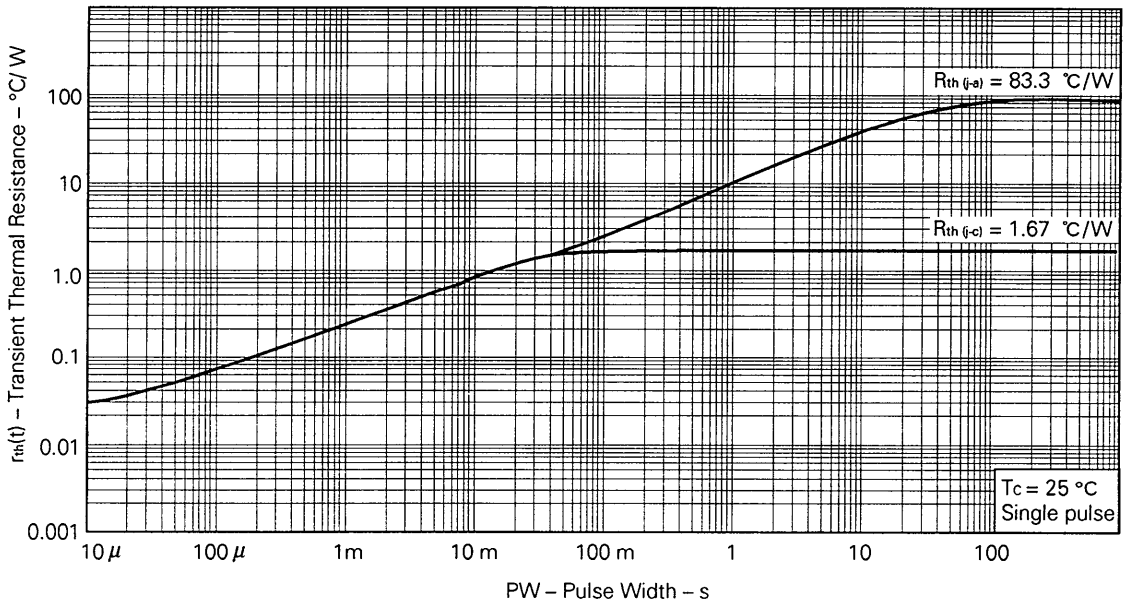
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



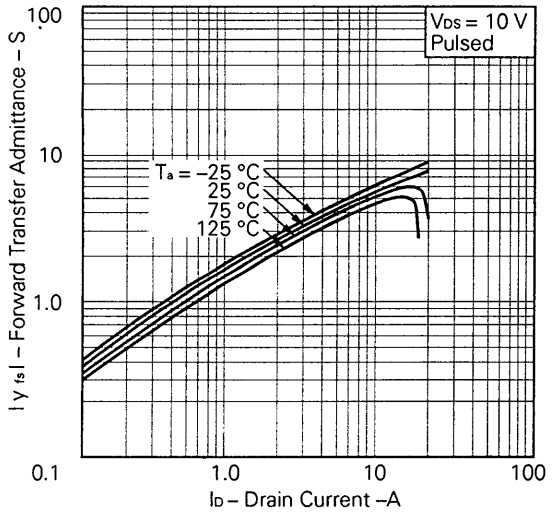
TRANSFER CHARACTERISTICS



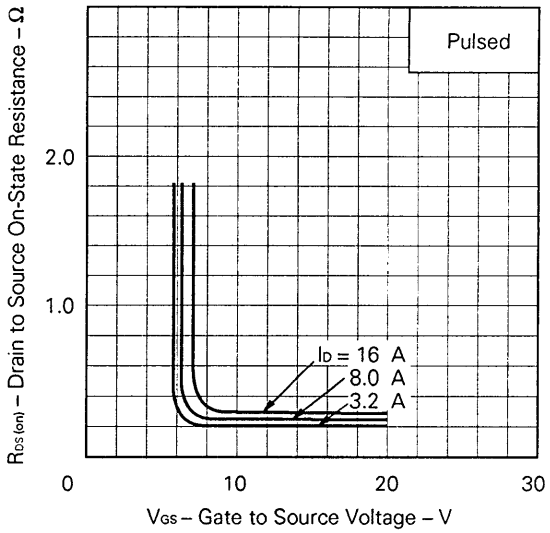
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



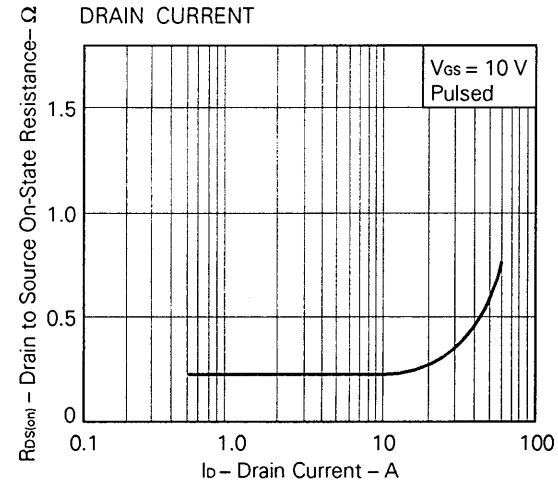
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



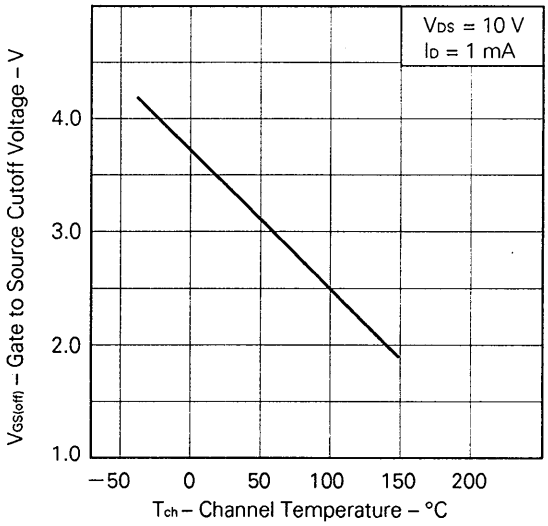
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



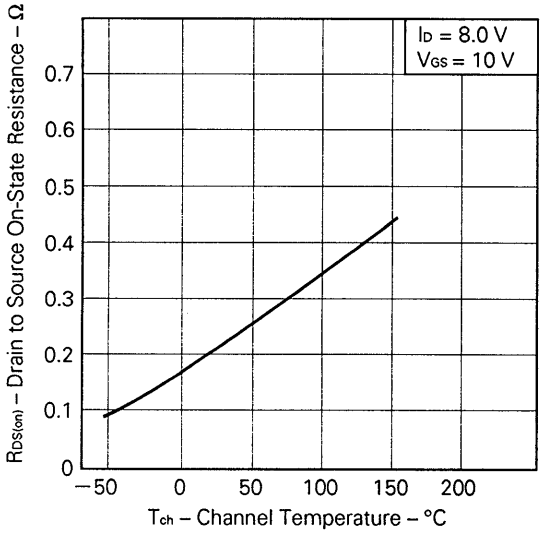
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



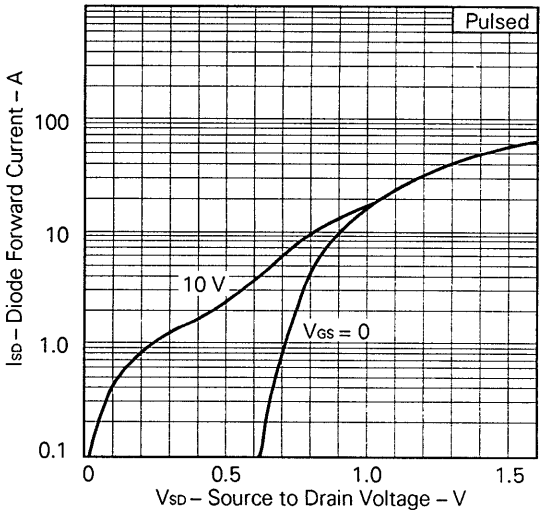
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



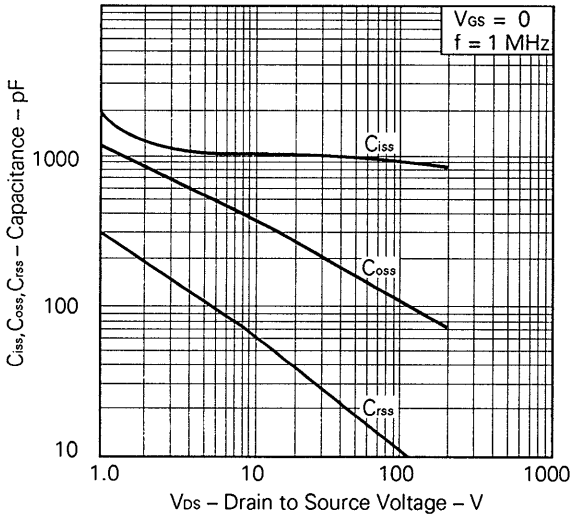
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



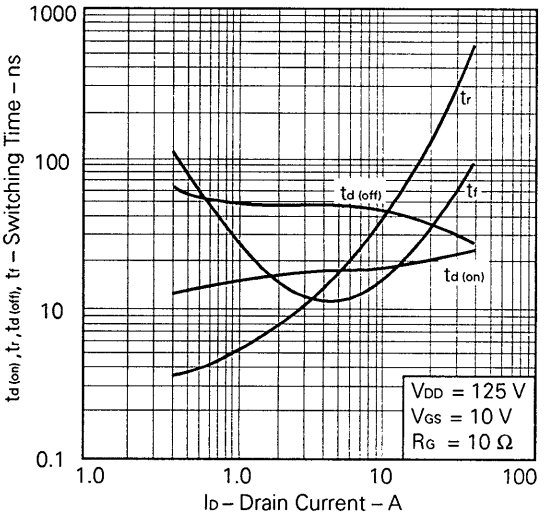
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



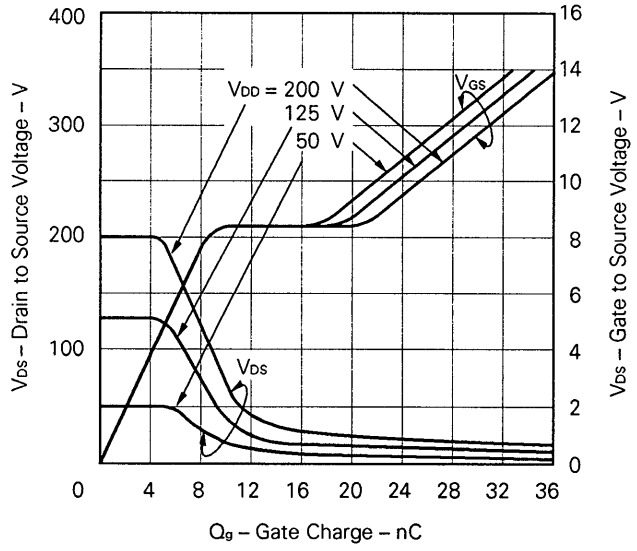
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



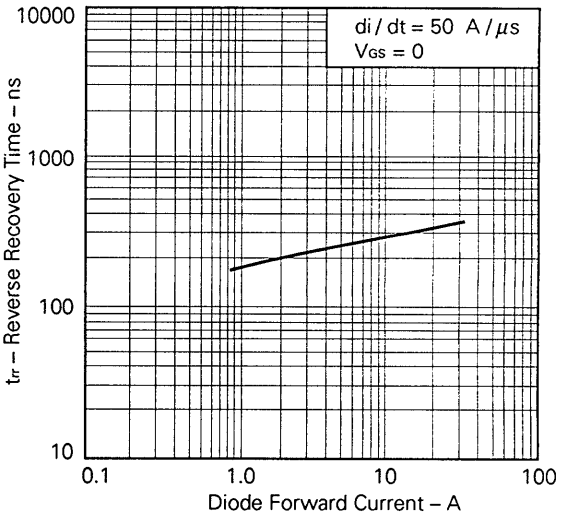
SWITCHING CHARACTERISTICS



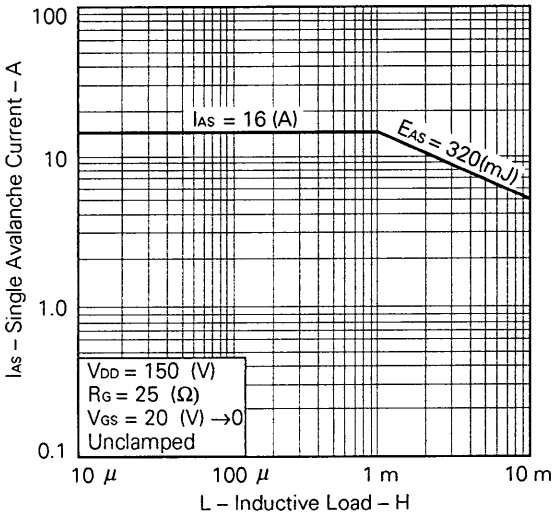
DYNAMIC INPUT/ OUTPUT CHARACTERISTICS



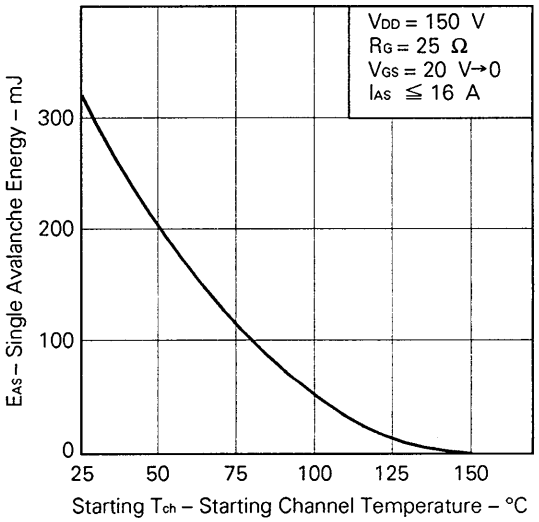
REVERSE RECOVERY TIME vs. REVERSE DRAIN CURRENT



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY vs.
STARTING CHENNEL TEMPERATURE



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