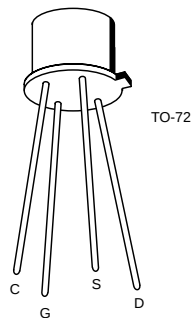


FEATURES

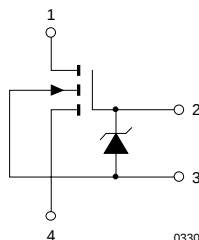
- Low I_{GSS}
- Integrated Zener Clamp for Gate Protection

PIN CONFIGURATION



1003Z

DEVICE SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise specified)

Drain to Source Voltage	30V
Gate to Drain Voltage	30V
Drain Current	50mA
Gate Zener Current	$\pm 0.1\text{mA}$
Storage Temperature Range	-65°C to $+200^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Lead Temperature (Soldering, 10sec)	$+300^\circ\text{C}$
Power Dissipation	225mW
Derate above 25°C	2.2mW/ $^\circ\text{C}$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

Part	Package	Temperature Range
M116	Hermetic TO-72	-55°C to $+125^\circ\text{C}$
XM116	Sorted Chips in Carriers	-55°C to $+125^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ and $V_{BS} = 0$ unless otherwise specified)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
$r_{DS(on)}$	Drain Source ON Resistance		100 200	Ω	$V_{GS} = 20\text{V}, I_D = 100\mu\text{A}$ $V_{GS} = 10\text{V}, I_D = 100\mu\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	1	5		$V_{GS} = V_{DS}, I_D = 10\mu\text{A}$
BV_{DSS}	Drain-Source Breakdown Voltage	30			$I_D = 1\mu\text{A}, V_{GS} = 0$
BV_{SDS}	Source-Drain Breakdown Voltage	30			$I_S = 1\mu\text{A}, V_{GD} = V_{BD} = 0$
BV_{GBS}	Gate-Body Breakdown Voltage	30	60		$I_G = 10\mu\text{A}, V_{SB} = V_{DB} = 0$
$I_{D(OFF)}$	Drain Cutoff Current		10	nA	$V_{DS} = 20\text{V}, V_{GS} = 0$
$I_{S(OFF)}$	Source Cutoff Current		10		$V_{SD} = 20\text{V}, V_{GD} = V_{BD} = 0$
I_{GSS}	Gate-Body Leakage		100	pA	$V_{GS} = 20\text{V}, V_{DS} = 0$
C_{gs}	Gate-Source (Note 1)		2.5		$V_{GB} = V_{DB} = V_{SB} = 0, f = 1\text{MHz}$ Body Guarded
C_{gd}	Gate-Drain Capacitance (Note 1)		2.5		
C_{db}	Drain-Body Capacitance (Note 1)		7		$V_{GB} = 0, V_{DB} = 10\text{V}, f = 1\text{MHz}$
C_{iss}	Input Capacitance (Note 1)		10		$V_{GB} = 0, V_{DB} = 10\text{V}, V_{BS} = 0, f = 1\text{MHz}$

NOTE 1: For design reference only, not 100% tested.