

**700-BIT (50-WORD BY 14-BIT) ELECTRICALLY ALTERABLE ROM**

**DESCRIPTION**

The M58653P is a serial input/output 700 bit electrically erasable and reprogrammable ROM organized as 50 words of 14 bits, and fabricated using MNOS technology. Data and addresses are transferred serially via a one-bit bidirectional bus.

**FEATURES**

- Word-by-word electrically alterable
- Non-volatile data storage . . . . . 10 years (min)
- Write/erase time . . . . . 20ms/word
- Typical power supply voltages . . . . . -30V, +5V
- Number of erase-write cycles . . . . . 10<sup>5</sup> times (min)
- Number of read access unrefreshed. . . 10<sup>9</sup> times (min)
- 5V I/O interface

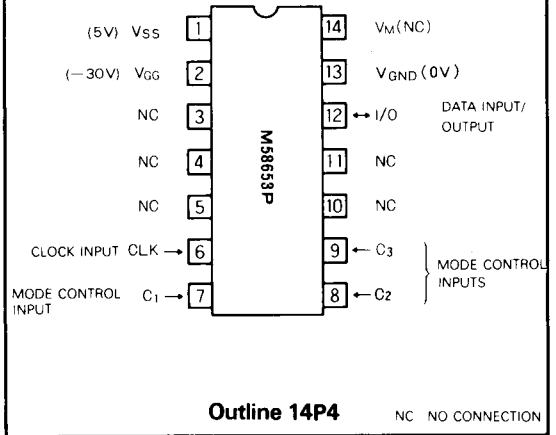
**APPLICATION**

Non-volatile channel memories for electronic tuning systems and field-reprogrammable read-only memory systems

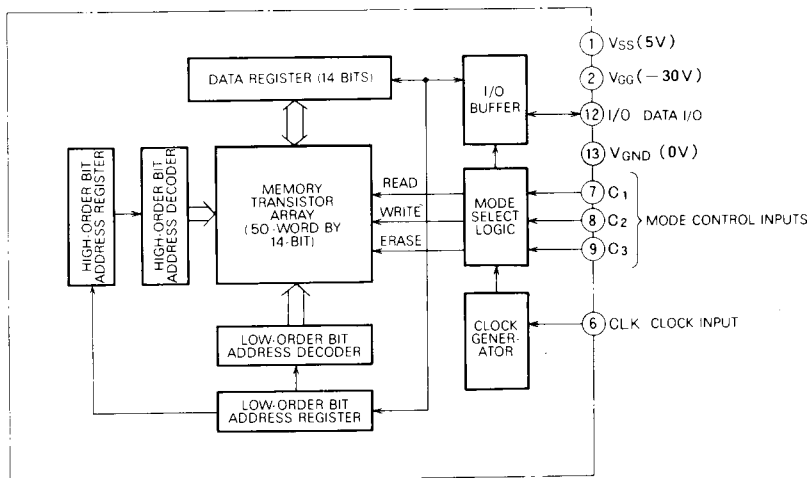
**FUNCTION**

The address is designated by one of five and one of ten coded digits. Seven modes—accept address, accept data, shift data output, erase, write, read, and standby—are all selected by a 3-bit code applied to C<sub>1</sub>, C<sub>2</sub>, and C<sub>3</sub>. Data is stored by internal negative writing pulses that selectively tunnel charges into the SiO<sub>2</sub>-Si<sub>3</sub>N<sub>4</sub> interface of the gate insulators of the MNOS memory transistors.

**PIN CONFIGURATION (TOP VIEW)**



**BLOCK DIAGRAM**



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**PIN DESCRIPTION**

Pin	Name	Functions
I/O	I/O	In the accept address and accept data modes, used for input In the shift data output mode, used for output In the standby, read, erase and write modes, this pin is in a floating state
V <sub>M</sub>	Test	Used for testing purposes only. It should be left unconnected during normal operation.
V <sub>SS</sub>	Chip substrate voltage	Normally connected to +5V
V <sub>GG</sub>	Power supply voltage	Normally connected to -30V
CLK	Clock input	14kHz timing reference. Required for all operating modes. High-level input is possible during standby mode.
C <sub>1</sub> - C <sub>3</sub>	Mode control input	Used to select the operation mode.
V <sub>GND</sub>	Ground voltage	Connected to ground (0V)

**OPERATION MODES**

C <sub>1</sub>	C <sub>2</sub>	C <sub>3</sub>	Functions
H	H	H	Standby mode. The contents of the address registers and the data register remain unchanged. The output buffer is held in the floating state.
H	H	L	Not used.
H	L	H	Erase mode. The word stored at the addressed location is erased. The data bits after erasing are all low-level.
H	L	L	Accept address mode. Data presented at the I/O pin is shifted into the address registers one bit with each clock pulse. The address is designated by one of five and one of ten coded digits.
L	H	H	Read mode. The addressed word is read from the memory into the data register.
L	H	L	Shift data output mode. The output driver is enabled and the contents of the data register are shifted to the I/O pin one bit with each clock pulse.
L	L	H	Write mode. The data contained in the data register is written into the location designated by the address registers.
L	L	L	Accept data mode. The data register accepts serial data from the I/O pin one bit with each clock pulse. The address registers remain unchanged.

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>GG</sub>	Supply voltage	With respect to V <sub>SS</sub>	0.3 ~ -40	V
V <sub>I</sub>	Input voltage		0.3 ~ -20	V
V <sub>O</sub>	Output voltage		0.3 ~ -20	V
T <sub>stg</sub>	Storage temperature		-40 ~ 125	°C
T <sub>opr</sub>	Operating temperature		-10 ~ 70	°C

RECOMMENDED OPERATING CONDITIONS (T<sub>a</sub> = -10 ~ 70°C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V <sub>GG</sub> -V <sub>SS</sub>	Supply voltage	-32.2	-35	-37.8	V
V <sub>SS</sub> -V <sub>GND</sub>	Supply voltage	4.75	5	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>SS</sub> -1		V <sub>SS</sub> +0.3	V
V <sub>IL</sub>	Low-level input voltage	V <sub>SS</sub> -6.5		V <sub>SS</sub> -4.25	V

Note 1:  
The order of V<sub>SS</sub> V<sub>GG</sub> with on or off.  
With on, V<sub>GG</sub> is turned on after V<sub>SS</sub> is done.  
With off, V<sub>SS</sub> is turned off after V<sub>GG</sub> is done.

ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = -10 ~ 70°C, V<sub>GG</sub>-V<sub>SS</sub> = -35V ± 8%, V<sub>SS</sub>-V<sub>GND</sub> = 5V ± 5%, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V <sub>IH</sub>	High-level input voltage		V <sub>SS</sub> -1		V <sub>SS</sub> +0.3	V
V <sub>IL</sub>	Low-level input voltage		V <sub>SS</sub> -6.5		V <sub>SS</sub> -4.25	V
I <sub>IL</sub>	Low-level input current	V <sub>I</sub> -V <sub>SS</sub> = -6.5V			± 10	μA
I <sub>OZL</sub>	Off-state output current, low-level voltage applied	V <sub>O</sub> -V <sub>SS</sub> = -6.5V			± 10	μA
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -200μA	V <sub>SS</sub> -1			V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 10μA			V <sub>GND</sub> +0.5	V
I <sub>GG</sub>	Supply current from V <sub>GG</sub>	I <sub>O</sub> = 0μA		5.5	8.8	mA

Note 2. Typical values are at T<sub>a</sub>=25°C and nominal supply voltage.

TIMING REQUIREMENTS (T<sub>a</sub> = -10 ~ 70°C, V<sub>GG</sub>-V<sub>SS</sub> = -35V ± 8%, V<sub>SS</sub>-V<sub>GND</sub> = 5V ± 5%, unless otherwise noted.)

Symbol	Parameter	Alternative symbols	Test conditions	Limits			Unit
				Min	Typ	Max	
f(φ)	Clock frequency	fφ		10	14	17	kHz
D(φ)	Clock duty cycle	Dφ		30	50	55	%
t <sub>w</sub> (W)	Write time	t <sub>w</sub>		16	20	24	ms
t <sub>w</sub> (E)	Erase time	t <sub>e</sub>		16	20	24	ms
t <sub>r</sub> , t <sub>f</sub>	Risetime, fall time	t <sub>r</sub> , t <sub>f</sub>				1	μs
t <sub>su</sub> (c-φ)	Control setup time before the fall of the clock pulse	t <sub>CS</sub>		0			ns
t <sub>h</sub> (φ-c)	Control hold time after the rise of the clock pulse	t <sub>CH</sub>		0			ns

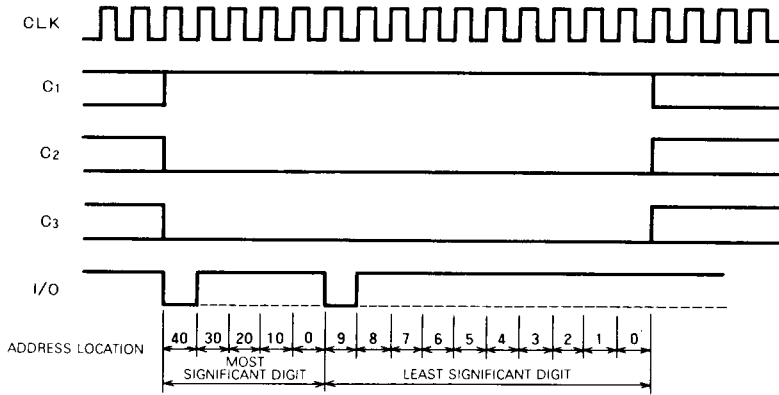
SWITCHING CHARACTERISTICS (T<sub>a</sub> = -10 ~ 70°C, V<sub>GG</sub> = -35V ± 8%, unless otherwise noted.)

Symbol	Parameter	Alternative symbols	Test conditions	Limits			Unit
				Min	Typ	Max	
t <sub>a</sub> (c)	Read access time	t <sub>pw</sub>	C <sub>L</sub> = 100 pF, V <sub>OH</sub> = V <sub>SS</sub> - 2V, V <sub>OL</sub> = V <sub>GND</sub> + 1.5V			20	μs
t <sub>s</sub>	Unpowered nonvolatile data retention time	T <sub>S</sub>	N <sub>EW</sub> = 10 <sup>4</sup> , t <sub>w</sub> (W) = 20ms, t <sub>w</sub> (E) = 20ms	10			Year
		T <sub>S</sub>	N <sub>EW</sub> = 10 <sup>5</sup> , t <sub>w</sub> (W) = 20ms, t <sub>w</sub> (E) = 20ms	1			
N <sub>EW</sub>	Number of erase/write cycles	N <sub>W</sub>		10 <sup>5</sup>			Times
N <sub>RA</sub>	Number of read access unrefreshed	N <sub>RA</sub>		10 <sup>9</sup>			Times
t <sub>dv</sub>	Data valid time	t <sub>pw</sub>				20	μs

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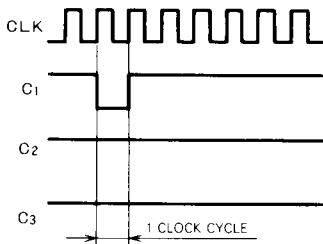
TIMING DIAGRAM

Accept Address Mode

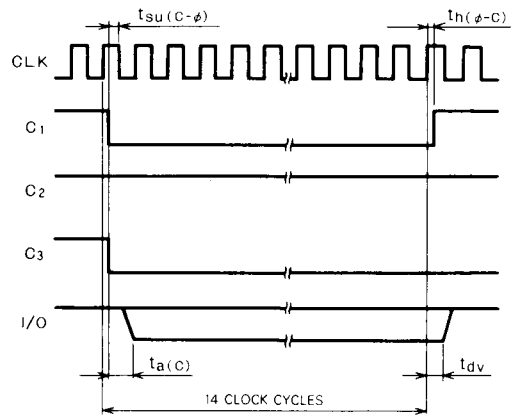


Note 3: The address is designated by one-of-five and one-of-ten coded digits. The figure shows designation of the address 49.

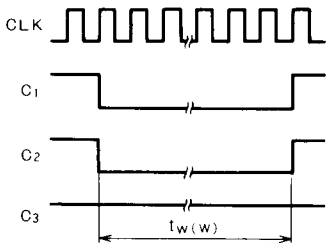
Read Mode



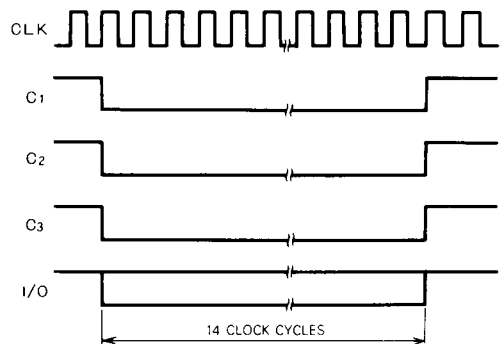
Shift Data Output Mode



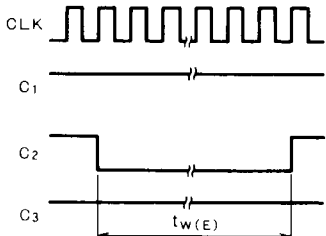
Write Mode



Accept Data Mode

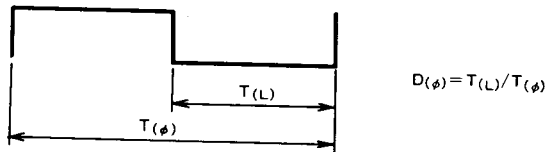


Erase Mode



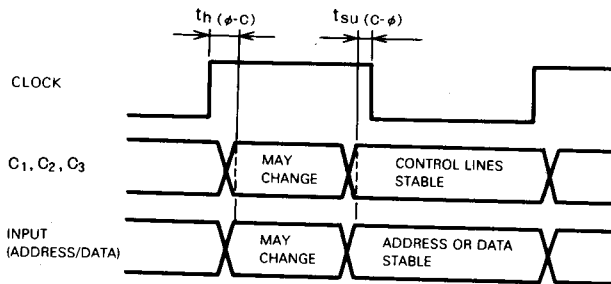
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The definition of clock duty cycle,  $D(\phi)$

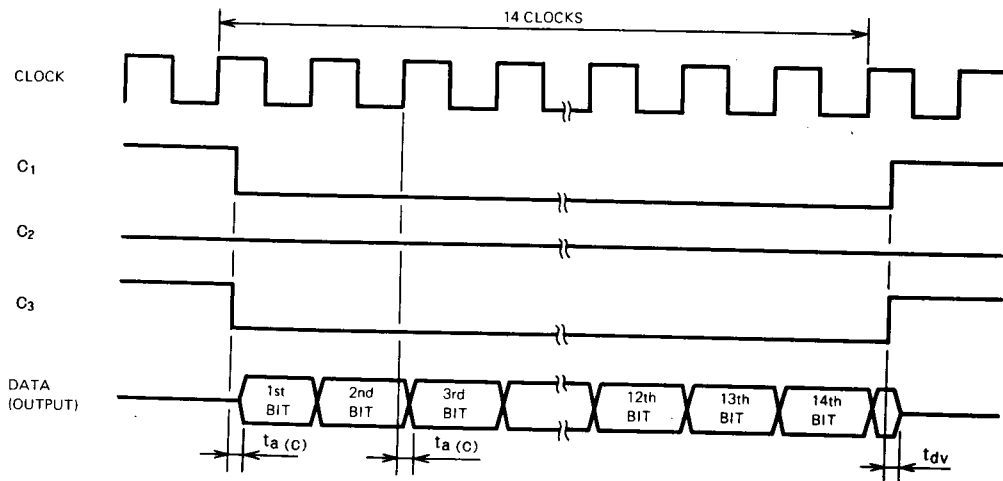


**Timing of data input and mode control inputs**

Mode control inputs,  $C_1$ ,  $C_2$ ,  $C_3$  and input signal may change, when clock is 'H' level.



**Timing of data output**



The 1st bit of output data is output after access time of  $t_a(C)$  from the mode control transition. And other bits are output after  $t_a(C)$  from positive edge of clock.

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Operating sequential flow

