

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC33689

Product Preview

System Basis Chip with
LIN transceiver

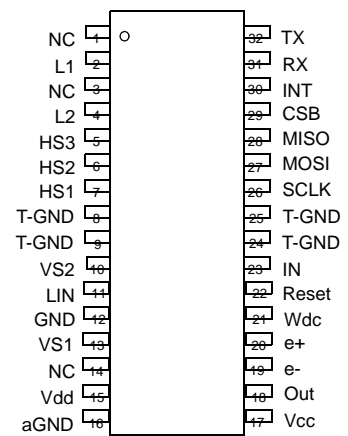
LIN System basis chip

SILICON MONOLITHIC
INTEGRATED CIRCUIT

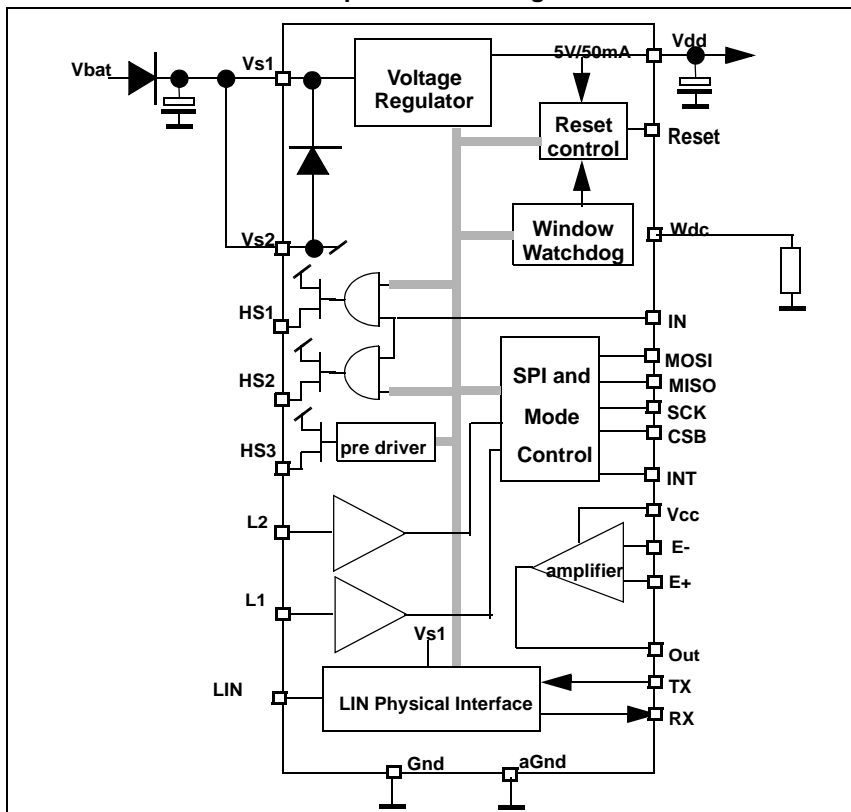
The LIN SBC is a monolithic integrated circuit combining many functions frequently used by automotive LIN distributed slave nodes. It incorporates:

- Single voltage regulator with low power modes
 - LIN physical interface.
 - Wake up inputs.
 - Triple high side driver
 - Current sense op amp
- Vdd: Low drop voltage regulator, current limitation, over temperature detection, monitoring and reset function, current capability 50mA.
 - Programmable window watchdog
 - Three operational modes (normal, stop and sleep modes)
 - Low current consumption in sleep and stop modes
 - LIN physical interface compatible with LIN standard.
 - Two external high voltage wake-up inputs
 - Dual high side switches, relay driver capability, internal clamp, PWM capability.
 - Single low current high side switch, 50mA capability for switch bias and hall sensor supply
 - Current sense amplifier
 - Nominal DC operating voltage from 5.5 to 27V
 - 40V maximum transient voltage
 - Wake up capabilities (wake up inputs, LIN interface)

Pin out SO32WB fine pitch



Simplified Block Diagram



ORDERING INFORMATION

| Device | Operating Temperature Range | Package |
|---------------|-------------------------------|---------|
| MC33689DWB/R2 | T _A = -40 to 125°C | SO-32 |

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1 MAXIMUM RATINGS

| Ratings | Symbol | Min | Typ | Max | Unit |
|---------|--------|-----|-----|-----|------|
|---------|--------|-----|-----|-----|------|

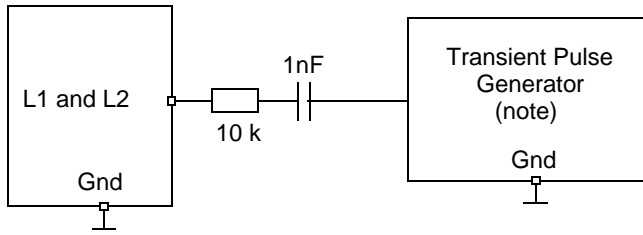
ELECTRICAL RATINGS

| | | | | | |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|--------------------|--------------------|-------------|--------|
| Supply Voltage at Vs1 and Vs2 - Continuous voltage - Transient voltage (Load dump) | Vsupdc Vsuptr | -0.3 | | 27 40 | V |
| Supply Voltage Vdd and Vcc | Vdd | -0.3 | | 5.5 | V |
| Logic Inputs: MOSI, SCK, CSB, IN, Tx | Vinlog | - 0.3 | | Vdd+0.3 | V |
| Logic output: MISO, INT, Rx, Reset | Voutlog | - 0.3 | | Vdd+0.3 | V |
| Output current Vdd | Idd | | Internally limited | | A |
| E+, E- input voltage | Ve+- | -0.3 | | 7 | V |
| E+, E- input current | Ie+- | -20 | | 20 | mA |
| Out output voltage | Vout | -0.3 | | Vcc+0.3 | V |
| Out output current | Iout | -20 | | 20 | mA |
| L1 and L2 - DC Input voltage with a 33k resistor - Transient input voltage (according to ISO7637 specification) and with external component (see figure 1 below). | Vlxdc Vlxtr | -18V -100 | | 40 +100 | V V |
| HS1 and HS2 output | Vhs12 | internally clamped | | Vs2+0.3 | V |
| HS3 | Vhs3 | -0.3 | | Vs2+0.3 | V |
| LIN - DC voltage Transient input voltage (according to ISO7637 specification) and with external component (see figure 1 below). | Vbusdc Vbustr | -18 -150 | | +40 +100 | V |
| ESD voltage (HBM 100pF, 1.5k) (GND, T-GND and aGND pins connected together and configured as ground) - LIN, L1, L2 - All other pins | Vesdh | -4 -2 | | 4 2 | kV |
| ESD voltage (HBM 100pF, 1.5k) (GND pin configured as ground, T-GND and aGND pins as I/O) - LIN, L1, L2 - All other pins | Vesdh | -4 -2 | | 4 2 | kV |
| ESD voltage (Machine Model) All pins (GND, T-GND and aGND pins connected together and configured as ground) | Vesdm | -200 | | 200 | V |
| ESD voltage (Machine Model) All pins (GND pin configured as ground, T-GND and aGND pins as I/O) | Vesdm | -150 | | 150 | V |

THERMAL RATINGS

| | | | | | |
|----------------------------------------|----------------|------|--|------|------|
| Junction Temperature | T _j | - 40 | | +150 | °C |
| Storage Temperature | T _s | - 55 | | +165 | °C |
| Ambient Temperature (for info only) | T _a | - 40 | | +85 | °C |
| Thermal resistance junction to ambient | Rthj/a | | | 80 | °C/W |

Figure 1. : Transient test pulses for LIN and Wake pins



note: Waveform in accordance to ISO7637 part1, test pulses 1, 2, 3a and 3b.

2 ELECTRICAL CHARACTERISTICS

(V_{s1} and V_{s2} from 5.5V to 18V and T_{amb} from -40°C to 125°C unless otherwise noted)

| Description | Symbol | Characteristics | | | Unit | Conditions |
|-----------------------------------------------|------------------------|-----------------|-------|-------|------|----------------------------------------------------------------------------|
| | | Min | Typ | Max | | |
| Vs1 and Vs2 pins (Device power supply) | | | | | | |
| Nominal DC Voltage range | Vsup | 5.5 | | 18 | V | |
| Input Voltage during Load Dump | VsupLD | | | 40 | V | Load dump situation |
| Input Voltage during jump start | VsupJS | | | 27 | V | Jump start situation (note 1) |
| Supply Current in Normal Mode (note 2) | I _{sup(norm)} | | 5 | 7.5 | mA | I _{out} at V _{dd} =10mA, LIN recessive state |
| Supply Current in Sleep Mode (note 2) | I _{sleep} | | 30 | 40 | uA | V _{dd} off, V _{sup} ≤ 13.5V |
| Supply Current in Stop Mode (note 2) | I _{stop} | | 60 | 75 | uA | V _{dd} ON with I _{out} < 100uA, V _{sup} ≤ 13.5V |
| Supply voltage fall early warning threshold | VSUVew | 5.7 | 6 | 6.6 | V | Normal mode, INT generated, bit VSUV set |
| VSUV flag hysteresis | VSUVhyst | | 1 | | V | guaranteed by design |
| Supply voltage over voltage warning threshold | VSOVw | 18 | 19.25 | 20.50 | V | Normal mode, INT generated, bit VSOV set |
| VSOV flag hysteresis | VSOVhyst | | 220 | | mV | guaranteed by design |

note 1: Device is fully functional. All functions are operating. Over temperature may occur.

note 2: Total current (I_{Vs1}+I_{Vs2}) measured at gnd pins.

Vdd (external 5V output for MCU supply). Specification with external capacitor 2uF < C < 10uF and 200mOhms ≤ ESR ≤ 10 ohm. Normal mode. Capacitor value up to 47uF chemical can be used.

| | | | | | | |
|----------------------------------------------------|---------------------|------|-----|------|----|------------------------------------------------------------------------------|
| Vdd Output Voltage | V _{ddout} | 4.75 | 5 | 5.25 | V | I _{dd} from 2 to 50mA 5.5V < V _{sup} < 27V |
| Dropout Voltage (note 1) | V _{dddrop} | | 100 | 200 | mV | I _{dd} = 50mA (note 1) V _{sup} > 4.5V |
| I _{dd} output current limitation (note 2) | I _{dd} | 50 | 110 | 200 | mA | Internally limited |
| Over temperature pre warning (junction) | T _{pre} | 120 | 135 | 160 | °C | Normal mode, INT generated, Bit V _{ddT} set guaranteed by design |
| Thermal Shutdown (junction) | T _{sd} | 155 | 170 | | °C | Normal mode guaranteed by design |
| Temperature threshold difference | | 20 | 30 | 45 | °C | Normal mode (T _{sd} -T _{pre}) guaranteed by design |
| V _{sup} range for Reset Active | V _{supr} | 3.5 | | | V | 0.5 < V _{dd} < V _{dd} (R _{st} -th1) |
| Line Regulation | LR | | 20 | 150 | mV | 5.5V < V _{sup} < 27V, I _{dd} = 10mA |
| Load Regulation | LD | | 40 | 150 | mV | 1mA < I _{dd} < 50mA |

note 1: measured when voltage has dropped 100mV below its nominal value.

note 2: total V_{dd} regulator current. A 5mA current for operational amplifier operation is included. Digital output supplied from V_{dd}.

Vdd: in Stop mode

| | | | | | | |
|---------------------------------------------|---------------------|------|------|------|----|------------------------------------------------------|
| Vdd Output Voltage (note 1) | V _{ddstop} | 4.75 | 5.00 | 5.25 | V | I _{dd} ≤ 2mA |
| I _{dd} current capability (note 2) | I _{dds} | 4 | 8 | 14 | mA | Stop mode |
| Line regulation | LR-s | | 10 | 100 | mV | 5.5V < V _{sup} < 27V, I _{dd} = 2mA |
| Load regulation | LD-s | | 40 | 150 | mV | 1mA < I _{dd} < 5mA |

note 1: when switching from Normal mode to Stop mode, or from Stop mode to Normal mode the output voltage can varies within the output voltage specification.

note 2: when I_{dd} is above I_{dds} device enters reset mode

Reset: normal and stop modes (output pin only)

| | | | | | | |
|--------------------------------------------------|----------------------|------|------|----------------------|----|---------------------------------------|
| Reset threshold | R _{st} -th1 | 4.50 | 4.68 | V _{dd} -0.2 | V | |
| High Level Output current | I _{oh} | | -250 | | μA | V _{out} > 0.7V _{dd} |
| Low Level Output Voltage (I _o =1.5mA) | V _{ol} | 0 | | 0.9 | V | 4.5V < V _{sup} < 27V |

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MC33689

(V_{s1} and V_{s2} from 5.5V to 18V and T_{amb} from -40°C to 125°C unless otherwise noted)

| Description | Symbol | Characteristics | | | Unit | Conditions |
|-------------------------------|-----------|-----------------|-----|------|------|-----------------------------------------------------------|
| | | Min | Typ | Max | | |
| Reset pull down current | lpdw | 1.5 | | 8 | mA | Internally limited. $V_{dd} < 4V$, $V_{reset} = 4.6V$ |
| Reset Duration after Vdd High | reset-dur | 0.65 | 1 | 1.35 | ms | |

IN: input

| | | | | | | |
|--------------------------|----------|--------|--|---------|---------|-----------------------|
| High Level Input Voltage | V_{ih} | 0.7Vdd | | Vdd+0.3 | V | |
| Low Level Input Voltage | V_{il} | -0.3 | | 0.3Vdd | V | |
| Input Current | lin | -10 | | 10 | μA | $0 < V_{IN} < V_{dd}$ |

MISO: SPI output

| | | | | | | |
|--------------------------------|----------|---------|--|-----|---------|--------------------------|
| Low Level Output Voltage | V_{ol} | 0 | | 1.0 | V | I out = 1.5mA |
| High Level Output Voltage | V_{oh} | Vdd-0.9 | | Vdd | V | I out = -250uA |
| Tristated MISO Leakage Current | | -2 | | +2 | μA | $0V < V_{miso} < V_{dd}$ |

MOSI, SCLK, CSB: SPI input

| | | | | | | |
|----------------------------|----------|--------|--|---------|---------|-----------------------|
| High Level Input Voltage | V_{ih} | 0.7Vdd | | Vdd+0.3 | | |
| Low Level Input Voltage | V_{il} | -0.3 | | 0.3Vdd | V | |
| CSB Pull up current source | lih | -100 | | -20 | μA | V_i 1V to 3.5V |
| MOSI, SCK Input Current | lin | -10 | | 10 | μA | $0 < V_{IN} < V_{dd}$ |

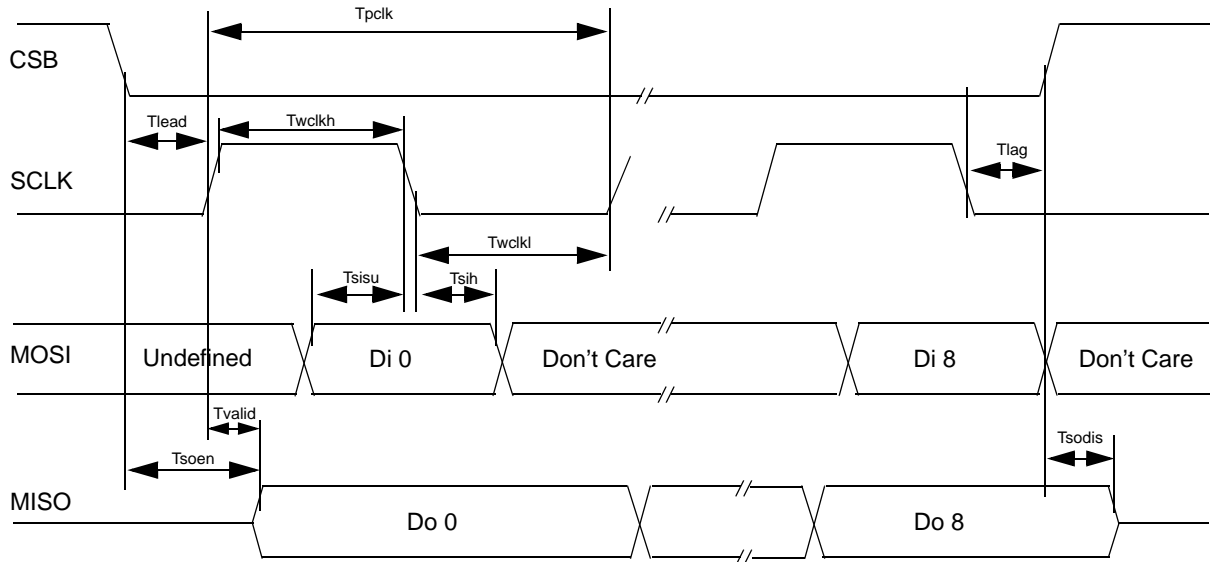
SPI: DIGITAL INTERFACE TIMING

| | | | | | | |
|----------------------------------------------------------------------------------------------|---------------------------|------|----|----------|-----|------------------------------------------------------------------------|
| SPI operation frequency | Freq | 0.25 | | 4 | MHz | |
| SCLK Clock Period | t_{pCLK} | 250 | | N/A | ns | |
| SCLK Clock High Time | t_{wSCLKH} | 125 | | N/A | ns | |
| SCLK Clock Low Time | t_{wSCLKL} | 125 | | N/A | ns | |
| Falling Edge of CS to Rising Edge of SCLK | t_{lead} | 100 | | N/A | ns | |
| Falling Edge of SCLK to CS Rising Edge | t_{lag} | 100 | | N/A | ns | |
| MOSI to Falling Edge of SCLK | t_{SISU} | 40 | | N/A | ns | |
| Falling Edge of SCLK to MOSI | t_{SIH} | 40 | | N/A | ns | |
| MISO Rise Time (CL = 220pF) | t_{rSO} | | 25 | 50 | ns | guaranteed by design |
| MISO Fall Time (CL = 220pF) | t_{fSO} | | 25 | 50 | ns | guaranteed by design |
| Time from Falling or Rising Edges of CS to: - MISO Low Impedance - MISO High Impedance | t_{SOEN} t_{SODIS} | 0 | | 50 50 | ns | guaranteed by design |
| Time from Rising Edge of SCLK to MISO Data Valid | t_{valid} | 0 | | 50 | ns | $0.2 V_1 = <MISO> = 0.8V_1$, $C_L = 100pF$ guaranteed by design |

(V_{S1} and V_{S2} from 5.5V to 18V and T_{amb} from -40°C to 125°C unless otherwise noted)

| Description | Symbol | Characteristics | | | Unit | Conditions |
|-------------|--------|-----------------|-----|-----|------|------------|
| | | Min | Typ | Max | | |

Figure 2. SPI Timing characteristic



Note:

Incoming data at MOSI pin is sampled by the SBC at SCLK falling edge.
Outcoming data at MISO pin is set by the SBC at SCLK rising edge (after Tvalid delay time)

INT: output pin

| | | | | | | |
|--------------------------------------------|-----|---------|--|-----|---|--|
| Low Level Output Voltage ($I_O=1.5mA$) | Vol | 0 | | 0.9 | V | |
| High Level Output Voltage ($I_O=-250uA$) | Voh | Vdd-0.9 | | Vdd | | |

WDC: window watchdog configuration pin

| | | | | | | |
|----------------------------------------------------------|---------|-----|--------|-----|-------|-------------------------------------|
| External resistor range | Rext | 10 | | 100 | kohms | |
| Watchdog period accuracy with external resistor | Wdcacc | -15 | | 15 | % | Excluding resistor accuracy. Note 1 |
| Watchdog period with external resistor | Wdp 10 | | 10.558 | | ms | R = 10 kohms. note 1 |
| Watchdog period with external resistor | Wdp 100 | | 99.748 | | ms | R = 100 kohms. note 1 |
| Watchdog period without external resistor, Conf pin open | PWdoff | 97 | 150 | 205 | ms | Normal mode |

note 1: watchdog timing period calculation formula: $Twd = 0.991 * R + 0.648$ (R in kohms and Twd in ms).

HS1 and HS2: High side output pin

| | | | | | | |
|---------------------------------------------------|--------|-----|-----|-----|------|------------------|
| Rdson at $T_a=25^\circ C$, and $I_{out} -150mA$ | Ron25 | | 2 | 2.5 | Ohms | $V_{sup}>9V$ |
| Rdson at $T_a=125^\circ C$, and $I_{out} -150mA$ | Ron125 | | | 4.5 | Ohms | $V_{sup}>9V$ |
| Rdson at $T_a=125^\circ C$, and $I_{out} -120mA$ | Ron3 | | 3 | | Ohms | $5.5<V_{sup}<9V$ |
| Output current limitation | Ilim | 300 | 430 | 600 | mA | |
| Over temperature Shutdown | Ovt | 155 | | 190 | °C | note 1 |
| Leakage current | Ileak | | | 10 | uA | |
| Output Clamp Voltage at $I_{out} = -100mA$ | Vcl | -6 | | | V | |

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(V_{S1} and V_{S2} from 5.5V to 18V and T_{amb} from -40°C to 125°C unless otherwise noted)

| Description | Symbol | Characteristics | | | Unit | Conditions |
|-------------|--------|-----------------|-----|-----|------|------------|
| | | Min | Typ | Max | | |

note 1: when over temperature occurs, switch is turned off and latched off. Flag is set in SPI.

HS3: High side output pin

| | | | | | | |
|------------------------------------------------------------|--------|-----|-----|-----|------|--------------------------|
| Rdson at T _J =25°C, and I _{out} -50mA | Ron25 | | | 7 | Ohms | V _{sup} >9V |
| Rdson at T _a =125°C, and I _{out} -50mA | Ron125 | | | 10 | Ohms | V _{sup} >9V |
| Rdson at T _a =125°C, and I _{out} -30mA | Ron3 | | | 14 | Ohms | 5.5<V _{sup} <9V |
| Output current limitation | Ilim | 60 | 100 | 200 | mA | |
| Over temperature Shutdown | Ovt | 155 | | 190 | °C | note 1 |
| Leakage current | Ileak | | | 10 | uA | |

note 1: when over temperature occurs, switch is turned off and latched off. Flag is set in SPI

SENSE CURRENT AMPLIFIER SECTION:

| | | | | | | |
|--------------------------------|-------------------|------|----|----------------------|------|-----------------------------------------------------|
| Rail to rail input voltage | V _{imc} | -0.1 | | V _{cc} +0.1 | V | |
| Output voltage range | V _{out1} | 0.1 | | V _{cc} -0.1 | V | Output current +- 1mA |
| Output voltage range | V _{out2} | 0.3 | | V _{cc} -0.3 | V | Output current +-5 mA |
| Input bias current | I _b | | | 250 | nA | |
| Input offset current | I _o | -100 | | 100 | nA | |
| Input offset voltage | V _{io} | -15 | | 15 | mV | |
| Supply voltage rejection ratio | svr | 60 | | | dB | Guaranteed by design |
| Common mode rejection ratio | cmr | 70 | | | dB | Guaranteed by design |
| Gain bandwidth | GBP | 1 | | | Mhz | Guaranteed by design |
| Slew rate | SR | 0.5 | | | V/us | |
| Phase margin | PHMO | 40 | | | ° | For gain=1,load 100pF//5kohms. Guaranteed by design |
| Open loop gain | OLG | | 85 | | dB | Guaranteed by design |

L1, L2 inputs

| | | | | | | |
|------------------------------|-------------------|-----|-----|-----|----|-----------------------------------------------------------------------------------|
| Negative Switching Threshold | V _{thn} | 2 | 2.5 | 3 | V | 5.5V<V _{sup} <6V 6V<V _{sup} <18V 18V<V _{sup} <27 |
| | | 2.5 | 3 | 3.5 | | |
| | | 2.7 | 3.2 | 3.7 | | |
| Positive Switching Threshold | V _{thp} | 2.7 | 3.3 | 3.8 | V | 5.5V<V _{sup} <6V 6V<V _{sup} <18V 18V<V _{sup} <27 |
| | | 3 | 4 | 4.5 | | |
| | | 3.5 | 4.2 | 4.7 | | |
| Hysteresis | V _{hyst} | 0.5 | | 1.3 | V | 5.5V<V _{sup} <27 |
| Input current | I _{in} | -10 | | 10 | uA | -0.2V < V _{in} < 40V |
| Wake up Filter Time | T _{wuf} | 8 | 20 | 38 | us | Guaranteed by design |

STATE MACHINE TIMING

| | | | | | | |
|-----------------------------------------------------------------------------------------------------------------------|----------------------|-----|-----|-----|----|-----------------------------------------------------------------------------|
| Delay between CSB low to high transition (at end of SPI stop command) and Stop mode activation (Guaranteed by design) | T _{stop-m} | 1.4 | | 5 | us | Minimum Watchdog period No watchdog selected Maximum watchdog period |
| | T _{stop-nw} | 6 | | 30 | us | |
| | T _{stop-M} | 12 | | 50 | us | |
| Interrupt low level duration | T _{int} | 7 | 10 | 13 | us | |
| Internal oscillator frequency accuracy | Osc-f1 | -35 | | 35 | % | All modes, for info only |
| Normal request mode time out | NRtout | 97 | 150 | 205 | ms | Normal request mode |
| Delay between SPI command and HS1, HS2 or HS3 turn on (note 1, 2) | T _{s-HSon} | | | 20 | us | Normal mode V _{sup} >9V, V _{hs} >= 0.2 V _{s1} |
| Delay between SPI command and HS1, HS2 or HS3 turn off (note 1, 2) | T _{s-HSoff} | | | 20 | us | Normal mode V _{sup} >9V, V _{hs} <= 0.8 V _{s1} |
| Delay between Normal Request and Normal mode, after W/D trigger command | T _{s-NR2N} | 6 | 35 | 30 | us | Normal request mode, Guaranteed by design |
| Delay between CSB wake up (CSB low to high) and SBC normal request mode (V _{dd1} on & reset high) | T _{w-csb} | 15 | 40 | 80 | us | SBC in stop mode |

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(V_{S1} and V_{S2} from 5.5V to 18V and T_{amb} from -40°C to 125°C unless otherwise noted)

| Description | Symbol | Characteristics | | | Unit | Conditions |
|----------------------------------------------------------------------------|-----------|-----------------|-----|-----|------|----------------------------|
| | | Min | Typ | Max | | |
| Delay between CSB wake up (CSB low to high) and first accepted SPI command | Tw-spi | 90 | | N/A | us | SBC in stop mode |
| Delay between INT pulse and 1st SPI command accepted | Ts-1stspi | 30 | | N/A | us | In stop mode after wake up |
| The minimum time between two rising edges on the CSB | T2csb | 15 | | | us | |

note 1: when IN input is set to high, delay starts at falling edge of clock cycle #8 of the SPI command and start of device activation/deactivation. 30mA load on HS switches. Excluding rise or fall time due to external load.

note 2: when IN used to control HS switches, delays measured between IN and HS1 or HS2 on /off. 30mA load on HS switches. Excluding rise or fall time due to external load.

Rx: LIN physical layer output

| | | | | | | |
|---------------------------|-----------------|------|--|------|---|--------------------------|
| Low Level Voltage Output | V _{ol} | 0 | | 0.9 | V | I _{in} ≤ +1.5mA |
| High Level Voltage Output | V _{oh} | 3.75 | | 5.25 | V | I _{out} ≤ 250uA |

Tx: LIN physical layer input

| | | | | | | |
|----------------------------|---------------------|------|-----|-----|----|-------------------|
| Low Level Voltage Input | V _{il} | | | 1.5 | V | |
| High Level Voltage Input | V _{ih} | 3.5 | | | V | |
| Input Threshold Hysteresis | V _{inhyst} | 50 | 550 | 800 | mV | |
| Pull-up Current Source | I _s | -100 | | -20 | uA | 1V < V(Tx) < 3.5V |

LIN: physical layer bus (Voltage Expressed versus V_{sup} Voltage)

| | | | | | | |
|----------------------------------------------------------------------------------|--------------------------|----------------------|-----|---------------------|------------------|-------------------------------------------------------------------------|
| Low Level Dominant Voltage | V _{lin-low} | | | 1.4 | V | external bus pull 500 Ohms |
| High Level Voltage (Tx high, I _{out} = 1uA) | V _{lin-high} | V _{sup-1} | | | V | Recessive state |
| Pull up Resistor to V _{sup} | R _{pu} | 20 | 30 | 47 | kohms | In normal mode. In sleep and stop mode if not turned off by SPI |
| Pull up current source | I _{pu} | | 1.3 | | uA | In sleep and stop mode with 30k disconnected |
| Over current shutdown threshold | I _{ov-cur} | 50 | 75 | 150 | mA | |
| Over current shutdown delay | I _{ov-delay} | | 10 | | us | Guaranteed by design |
| Leakage Current to GND | I _{bus-pas-rec} | 0 | 3 | 20 | uA | Recessive state, V _{sup} 8V to 18V, V _{lin} 8V to 18V |
| Gnd disconnected, V _{gnd} = V _{sup} , V _{Lin} at -18V | I _{bus no gnd} | -1 | | 1 | mA | |
| Leakage Current to GND, V _{sup} Disconnected, V _{Lin} at +18V | I _{bus} | | 1 | 10 | uA | V _{sup} disconnected V _{lin} at +18V |
| Lin Receiver V _{il} (Tx high, Rx low) | Lin-vil | 0 | | 0.4V _{SUP} | | |
| Lin Receiver V _{ih} (Tx high, Rx high) | Lin-vih | 0.6 V _{SUP} | | V _{SUP} | | |
| LIN Receiver Threshold center | Lin-thres | 0.475 | 0.5 | 0.525 | V _{sup} | (Lin-vih - Lin-vil) / 2 |
| LIN Receiver Input Hysteresis | LIN hyst | | | 0.175 | V _{sup} | Lin-vih - Lin-vil |
| LIN wake up threshold | LIN wu | | 0.5 | | V _{sup} | |

LIN physical layer: bus driver timing characteristics for normal slew rate (note 1)

| | | | | | | |
|------------------------------------------------------------------|----------------------|--------|--|----|----|-------------------------------------------------|
| Dominant propagation delay Tx to LIN | t _{dom min} | | | 50 | us | Measurement threshold 58.1% V _{sup} |
| Dominant propagation delay Tx to LIN | t _{dom max} | | | 50 | us | Measurement threshold 28.4% V _{sup} |
| Recessive propagation delay Tx to LIN | t _{rec min} | | | 50 | us | Measurement threshold 42.2% V _{sup} |
| Recessive propagation delay Tx to LIN | t _{rec max} | | | 50 | us | Measurement threshold 74.4% V _{sup} |
| Prop delay symmetry: t _{dom min} - t _{rec max} | dt1 | -10.44 | | - | us | |

| | | | | | | |
|------------------------------------------|-----|---|--|----|----|--|
| Prop delay symmetry: tdom max - trec min | dt2 | - | | 11 | us | |
|------------------------------------------|-----|---|--|----|----|--|

note 1: Vsup from 7V to 18V, bus load R0 and C0 1nF/1k, 6.8nF/660, 10nF/500. Measurement thresholds: 50% of Tx signal to LIN signal threshold defined in the column "condition"

LIN physical layer: bus driver timing characteristics for slow slew rate (note 1)

| | | | | | | |
|------------------------------------------|----------|-----|--|-----|----|-------------------------------------|
| Dominant propagation delay Tx to LIN | tdom min | | | 100 | us | Measurement threshold 61.6% Vsup |
| Dominant propagation delay Tx to LIN | tdom max | | | 100 | us | Measurement threshold 25.1% Vsup |
| Recessive propagation delay Tx to LIN | trec min | | | 100 | us | Measurement threshold 38.9% Vsup |
| Recessive propagation delay Tx to LIN | trec max | | | 100 | us | Measurement threshold 77.8% Vsup |
| Prop delay symmetry: tdom min - trec max | dt1s | -22 | | - | us | |
| Prop delay symmetry: tdom max - trec min | dt2s | - | | 23 | us | |

note 1: Vsup from 7V to 18V, bus load R0 and C0 1nF/1k, 6.8nF/660, 10nF/500. Measurement thresholds: 50% of Tx signal to LIN signal threshold defined in the column "condition"

LIN physical layer: bus driver fast slew rate

| | | | | | | |
|---------------------------------------|------------|--|----|--|------|----------------|
| LIN high slew rate (programming mode) | Dv/Dt fast | | 13 | | V/us | Fast slew rate |
|---------------------------------------|------------|--|----|--|------|----------------|

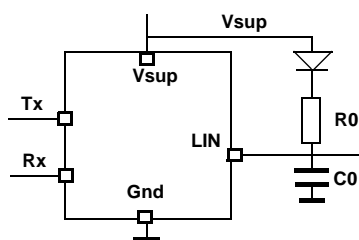
LIN physical layer: receiver characteristics and wake up timings

| | | | | | | |
|--------------------------------------|---------|----|-----|----|----|-----------------------------|
| Receiver dominant propagation delay | TrL | | 3.5 | 6 | us | LIN low to Rx low. Note 2 |
| Receiver recessive propagation delay | TrH | | 3.5 | 6 | us | LIN high to Rx high. note 2 |
| Receiver prop delay symmetry | Tr-sym | -2 | | 2 | us | TrL - TrH |
| Bus wake up deglitcher | TpropWL | 30 | 70 | 90 | us | Sleep and stop mode |
| Bus wake up event reported | Twake | | 20 | | us | Note 3 |

note 2: Measured between LIN signal threshold "Lin-vil" or "Lin-vih" and 50% of Rx signal.

note 3: Twake is typically 2 internal clock cycles after LIN rising edge detected. Ref to "LIN bus wake up behavior" figure. In sleep mode the Vdd rise time is strongly dependant upon the decoupling capacitor at Vdd pin.

Figure 3. Test circuit for timing measurements



R0 and C0: 1k/1nF, 660ohms/6.8nF and 500ohms/10nF

Figure 4. timing measurements for normal slew rate

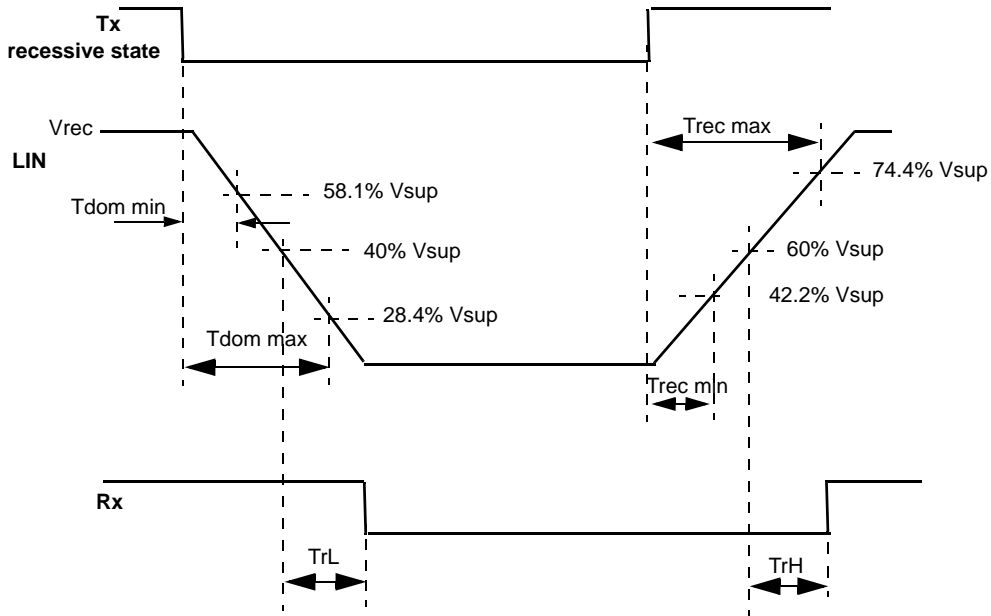


Figure 5. timing measurements for slow slew rate

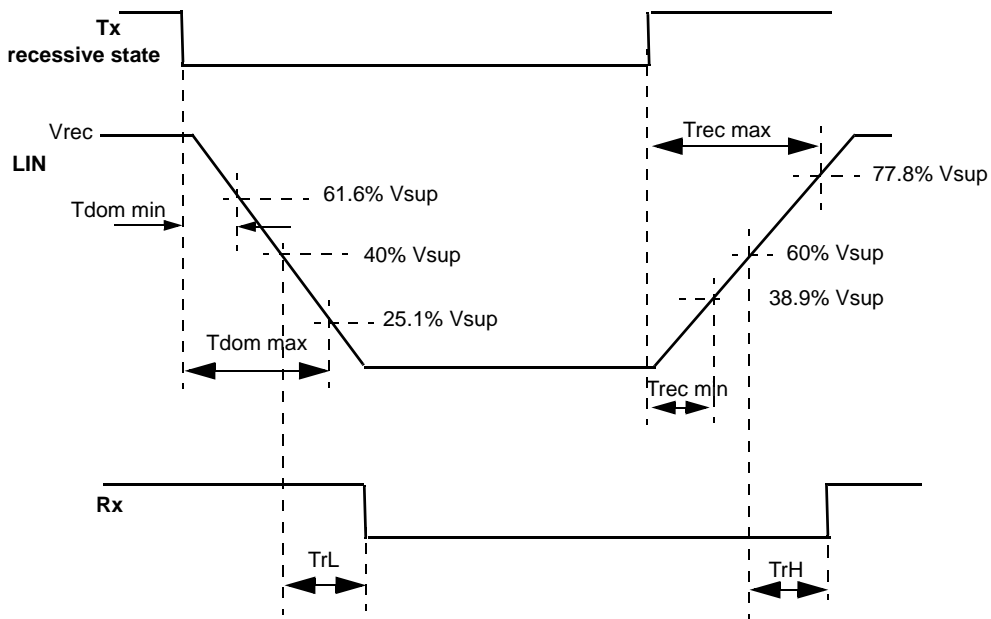
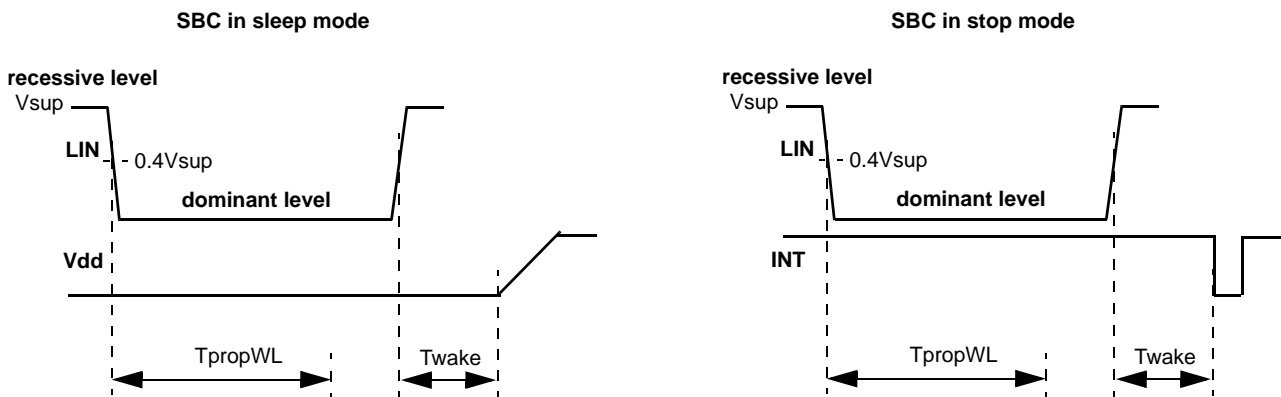
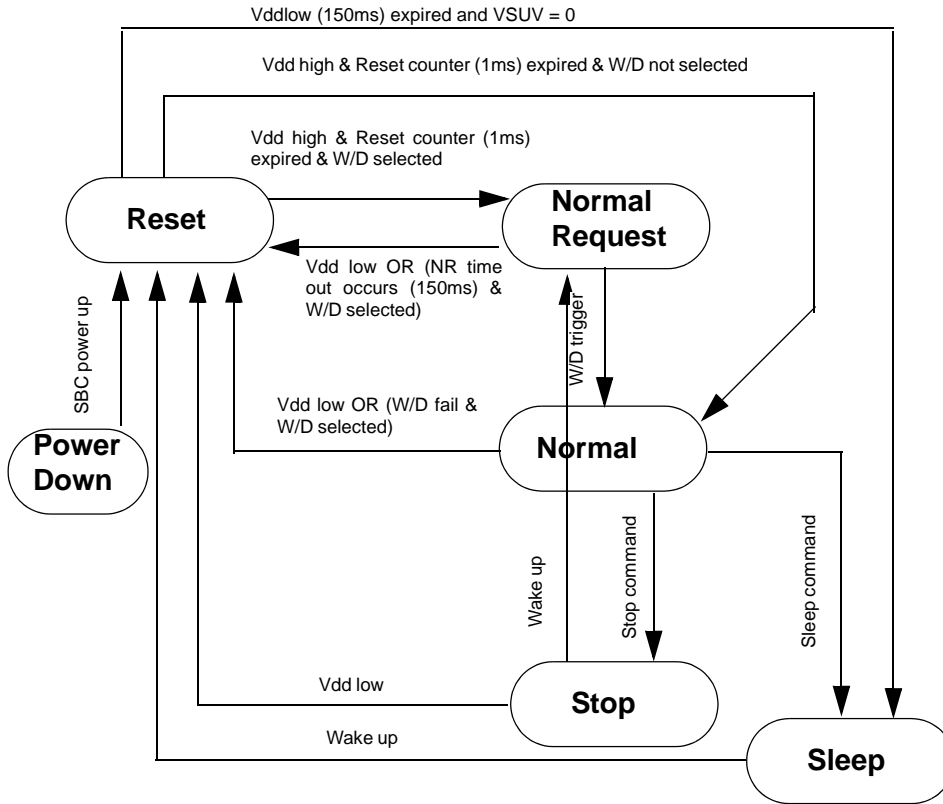


Figure 6. LIN bus wake up behavior



3 STATE MACHINE



W/D selected means: external resistor between Wdc pin and gnd or Wdc pin open.
 W/D not selected means Wdc pin connected to gnd.
 W/D fail means: W/D trigger occurs in closed window or no SPI W/D trigger command.
 Stop command means: SPI stop command.
 Sleep command means: SPI sleep request followed by SPI sleep command.
 Wake up means: L1 or L2 state change or LIN bus wake up or CSB rising edge.

4 PIN DESCRIPTION

| pin name | Pin number | function |
|---------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Vs1 | 13 | Power supply pin. Supply for the voltage regulator and the internal logic. |
| Vs2 | 10 | Power supply pin. Supply for the high side switches. |
| GND | 12 | Electrical ground pin pins for the device. |
| aGND | 16 | Analog ground pin for voltage regulator and sense amplifier. |
| T-GND | 8,9,24,25 | Thermal ground pins for the device |
| Vdd | 15 | 5V regulator output. |
| Reset | 22 | Reset output |
| Wdc | 21 | Configuration pin for the watchdog. A resistor is connected to this pin. The resistor value defines the watchdog period. If the pin is open, the W/D period is fixed (default value). If this pin is tied to gnd the watchdog is disabled. |
| Tx | 32 | Transmitter input of the LIN interface |
| Rx | 31 | Receiver output of the LIN interface |
| LIN | 11 | LIN bus line |
| HS1, HS2, HS3 | 7,6,5 | High side driver output 1, output 2 and output 3 |
| L1, L2 | 2,4 | Wake input 1, wake up input 2 |
| Vcc | 17 | 5V supply input of operational amplifier |
| E- | 19 | Inverted input of the sense amplifier |
| E+ | 20 | Non inverted input of the sense amplifier |
| Out | 18 | Output of the sense amplifier |
| MOSI | 27 | SPI: Master Out Slave In pin |
| MISO | 28 | SPI: Master In Slave Out |
| SCLK | 26 | SPI: Clock input pin |
| CSB | 29 | SPI: Device chip select pin |
| INT | 30 | Interrupt output pin AND wake up event signalling in stop mode. |
| IN | 23 | Direct input for PWM control of High Side switches 1 and 2 |

Table 4-1.

5 GENERAL DESCRIPTION

The LIN SBC is an integrated circuit dedicated to automotive applications. It includes the following functions:

- One full protected voltage regulator with 50mA total output current capability available at Vdd external pin, with under voltage reset function.
- Programmable window watchdog function, INT output
- Wake up from Lx wake input and LIN bus
- LIN physical interface
- Two 150mA high side protected switches PWM capable for relay or lamp drive
- One 50mA high side protected switch for hall sensor or
- Current sense op amp

5.1 Device Supply

The device is supplied from the battery line through the Vs1 and VS2 pins. An external diode is required to protect against negative transients and reverse battery. It can operate from 4.5V and under the jump start condition at 27V DC. Device functionality is guaranteed down to 4.5V at VS1 and VS2 pins. This pin sustains standard automotive voltage conditions such as load dump at 40V.

5.2 Over and under voltage warning.

If the voltage at VS1 exceed 20V typical or falls below 6V typical, the device generates an INT. VSOV or VSUV bits are set in the SPI register. Information is latched until the bit is read AND the fault has disappeared. The interrupt is not maskable.

5.3 LIN physical interface:

The device contains an integrated LIN physical interface.

5.4 L1 and L2 inputs:

These pins are used to sense external switches and to wake up the device from sleep or stop mode. During normal mode the state of these pins can be read through SPI.

5.5 HS1 and HS2:

These are two high side switches to drive load such as relays or lamps. They are protected against over current and over temperature and include internal clamp circuitry for inductive load drive. Control is done through SPI. PWM capability is offered through the IN input.

If PWM control is required, the internal circuitry which drive the internal high side switch is an AND function between the SPI bit HS1 (or HS2) and the IN input. In order to have HS1 on, bit HS1 must be set and IN input must be tied to a micro controller PWM output to generate the PWM control signal (HS1 on when IN is high, HS1 off when IN is low). Same for HS2 output.

If not PWM control is required, IN input must be connected to Vdd or to a high logic level, then the control of HS1 and HS2 is done through SPI only.

If over temperature occurs on any of the 3 switches, the faulty switch is turned off and latched off until HS1 (or HS2 or HS3) bit is set to 1 in the SPI register. The failure is reported through SPI by HSst bit.

5.6 HS3:

This high side switch can be used to drive small lamps, hall sensor or switch pull up resistors. Control is done through SPI

5.7 Sense amplifier:

E+, E- and OUT are the 3 terminations of the current sense amplifier. The amplifier is enable in normal mode only.

5.8 Mode of operation

Mode are controlled by the mode1 and mode 2 bits in the SPI register. 3 modes are available: sleep, stop and normal.

The operation modes and the associated functions are described in the table below.

| Device Mode | Voltage Regulator | Wake up capabilities | Reset output | Watchdog function | HS1 HS2 HS3 | LIN interface | Operational amplifier |
|----------------|-------------------|----------------------|---------------------------------------------------------------------------------------------------|--------------------------------|-------------|----------------------|-----------------------|
| Reset | Vdd: ON | N/A | Low for typ 1ms, then high (if Vdd above threshold) | Disable | OFF | Recessive only | Not active |
| Normal Request | Vdd: ON | N/A | - High. - Active low if Vdd under voltage occurs and if Normal Request timeout (if W/D enable) | 150ms time out if W/D enabled. | ON or OFF | Transmit and Receive | Not active |

Table 5-1.

| Device Mode | Voltage Regulator | Wake up capabilities | Reset output | Watchdog function | HS1 HS2 HS3 | LIN interface | Operational amplifier |
|-------------|------------------------------------------------------------|-----------------------------------|------------------------------------------------------------------------------------|-----------------------|-------------|--------------------------------------|-----------------------|
| Normal | Vdd: ON | N/A | - High. - Active low if Vdd under voltage occurs or if W/D fail (if W/D enable) | Window WD if enabled. | ON or OFF | Transmit and Receive | Active |
| Stop | Vdd ON, limited current capability | LIN and state change on Lx inputs | - Normally high. - Active low if Vdd under voltage occurs | Disable | OFF | Recessive state with Wake capability | Not active |
| Sleep | Vdd OFF, (Set to 5V after wake up to enter Normal request) | LIN and state change on Lx inputs | - Low - Go to high after wake up and Vdd within spec | Disable | OFF | Recessive state with Wake capability | Not active |

Table 5-1.

Sleep and stop mode enter:

To safely enter sleep or stop mode and to ensure that these modes are not entered by noise issue during SPI transmission, a dedicated sequence combining bit controlling the LIN bus and the device mode must be send twice.

Enter sleep mode: first and second SPI commands (with bit D6=1, D7=1, D5 =0 or 1, D1=0 and D0=0) 11x0_0000 must be sent.

Enter stop mode: first and second SPI commands (with bit D6=1, D7=1, D5 =0 or 1, D1=0 and D0=1) 11x0_0001 must be sent.

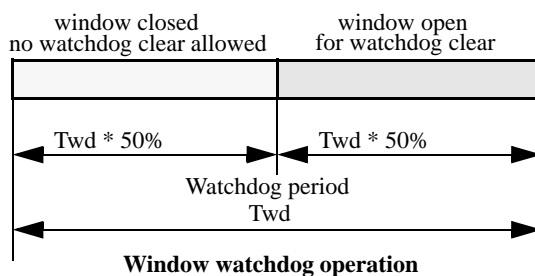
Sleep or stop mode is entered after the second SPI command. D5 bit must be set accordingly.

5.9 Window watchdog.

The window watchdog is configurable using external resistor at Wdc pin. The W/D is cleared through mode1 and mode 2 bit is SPI register. If Wdc pin is left open a fixed watchdog period is selected (typ 150ms). If no watchdog function is required or to disable the watchdog, the Wdc pin must be connected to gnd. The watchdog period is calculated by the following formula:

$$T_{wd} = 0.991 * R + 0.648$$

(with R in kohms and Twd in ms).



Watchdog clear:

The watchdog is cleared by SPI write command with following mode1 and mode2 bits.

| Mode 2 | Mode 1 | Mode |
|--------|--------|----------------------------------|
| 0 | 0 | Sleep mode (note 1) |
| 0 | 1 | Stop mode |
| 1 | 0 | Normal mode + W/D clear (note 2) |
| 1 | 1 | Normal mode |

Note 1: Special SPI command and sequence is implemented in order to avoid to go into sleep or stop mode with a single 8 bit SPI command.

Note 2: When a zero is written to "Mode1" bit while "Mode2" bit is written as a one, after the SPI command is completed "Mode1" bit is set to one and SBC stays in normal mode. In order to set the SBC in sleep mode, both "Mode1" and "Mode2" bits must be written in the same 8 bits SPI command.

The W/D clear on normal request mode (150ms) has no window.

5.10 INT pin:

This pin is used to report fault to the MCU. Int pulse is generated in case of:

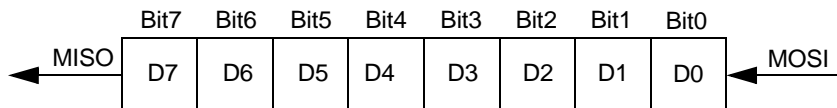
- Vdd regulator temperature pre warning
- high side switch 1, 2 or 3 thermal shutdown
- Vsup over voltage (20V typ)
- Vsup under voltage (6V typ).

If an INT is generated, when the next SPI read operation is performed bit D7 is set to 1. This mean that the bits (D6 to D0) report the interrupt source.

In case of wake up from stop mode, INT is set low in order to signal to the MCU wake up event from L1, L2 or LIN bus.

6 SPI INTERFACE AND REGISTER DESCRIPTION

6.1 Data format description



The SPI is an 8 bits SPI. All bits are data bytes. The MSB is send first. The minimum time between two rising edges on the CSB pin is 15us.

During an SPI communication the state of MISO reports the state of the SBC, at time of CSB high to low transitions. The status flag are latched at CSB high to low transitions.

Following tables describe the SPI register bit meaning, “reset value” and “bit reset condition”.

| | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------------------|---|------------|------------------|--------|----------------------|------------|------------|-------|-------|
| | W | LINSL2 | LINSL1 | LIN-PU | HS3 | HS2 | HS1 | Mode2 | Mode1 |
| | R | INT source | LINWU or LINFAIL | VSOV | VSUV BATFAIL (note1) | VddT | HSst | L2 | L1 |
| Write Reset value | | 0 | 0 | 0 | 0 | 0 | 0 | - | - |
| Write Reset condition | | POR, RESET | POR, RESET | POR | POR, RESET | POR, RESET | POR, RESET | | |

Note 1: The first SPI read, after reset, returns the BATFAIL flag state on bit D4.

D7 signals INT source. After INT occur, D7 read as a “1” means other bits report the INT source. D7 read as a “0” mean no INT occurred and other bit report real time status.

6.2 Write control bits:

6.2.1 Mode control bits:

| Mode 2 | Mode 1 | Description |
|--------|--------|-------------------------|
| 0 | 0 | Sleep mode |
| 0 | 1 | Stop mode |
| 1 | 0 | Normal mode + W/D clear |
| 1 | 1 | Normal mode |

6.2.2 High side switches control bits:

| HS1 | Description | HS2 | Description | HS3 | Description |
|-----|--------------------|-----|--------------------|-----|-------------|
| 0 | HS1 off | 0 | HS2 off | 0 | HS3 off |
| 1 | HS1 on (if IN = 1) | 1 | HS2 on (if IN = 1) | 1 | HS3 on |

6.2.3 LIN pull up termination control bits:

| LIN-PU | Description |
|--------|-------------------------------------------------|
| 0 | 30k pull up connected in sleep and stop mode |
| 1 | 30k pull up disconnected in sleep and stop mode |

6.2.4 LIN slew rate control and device low power mode pre selection:

| LINSL2 | LINSL1 | Description |
|--------|--------|-------------------------------------------------------------------------|
| 0 | 0 | Lin slew rate normal (baud rate up to 20kb/s) |
| 0 | 1 | Lin slew rate slow (baud rate up to 10kb/s) |
| 1 | 0 | Lin slew rate fast (for program download, baud rate up to 100kb/s) |
| 1 | 1 | Low power mode (sleep or stop mode) request, no change in LIN slew rate |

6.3 Read control bits:

6.3.1 Switch input wake up and real time status:

| L2 | Description | L1 | Description |
|----|--------------------------------------------------------------------|----|--------------------------------------------------------------------|
| 0 | L2 input low | 0 | L1 input low |
| 1 | L2 input high or wake up by L2 (first register read after wake up) | 1 | L1 input high or wake up by L1 (first register read after wake up) |

6.3.2 High side switch, voltage regulator and device supply status

| HSst | Description | VddT | Description | VSUV BATFAIL | Description | VSOV | Description |
|------|----------------------------|------|----------------------------------|-----------------|---------------|------|----------------|
| 0 | HS no over temp | 0 | No over temperature | 0 | Vsup above 6V | 0 | Vsup below 19V |
| 1 | HS1,2 or 3 OFF (over temp) | 1 | Vdd over temperature pre warning | 1 | Vsup below 6V | 1 | Vsup above 18V |

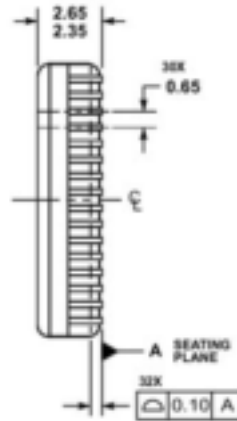
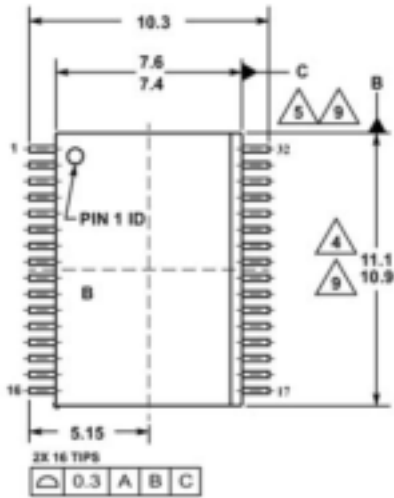
6.3.3 LIN bus status

| LINWU LINFALL | Description |
|------------------|------------------------------------------------------------------|
| 0 | No LIN bus wake up of failure |
| 1 | LIN bus wake up occurred or LIN over current of over temperature |

6.3.4 Interrupt status

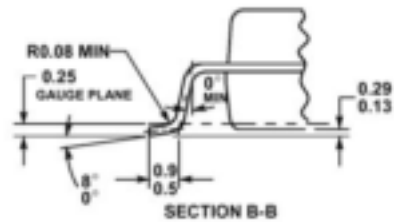
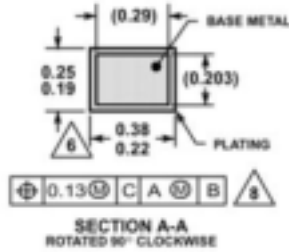
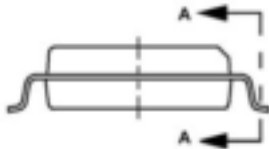
| INT mask | Description |
|----------|--------------------------------------------------------|
| 0 | SPI word read reflects the flag state |
| 1 | SPI word read reflects the interrupt or wake up source |


**DWB SUFFIX
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