

LC67216A



3071

T-49-19-04

CMOS LSI

4-Bit Single Chip Microcomputer

On-Chip FLT Controller, A/D Converter,
Remote Control Signal Detector, 16K-Byte ROM

©3106

Overview

The LC67216A is a 4-bit single chip microcomputer fabricated with CMOS technology. It includes CPU (operational speed: 0.92 μs), ROM (16K bytes), RAM (608 words), AD converter, DA converter (PWM type), Remote control signal receiver, FLT display controller/driver, and horizontal synchronization detect counter in a 64-pin package.

Applications:

- VCR timer, audio timer, DSP amp controller

Features:

- (1) Dedicated hardware: Simpler program and more additional values
 - FLT display controller/driver → Total 28 lines (max.): 20 segments and 16 digits (max.), Various display modes (dimmer, static, and so on), and automatic scanner function (no interrupt processing required)
 - Remote control signal receiver → Continuous pulse (L, H) detection by remote control detection timer and internal high-frequency band noise elimination filter. Recommended for use in products with the 'Association of home electronic appliances' standards.
 - Tone output → Beep sound and melody tone outputs
 - Horizontal synchronization detect counter → Tuner synchronization detectable by an independent 9-bit counter
 - PWM type DA converter → 14-bit DAC output, voltage synthesizer tuner and electronic volume control
- (2) AD converter: Lower cost, more additional values and higher functionality
 - Direct input of various analog signals → AD conversion for level meter and display, S curve detect → no dedicated IC required.
 - key matrix input by resistance division → Better economical space layout, less pins count, reduced harness and improved radiation immunity
- (3) Protection against noise radiation
 - Improved protection against noises from oscillation circuit or FLT driving circuit → Shortened noise protection design process and parts reduction in noise protection mechanism
- (4) Clock standby function
 - Two types of oscillation circuits (4MHz band and 32KHz band) → Battery-backed-up clock application

Hardware Configuration

Applicable to: LC66000 series/LC67000 series microcomputers

Model name	LC66506B/508B/512B/516B	LC66304A/306A/308A	LC67216A
ROM capacity	6K/8K/12K/16K bytes	4K/6K/8K bytes	16K bytes
RAM capacity	512 × 4	512 × 4	608 × 4 (96 × 4 for display)
Packaging	DIP64S, QIP64	DIP42S	DIP64S
High withstand voltage port	Not provided.	Not provided.	Provided (28 lines)
Analog input	Comparator (4 channels) Tri-state input (2 channels)	Comparator (4 channels) Tri-state input (2 channels)	AD converter with an accuracy of 4 bits (8 channels)
Evaluation chip	LC66599	LC66599	LC67999
Remarks	Currently on the market	Currently under development	Currently on the market

7129TA, TS III No. 3106-1/28

LC67216A

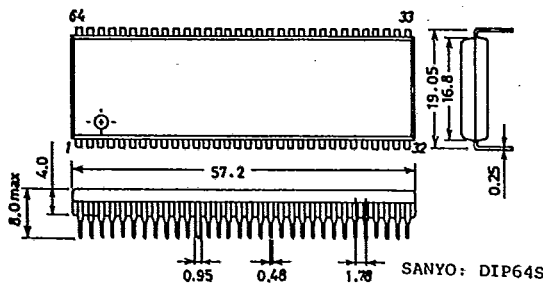
T-49-19-04

Functions:

- (1) Instructions: 116 (upwards compatible with the LC66000 series microcomputers)
- (2) ROM capacity: 16K bytes, RAM capacity: 608x4 words (of the capacity, 96 x 4 words used as the display RAM)
- (3) Minimum cycle time: 0.92 μ s at 4.5V to 6.0V. 7.6 μ s at 3.0V to 6.0V
- (4) System clock selectable by a software \rightarrow Less power dissipation
 - In case of main system clock = 4.19MHz: 0.95, 7.6 or 30.6 μ s
 - In case of sub system clock = 32.768KHz: 61 μ s
- (5) Input/output ports: Total = 53 lines
 - Output ports: 28 lines \rightarrow FLT controller directly drivable
 - Input/output ports: 24 lines \rightarrow LED directly drivable
 - Input port: 1 line
- (6) Interrupt: 11 sources (external interrupt = 4 lines, AC zero cross interrupt = 1 line, timer interrupt = 3 lines, serial input/output interrupt = 2 lines, and key scan interrupt = 1 line). 6 vector addresses.
- (7) Timer: 3-channel multiple-functional timer
 - Timer 1: Remote control signal receiver/8-bit interval + tone generator
 - Timer 2: PWM type DA converter(14 bits or 8 bits + 6 bits)/tone generator
 - Time base timer: Clock counter(also used as a watchdog timer)/14-bit event counter
- (8) Serial input/output: 8 bits x 2 channels. One of them can be used as the LSB-first or the MSB-first serial transfer port.
- (9) 4-bit 8-channel AD converter: AD conversion mode/comparator mode
- (10) FLT display controller
 - Segments: 8 to 20. Digits: 8 to 16 \rightarrow Selectable by software.
 - 8-level dimmer function
 - Pull-down resistor option available
 - Static display mode available
- (11) On-chip 9-bit counter for detecting horizontal sync.
- (12) On-chip AC zero cross detector
- (13) On-chip triac driver
- (14) Standby function
 - Count operation continues while the CPU operation stops.
 - All of the operations stop. Oscillation stabilization at the restart is internally supported.
- (15) Oscillation circuits: 2
 - Main clock: 4.19MHz crystal oscillator or 4.0MHz ceramic resonator
 - Sub clock: 32.768kHz crystal oscillator
- (16) Packaging: DIP64S
- (17) Evaluation LSI: LC67999(evaluation chip) + EVA850/800 - TB67216(evaluation chip board), LC67PG216 (piggyback type)

Pin Assignment

Case Outline 3071-D64IC
(unit:mm)

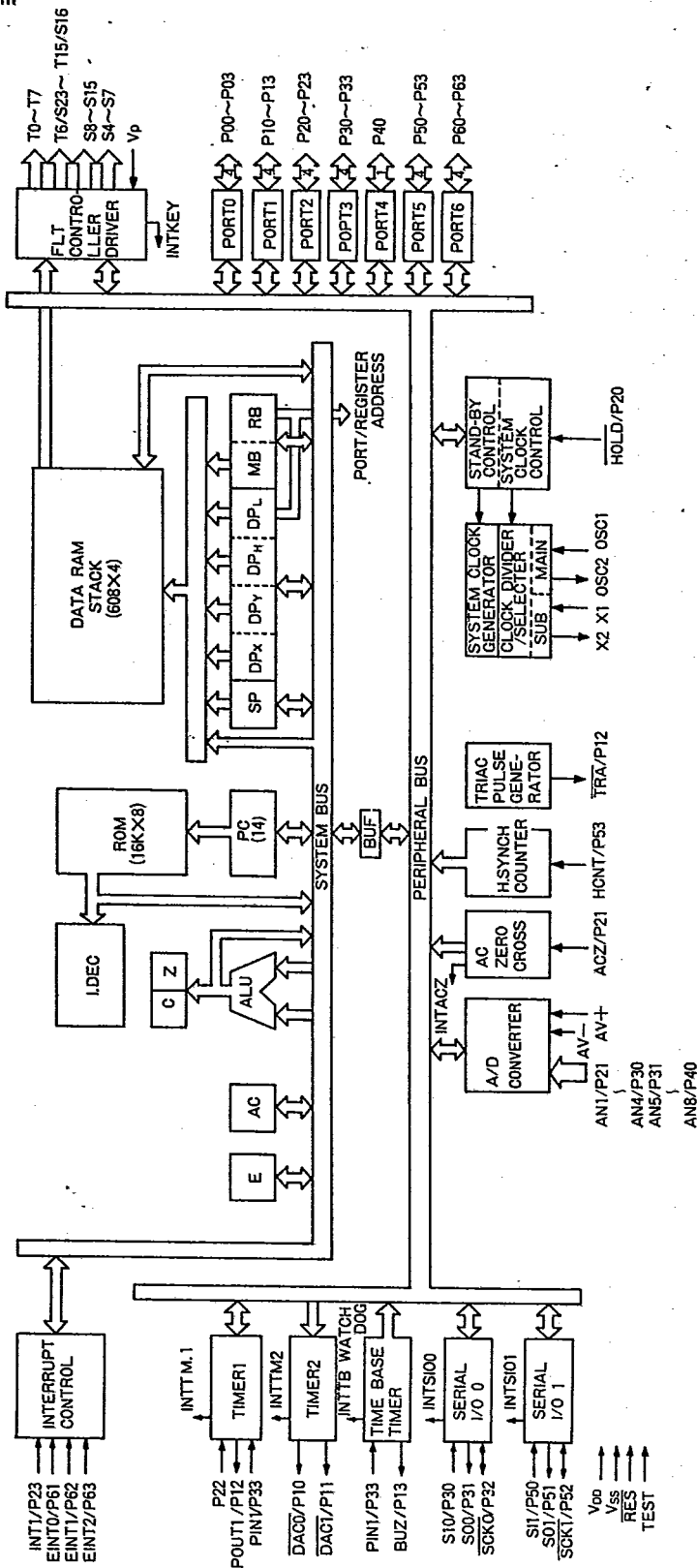


DIP64S		LC67216A	
AV+	1	64	P13/BUZ
AV-	2	63	P12/TRA/P0UT1
P20/HOLD	3	62	P11/DAG1
P21/ACZ/ANI	4	61	P10/DAG0
P22/AN2	5	60	P03/KEY3
P23/INT1/AN3	6	59	P02/KEY2
P30/SIO/AN4	7	58	P01/KEY1
P31/SO0/AN5	8	57	P00/KEY0
P32/SCR0/AN6	9	56	T0
P33/PIN1/AN7	10	55	T1
P40/AN8	11	54	T2
Vss	12	53	T3
OSC1	13	52	T4
OSC2	14	51	T5
Vcc	15	50	T6
RES	16	49	T7
X1	17	48	T8/S23
X2	18	47	T9/S22
TEST	19	46	T10/S21
P50/SI1	20	45	T11/S20
P51/SO1	21	44	T12/S19
P52/SCK1	22	43	T13/S18
P53/HONT	23	42	T14/S17
P60	24	41	T15/S16
P61/EINT0	25	40	VP
P62/EINT1	26	39	S15
P63/EINT2	27	38	S14
S4	28	37	S13
S5	29	36	S12
S6	30	35	S11
S7	31	34	S10
S8	32	33	S9

LC67216A

T-49-19-04

System Block Diagram



LC67216A Block Diagram

Development Support System

The following development support tools are provided to develop application programs for the LC67216A microcomputer.

(1) User's Manual

LC67216A User's Manual

(2) Development Tool Manual

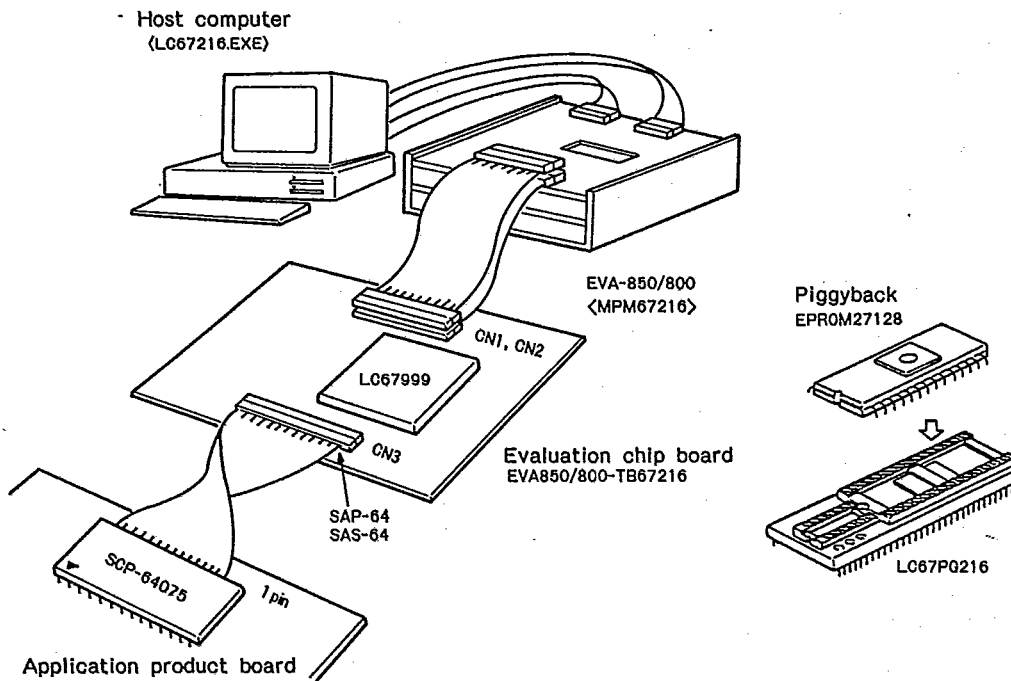
EVA850/800-LC67216 Development Tool Manual

(3) Development Support Tools**1 Tools for developing application programs**

- i. Host computer --- Sanyo MS-DOS machine compatible with IBM PC/XT or IBM PC/AT.
- ii. Cross Assembler ---MS-DOS based cross assembler (LC67216.EXE)

2 Tools for evaluating application programs

- i. Emulator --- EVA-850 main unit or EVA-800 main unit (monitor ROM: MPM67216) and EVA chip board (EVA850/800-TB67216)
- ii. Evaluation chip --- LC67999
- iii. Simulation chip --- LC67PG216

Outline of the development support system

Note 1: IBM PC/XT and IBM PC/AT are products of IBM Corporation. MS-DOS is a registered trademark of Microsoft Corporation.

Note 2: The suffixes of the EVA-850 and EVA-800 change like A to B, B to C, and so on as some improvements are made on them.

Please check the suffix before starting program evaluation.

Pin Description

Pin No	Pin name	I/O	Function(s)	Pin No	Pin name	I/O	Function(s)
1	AV+	-	AD conversion reference voltage input (+)	33	S9	O	Pch high withstand voltage output (for segment)
2	AV-	-	AD conversion reference voltage input (-)	34	S10	O	Same as above.
3	P20/HOLD	I	Input/HOLD control input	35	S11	O	Same as above.
4	P21/ACZ/AN1	I/O	Input/output, also used as AC zero cross input/AD input	36	S12	O	Same as above.
5	P22/AN2	I/O	Input/output, also used as AD input.	37	S13	O	Same as above.
6	P23/INT1/AN3	I/O	Input/output, also used as Interrupt input/AD input	38	S14	O	Same as above.
7	P30/S11/AN4	I/O	Input/output, also used as serial input/AD input.	39	S15	O	Same as above.
8	P31/SO0/AN5	I/O	Input/output, also used as serial output/AD input.	40	Vp	-	Power supply for pull-down resistors
9	P32/SCK0/AN6	I/O	Input/output, also used as serial clock input/output or AD input.	41	T15/S16	O	Pch high withstand voltage output (for digit/segment)
10	P33/PIN1/AN7	I/O	Input/output, also used as remote control signal input/AD input.	42	T14/S17	O	Same as above.
11	P40/AN8	I/O	Input/output, also used as AD input.	43	T13/S18	O	Same as above.
12	Vss	-	Power supply (-)	44	T12/S19	O	Same as above.
13	OSC1	I	Main clock oscillation input	45	T11/S20	O	Same as above.
14	OSC2	O	Main clock oscillation output	46	T10/S21	O	Same as above.
15	Vdd	-	Power supply (+)	47	T9/S22	O	Same as above.
16	RES	I	Reset input	48	T8/S23	O	Same as above.
17	X1	I	Sub clock oscillation input	49	T7	O	Pch high withstand voltage output (for digit)
18	X2	O	Sub clock oscillation output	50	T6	O	Same as above.
19	TEST	I	Test input	51	T5	O	Same as above.
20	P50/S11	I/O	Nch medium withstand voltage input/output, also used as serial input.	52	T4	O	Same as above.
21	P51/SO1	I/O	Nch medium withstand voltage input/output, also used as serial output.	53	T3	O	Same as above.
22	P52/SCK1	I/O	Nch medium withstand voltage input/output, also used as serial clock input/output	54	T2	O	Same as above.
23	P53/HCNT	I/O	Nch medium withstand voltage input/output, also used as H counter input.	55	T1	O	Same as above.
24	P60	I/O	Nch medium withstand voltage input/output	56	T0	O	Same as above.
25	P61/EINT0	I/O	Nch medium withstand voltage input/output, also used as Interrupt input	57	P00/KEY0	I/O	Nch medium withstand voltage input/output, also used as key scan input.
26	P62/EINT1	I/O	Same as above	58	P01/KEY1	I/O	Same as above.
27	P63/EINT2	I/O	Same as above	59	P02/KEY2	I/O	Same as above.
28	S4	O	Pch high withstand voltage output (for segment)	60	P03/KEY3	I/O	Same as above.
29	S5	O	Same as above.	61	P10/DAC0	I/O	Nch medium withstand voltage input/output, also used DA output.
30	S6	O	Same as above.	62	P11/DAC1	I/O	Nch medium withstand voltage input/output, also used DA output.
31	S7	O	Same as above.	63	P12/TRA /POUT1	I/O	Nch medium withstand voltage input/output, also used triac output/pulse output.
32	S8	O	Same as above.	64	P13/BUZ	I/O	Nch medium withstand voltage input/output, also used as buzzer sound output.

Pin Function

Pin name	g	I/O	Option(s)	Functional description	Logic and mode at reset	Unused pin handling
VDD	1	—	—	Power supply	—	—
VSS	1	—	—		—	—
Vp	1	—	—	Power supply for high withstand voltage pin load	—	Connected to VDD.
AV+	1	—	—	AD converter reference voltage input	—	Connected to VSS.
AV-	1	—	—		—	
TEST	1	I	—	LSI test input. Be sure to connect this with VSS.	—	Always connected to VSS.
RES	1	I	—	System reset input. With HOLD = 'H' and RES = 'L', the system will be initialized (initial system reset).	—	—
OSC1	1	I	• CF • X'tal	Main system clock oscillation circuit pin. If external clock input is selected, leave the OSC2 pin open and use the OSC1 input pin.	—	—
OSC2	1	O	• External Input		—	—
X1	1	I	—	Sub clock oscillation circuit pin. If external clock input is selected, leave the X2 pin open and use the X1 input pin. With on-chip feedback resistor and damping resistor.	—	Connect X1 to VDD while leave X2 open.
X2	1	O	—		—	
P00/KEY0 P01/KEY1 P02/KEY2 P03/KEY3	4	I/O	• Pull-up/open drain output (in bit units) • Pull-down resistor (in-bit units)	Input/output in bit units or 4-bit units. Output circuit type can be selected for each pin from open drain (OD) and pull-up MOS output (PU) types. If OD is selected, the withstand voltage level will be +15V. Low threshold level input for key scan input. Automatic key data storage into RAM	'H' in output mode	Connect OD pin to VSS while leave the PU pin open.
P10/DAC0 P11/DAC1 P12/TRA /POUT1 P13/BUZ	4	I/O	• Pull-up/open drain output (in bit units)	Input/output in bit units or 4-bit units. Output circuit type can be selected for each pin from open drain (OD) and pull-up MOS output (PU) types. If OD is selected, the withstand voltage level will be +15V. Alternative pin function(s) DAC0 PWM DAC0 output from timer 2 DAC1 PWM DAC1 output from timer 2, and program pulse output [TRA Triac control pulse output, or program pulse output from timer 1 [/POUT1 BUZ Buzzer output from time base timer	'H' in output mode	Connect OD pin to VSS while leave the PU pin open.
P20/HOLD	4	I	—	Input/output in bit units or 4-bit units. A direction register is provided to set an operation mode (input mode or output mode) for each port bit. The P20/HOLD pin is used only as the input pin. Alternative pin function(s) HOLD HOLD control input and reset inhibit input ACZ AC zero cross detect input INT1 Interrupt input AN1 AD converter channel 1 input AN2 AD converter channel 2 input AN3 AD converter channel 3 input	Input mode	Connected to VDD. The pins already connected to VDD should not be set to the output mode by software.
P21/ACZ/AN1	I/O	—				
P22/AN2	I/O	—				
P23/INT1/AN3	I/O	—				
P30/SI0/AN4 P31/SO0/AN5 P32/SCK0 /AN6 P33/PIN1/AN7	4	I/O	—	Input/output in bit units or 4-bit units. A direction register is provided to set an operation mode (input mode or output mode) for each port bit. Alternative pin function(s) SI0 Serial I/O channel 0 → Serial data input SO0 Serial I/O channel 0 → Serial data output SCK0 Serial I/O channel 0 → Serial clock input/output PIN1 External interrupt source input (timer 1 and time base timer) AN4 AD converter channel 4 input AN5 AD converter channel 5 input AN6 AD converter channel 6 input AN7 AD converter channel 7 input	Input mode	Connected to VDD. Note that the pins already connected to VDD should not be set to the output mode by software.

Continued on next page.

Continued from previous page.

Pin name	I/O	Option(s)	Functional description	Logic and mode at reset	Unused pin handling
P40/AN8	I/O	---	Input/output in bit units. A direction register is provided to set an operation mode (input mode or output mode) for each port bit. Alternative pin function AN8 AD converter channel 8 Input	Input mode	Connected to VDD. Note that the pins already connected to VDD should not be set to the output mode by software.
P50/S11 P51/SO1 P52/SCK1 P53/HCNT	I/O	• Pull-up/open drain output (in bit units)	Input/output in bit units or 4-bit units. Output circuit type can be selected for each pin from open drain (OD) and pull-up MOS output (PU) types. If OD is selected, the withstand voltage level will be +15V. A port control register is provided to set an operation mode (input mode or output mode) for all the four port pins at the same time. Alternative pin function(s) S11 Serial I/O channel 1 → Serial data Input SO1 Serial I/O channel 1 → Serial data output SCK1 Serial I/O channel 1 → Serial clock Input/output HCNT H counter count Input	Input mode	Connect the OD pin to VSS while leave the PU pin open.
P60 P61/EINT0 P62/EINT1 P63/EINT2	I/O	• Pull-up/open drain output (in bit units)	Input/output in bit units or 4-bit units. Output circuit type can be selected for each pin from open drain (OD) and pull-up MOS output (PU) types. If OD is selected, the withstand voltage level will be +15V. Alternative pin function(s) EINT0 Extended interrupt input EINT0 EINT1 Extended interrupt input EINT1 EINT2 Extended interrupt input EINT2	H' in output mode	Same as above.
S4~S7	O	Pull-down resistor (in bit units)	Segment outputs from an FLT controller (S4 to S7). If static display mode is selected, these output pins are used to output data to an external circuit from a fixed RAM address (general discrete output).	L' in output mode	Leave the pull-down type pins open while connect the OD type pins to VDD.
S8~S15	O	Pull-down resistor (in bit units)	Segment outputs from an FLT controller (S8 to S15). If static display mode is selected, these output pins are used to output data to an external circuit from fixed RAM addresses (general discrete output).	L' in output mode	Same as above.
T0~T7	O	Pull-down resistor (in bit units)	Timing signal outputs from an FLT controller (T0 to T7). If static display mode is selected, these output pins are used to output data to an external circuit from fixed RAM addresses (general discrete output).	L' in output mode	Same as above.
T8/S23~ T15/S16	O	Pull-down resistor (in bit units)	Timing signal/segment outputs from an FLT controller (alternate output pins). If static display mode is selected, these output pins are used to output data to an external circuit from fixed RAM addresses (general discrete output). In addition, unused pins are used for the same purpose.	L' in output mode	Same as above.

LC67216A

T-49-19-04

User Options

① Options for main clock oscillation circuits

Option name	Related pins	Oscillation circuit type	Circuit conditions
External clock option	OSC1, OSC2		<ul style="list-style-type: none"> - Internal clock input with Schmitt specification - Leave the OSC2 pin open.
Ceramic (CF) resonator oscillation option			<ul style="list-style-type: none"> - Rf is a feedback resistor. - Internal clock input with Schmitt specification
Crystal (X'tal) oscillation option			

② Options for sub clock oscillation circuits

Option name	Related pins	Oscillation circuit type	Circuit conditions
Crystal (X'tal) oscillation option	X1, X2		<ul style="list-style-type: none"> - Rf is a feedback resistor. - Rd is a damping resistor.
External clock option			<ul style="list-style-type: none"> - Leave the X2 pin open.
No sub clock oscillation circuit			<ul style="list-style-type: none"> - Connect the X1 pin to VDD. - Leave the X2 pin open.

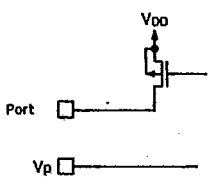
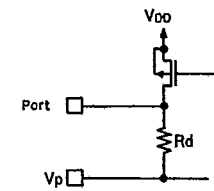
③ Options for port 0 input pull-down resistor (in 4-bit units)

Option name	Related pins	Oscillation circuit type	Circuit conditions
No pull-down resistor selected	P00~P03		
Pull-down resistor selected			- The pull-down resistor has been selected. Note that the pull-down resistor option can be used independently of the pull-up (PU) transistor output option.

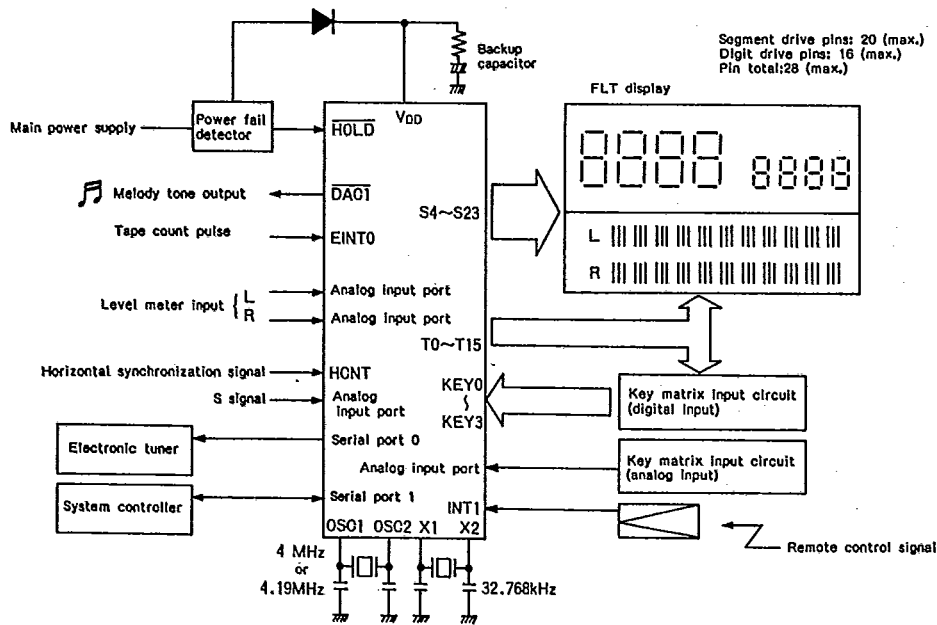
④ Options for output circuit types of medium withstand voltage ports (in bit units)

Option name	Related pins	Oscillation circuit type	Circuit conditions
Nch open drain output (OD)	P00~P03 P10~P13 P50~P53 P60~P63		Input/output withstand voltage level = +15V
Pull-up transistor output (PU)			Input/output withstand voltage level = $V_{DD} + 0.3V$. The output types can be divided into two according to Pch transistor driving capability: CMOS output (P1 and P5) and PU MOS output (P0 and P6).

⑤ Options for the output types of high withstand voltage ports (in bit units)

Option name	Related pins	Oscillation circuit type	Circuit conditions
Pch open drain output (OD)	T0~T7 T8/S23~T15/S16 S4~S15		
Output with a pull-down resistor (PD)			

Example application



Example application: VCR channel select timer, level meter, tape counter, and remote control signal receiver

LC67216A

T-49-19-04

Main Specifications for the LC67216A

1. Absolute Maximum Ratings/Ta = 25°C, VSS = 0V

Parameter	Symbol	Related Pins	Conditions		Limits	Units
Power supply voltage	VDD max	VDD			-0.3~+7.0	V
	Vp max	Vp			VDD-45~VDD+0.3	
	AV+max	AV+			-0.3~VDD+0.3	
	AV-max	AV-			-0.3~VDD+0.3	
Input voltage	Vi(1)	OSC1, X1	Self oscillation		Up to produced voltage.	V
	Vi(2)	TEST, RES, OSC1, P20/HOLD	OSC1: External clock input		-0.3~VDD+0.3	
	Vi(3)	P00~P03	Input pull-down resistor selected, Nch output transistor OFF.		-0.3~VDD+0.3	
Output voltage	Vo(1)	OSC2, X2	Self oscillation		Up to produced voltage.	V
	Vo(2)	S4~S15, T0~T7, T8/S23~T15/S16			VDD-45~VDD+0.3	
Input/output voltage	Vio(1)	P21~P23, P30~P33, P40			-0.3~VDD+0.3	V
		P00~P03, P10~P13, P50~P53, P60~P63	Pull-up option selected.			
	Vio(2)	P00~P03, P10~P13, P50~P53, P60~P63	Open drain option selected, P00-P03; Without input pull-down resistor		-0.3~+15	V
Output current	Iop(1)	P00~P03, P60~P63	Pull-up option selected	Per pin	-2~0	mA
		P21~P23	Output enable mode			
	Iop(2)	P10~P13, P50~P53	Pull-up option selected	Per pin	-4~0	mA
		P30~P33, P40	Output enable mode			
	Iop(3)	S4~S15	Per pin		-15~0	mA
	Iop(4)	T0~T7, T8/S23~T15/S16	Per pin		-30~0	
	ION(1)	P00~P03, P21~P23, P40, P60~P63	Per pin		0~15	mA
			ION(2)	P30~P33, P50~P53	0~20	
					ION(3)	
	ΣIop(1)	P00~P03, P10~P13, P21~P23, P30~P33, P40	Pull-up option selected	Pin total	-15~0	mA
Output enable mode						
ΣIop(2)	P50~P53, P60~P63, S4~S15, T0~T7, T8/S23~T15/S16	Pull-up option selected	Pin total	-120~0	mA	

Continued on next page.

Continued from previous page.

Parameter	Symbol	Related Pins	Conditions		Limits	Units
Output current	$\Sigma I_{ON}(1)$	P00~P03 P10~P13 P21~P23 P30~P33 P40	Pin total	Average value for 100 msec	0~55	mA
	$\Sigma I_{ON}(2)$	P50~P53 P60~P63	Pin total	Average value for 100 msec	0~30	mA
Allowable power dissipation	$P_d \max$	DIP-64S	$T_a = -30 \sim +70^\circ\text{C}$		600	mW
Operating temperature range	T_{opg}				-30~+70	°C
Storage temperature range	T_{stg}				-55~+125	°C

2. Recommended Operating Conditions / $T_a = -30$ to $+70^\circ\text{C}$, $V_{SS} = 0\text{V}$

Parameter	Symbol	Related Pins	Conditions	Limits			Units		
				$V_{DD}(V)$	min	typ		max	
Operating power supply	$V_{DD}(1)$	VDD	Main clock operation mode $0.92\mu\text{s} \leq T_{cyc} \leq 67\mu\text{s}$		4.5		6.0	V	
	$V_{DD}(2)$				3.0		6.0		
	$V_{DD}(3)$				3.0		6.0		
	V_p	V_p	Sub clock operation mode $40\mu\text{s} \leq T_{cyc} \leq 67\mu\text{s}$		-35		V_{DD}	V	
	AV+	AV+			AV-		V_{DD}		
	AV-	AV-			VSS		AV+		
Power supply for RAM backed-up mode	VST	VDD	HOLD mode		1.8		6.0	V	
Input High voltage	$V_{IH}(1)$ (Schmitt)	RES		4.5~6.0	0.75 V_{DD}		V_{DD}	V	
				3.0~4.5	0.8 V_{DD}		V_{DD}		
				1.8~3.0	0.85 V_{DD}		V_{DD}		
	$V_{IH}(2)$ (Schmitt)	P20/HOLD		4.5~6.0	0.75 V_{DD}		V_{DD}		
				3.0~4.5	0.8 V_{DD}		V_{DD}		
	$V_{IH}(3)$ (Schmitt)	P22, P23 P30~P33 OSC1 and X1: External clock input		P22, P23, P30 to P33: Output disabled	4.5~6.0	0.75 V_{DD}			V_{DD}
					3.0~4.5	0.8 V_{DD}			V_{DD}
	$V_{IH}(4)$ (Schmitt)	Output option: OD P50~P53 P61~P63		Nch output transistor OFF	4.5~6.0	0.75 V_{DD}			+13.5
					3.0~4.5	0.8 V_{DD}			+13.5
$V_{IH}(5)$ (Schmitt)	Output option: PU P50~P53 P61~P63	Nch output transistor OFF	4.5~6.0	0.75 V_{DD}		V_{DD}			
			3.0~4.5	0.8 V_{DD}		V_{DD}			
$V_{IH}(6)$ (Low threshold input voltage)	Output option: OD P00~P03	Nch output transistor OFF	3.0~6.0	1.9		+13.5			
$V_{IH}(7)$ (Low threshold input voltage)	Output option: PU P00~P03	Nch output transistor OFF	3.0~6.0	1.9		V_{DD}			
$V_{IH}(8)$	P21, P40 P60 with PU output specification	P21 and P40: Output disabled. P60: Nch output transistor OFF	4.5~6.0	0.7 V_{DD}		V_{DD}			
			3.0~4.5	0.75 V_{DD}		V_{DD}			
$V_{IH}(9)$	P10 to P13 and P60 with OD output specification	Nch output transistor OFF	4.5~6.0	0.7 V_{DD}		+13.5			
			3.0~4.5	0.75 V_{DD}		+13.5			

Continued on next page.

Continued from previous page.

Parameter	Symbol	Related Pins	Conditions	Limits (Ta=-30to+70°C)			Units		
				VDD(V)	min	typ		max	
Input Low voltage	VIL(1) (Schmitt)	RES P20/HOLD		4.5~6.0	Vss		0.25VDD	V	
				3.0~4.5	Vss		0.2VDD		
				1.8~3.0	Vss		0.15VDD		
	VIL(2) (Schmitt)	P22, P23 P30~P33 P61~P63 P50 to P53: Output with OD specification. OSC1: External clock input	P22, P23, P30 to P33: Output disabled P50 to P53, P61 to P63: Nch output transistor OFF	4.5~6.0	Vss		0.25VDD	V	
				3.0~4.5	Vss		0.2VDD		
	VIL(3) (Low threshold input voltage)	P00~P03	Nch output transistor OFF	4.5~6.0	Vss		0.5	V	
				3.0~4.5	Vss		0.35		
	VIL(4)	P10 to P13, P40, P60, and P21: output with OD specification. TEST X1: External clock input	P10 to P13, P60: Nch output transistor OFF P21 and P40: Output disabled	4.5~6.0	Vss		0.3VDD	V	
3.0~4.5				Vss		0.25VDD			
Instruction cycle time	Tcyc		The instruction cycle times vary depending on the operating power supply range. References to VDD(1) to VDD (3) are also required.		0.92	67	μSEC		
External main clock input mode	Frequency	fmosc(1)	OSC1	See Figure 1.	3.0~6.0	2.0	4.33	MHz	
	Pulse width	fmexth fmextL		Same as above.	4.5~6.0	70		nsec	
					3.0~6.0	140			
	Rise time and fall time	tmextr tmextF		Same as above.	4.5~6.0		30	nsec	
3.0~6.0						60			
External sub clock input mode	Frequency	tsosc	X1	See Figure 1.	3.0~6.0	30	50	kHz	
	Pulse width	tsexth tsextL		Same as above.	3.0~6.0	6	34	μSEC	
					3.0~6.0		0.2	μsec	
	Rise time and fall time	tsextr tsextF		Same as above.	3.0~6.0				
Self main clock oscillation	Ceramic resonator oscillation	Oscillation frequency	fmxtal	OSC1, OSC2	See Figure 2.	4.19MHz	3.0~6.0	4.194304	MHz
		Oscillation stable period	tmsxtat				See Figure 5.		20
	Ceramic resonator oscillation	Oscillation frequency	fmcf	See Figure 3.	4 MHz	3.0~6.0		4.0	MHz
		Oscillation stable period	tmscf	See Figure 5.	4 MHz	3.0~6.0		20	msec
Self sub clock oscillation	Crystal oscillation	Oscillation frequency	fsxtal	X1, X2	See Figure 4.	32kHz	3.0~6.0	32.768	kHz
		Oscillation stable period	fssxtal				See Figure 5.		10

LC67216A

T-49-19-04

3. Electrical Characteristics
3-1. DC Characteristics/Ta=-30 to +70°C, Vss=0 V

Parameter	Symbol	Related Pins	Conditions		Limits			Units	
					VDD(V)	min	typ		max
Input High current	I _{IH} (1)	Output option: OD specification P00~P03 P10~P13 P50~P53 P60~P63	V _{IN} = +13.5V	Nch output transistor OFF (Including output-OFF leakage current). P00 to P03: Without input pull-down resistor.	3.0~6.0			+5.0	μA
	I _{IH} (2)	RES, P20/HOLD OSC1: External clock Input	V _{IN} =VDD		3.0~6.0			+1.0	μA
	I _{IH} (3)	P21~P23 P30~P33 P40	V _{IN} =VDD	Output disabled (Including output-OFF leakage current). P21 or ACZ: Self bias OFF.	3.0~6.0			+1.0	μA
	I _{IH} (4)	P00 to P03: PD output specification	V _{IN} =VDD	Nch output transistor OFF	3.0~6.0	+2.5		+200	μA
				4.5~6.0	+13		+200		
Input Low current	I _{IL} (1)	Output option: OD specification P00~P03 P10~P13 P50~P53 P60~P63 P20 / HOLD, RES OSC1: External clock input	V _{IN} =VSS	Nch output transistor OFF (including output-OFF leakage current)	3.0~6.0	-1.0			μA
	I _{IL} (2)	P21~P23 P30~P33 P40	V _{IN} =VSS	Output disabled (including output-OFF leakage current). P21 or ACZ: Self bias OFF.	3.0~6.0	-1.0			μA
	I _{IL} (3) (Pull-up MOS output current)	P00~P03 P21~P23 P60~P63	V _{IN} =VSS	H output. Output enabled (including output-OFF leakage current). P22 or ACZ: Self bias OFF.	6.0	-1.6			mA
Output High voltage	V _{OH} (1) (Pull-up MOS output voltage)	P21~P23 Output option: PU specification P00~P03 P60~P63	I _{OH} = -200μA	P21 to P23: Output disabled. P22 or ACZ: Self bias OFF.	4.5	2.4			V
			I _{OH} = -10μA		4.5	4.0			
	V _{OH} (2) (CMOS output voltage)	P30~P33 P40 Output option: PU specification P10~P13 P50~P53	I _{OH} = -1 mA	P30 to P33 and P40: Output disabled. The other ports mean the ports to which V _{OH} (1) and V _{OH} (2) apply. However, the I _{OH} total should not exceed the absolute maximum rating.	4.5~6.0	VDD	-1.0		V
	I _{OH} = -0.1mA (I _{OH} of each pin of other ports must be less than -1mA.)	3.0~6.0	VDD		-0.5				

Continued on next page.

LC67216A

T-49-19-04

Continued from previous page.

Parameter	Symbol	Related Pins	Conditions	Limits			Units		
				V _{DD} (V)	min	typ		max	
Output High voltage	VOH(3)	S4~S15	I _{OH} = -5 mA	The other ports mean the ports to which VOH(3) and VOH(4) apply. However, the I _{OH} total should not exceed the absolute maximum rating.	4.5~6.0	V _{DD} -1.8		V	
			I _{OH} = -1 mA (I _{OH} of each pin of other ports must be less than -1mA.)		3.0~6.0	V _{DD} -1.0			
	VOH(4)	T0~T7 T8/S23~T15/S16	I _{OH} = -20mA	The other ports mean the ports to which VOH(3) and VOH(4) apply. However, the I _{OH} total should not exceed the absolute maximum rating.	4.5~6.0	V _{DD} -2.1			V
			I _{OH} = -1 mA (I _{OH} of each pin of other ports must be less than -1mA.)		3.0~6.0	V _{DD} -1.0			
Output Low voltage	VOL(1)	P00~P03 P21~P23 P40 P60~P63	I _{OL} =10mA	P21/ACZ: Self bias OFF, P21 to P23, and P40; Output enable mode	4.5~6.0		2.0	V	
			I _{OL} =5 mA		3.0~6.0		2.0		
	VOL(2)	P30~P33 P50~P53	I _{OL} =15mA	Output enable mode. The other ports mean the ports to which VOH(1), VOH(2), VOH(3) and VOH(4) apply. However, the I _{OL} total should not exceed the absolute maximum rating.	4.5~6.0		2.0	V	
			I _{OL} =1.6mA		4.5~6.0		0.4		
			I _{OL} =0.5mA (I _{OL} of each pin of other ports must be less than 1mA.)		3.0~6.0		0.5		
	VOL(3)	P10~P13	I _{OL} =30mA	The other ports mean the ports to which VOH(1), VOH(2), VOH(3) and VOH(4) apply. However, the I _{OL} total should not exceed the absolute maximum rating.	4.5~6.0		2.0	V	
			I _{OL} =2 mA (I _{OL} of each pin of other ports must be less than 1mA.)		3.0~6.0		1.0		
	VOL(4)	Output option: PD specification S4~S15 T0~T7 T8/S23~T15/S16	V _p =-35V See Figure 9.	Pch output transistor OFF.	4.5~6.0		-33	V	
Output-OFF leakage current	I _{OFF} (1)	Output option: OD specification. S4~S15 T0~T7 T8/S23~T15/S16	V _{OUT} =V _{DD}	Pch output transistor OFF	3.0~6.0		+30	μA	
			V _{OUT} = V _{DD} -40V		3.0~6.0	-30			
Output Low current (current which flows into a pull-down resistor)	I _{OL} (1)	Output option: PD specification S4~S15 T0~T17 T8/S23~T15/S16	V _{OUT} = +3.0V V _p =-35V	Pch output transistor OFF	5.0	190	362	830	μA

Continued on next page.

Continued from previous page.

Parameter	Symbol	Related Pins	Conditions		Limits			Units	
					VDD(V)	min	typ		max
Hysteresis voltage	VHYS(1)	P20/HOLD, P22, P23 P30~P33 P50 to P53 and P61 to P63; OD output specification. OSC1: External clock input RES.	P20, P22 and P23, and P30 to P33: Output disabled, P50 to P53, and P60 to P63: Nch output transistor OFF		3.0~6.0		0.1VDD		V
Operating current dissipation	IDDOP(1)	VDD	Main crystal oscillation fosc = 4.19MHz. Sub crystal oscillation fosc = 32kHz. Tcyc = 0.95 μsec. Internal operation at a maximum mode.	Not including the amount of current dissipated by output drivers and pull-down resistors.	4.5~6.0		4	12	mA
					3.0		0.35	1	
	IDDOP(2)				6.0		1.4	3.6	mA
					3.0		0.04	0.15	
	IDDOP(3)				6.0		0.25	0.8	mA
Current dissipation at HALT mode	IDDHALT (1)	VDD	Internal operation at a maximum mode. Main crystal oscillation fosc = 4.19MHz. Sub crystal oscillation fosc = 32kHz. HALT mode.	Not including the amount of current dissipated by output drivers and pull-down resistors.	4.5~6.0		1.5	4	mA
					3.0		15	50	
	IDDHALT (2)				6.0		150	500	μA
Current dissipation at HOLD mode	IDDHOLD	VDD	HOLD mode	Not including the amount of current dissipated by output drivers and pull-down resistors. In addition, the input current to each pin and output-OFF leakage current are not included.	6.0		0.05	10	μA
					1.8		0.02	2	

3-2. AC Characteristics/Ta=-30to+70°C, Vss=0V

Parameter	Symbol	Related Pins	Conditions	Limits			Units
				V _{DD} (V)	min	typ	
Serial clock	Cycle time	tCKCY	SCK0, SCK1 See Figure 6. OD output specification requires a 1kΩ of pull-up resistance to be externally added.	4.5~6.0	0.8		μSEC
				3.0~6.0	3.2		
	3.0~6.0	2Tcyc					
	Low level pulse width, High level pulse width.	tCKL tCKH	Same as above.	4.5~6.0	0.3		μSEC
3.0~6.0				1.2			
Serial input	Data setup time	tICK	SI0, SI1 Same as above.	4.5~6.0	0.15		μSEC
	Data hold time	tCKI		3.0~6.0	0.6		
Serial output	Output delay time	tCKO	SO0, SO1 Same as above.	4.5~6.0		0.25	μSEC
				3.0~6.0		1.0	
Pulse input conditions	High level/ Low level pulse width	tPIH(1) tPIL(1)	INT1 EINT0 EINT1 EINT2 HCNT RES PIN1 INT1 EINT1 EINT2 HCNT RES PIN1 • Conditions required by each interrupt source. • See Figure 7. • H counter operational conditions required by clock detect mode. • Reset conditions required by a reset operation.	3.0~6.0	2Tcyc		μSEC
		tPIH(2) tPIL(2)	PIN1 See Figure 7. Timer 1 pulse counter operational conditions required by a remote control signal receive mode.	3.0~6.0	61		μSEC
		tPIH(3) tPIL(3)	PIN1 HCNT • Time base timer pulse count conditions required by an external clock input mode. • H counter pulse count conditions required by an immediate input mode. See Figure 7.	3.0~6.0	0.5		μSEC

Continued on next page.

Continued from previous page.

Parameter	Symbol	Related Pins	Conditions	VDD(V)	Limits			Units	
					min	typ	max		
AC zero cross detect input characteristics	Input frequency	fZIN	ACZ/P21	4.5~6.0	40		1000	Hz	
	Input voltage	VZIN	Coupling capacitor C=1 μF		1.0		2.4	Vp-p	
	Detection error	VZA	60Hz Sine wave input				±100	mV	
	Input current	IiHZ			VIN=VDD		+20	+60	μA
		IiLZ			VIN=VSS	-60	-20		
	H level input threshold voltage	Vt*ACH					Vt*ACM +0.2		V
	M level input threshold voltage	Vt*ACM				0.3VDD		0.7VDD	
L level input threshold voltage	Vt*ACL				Vt*ACM -0.2				

3-3, A/D conversion characteristics /Ta=-30to+70°C, VSS=0V (A/D conversion is used in A/D mode.)

Parameter	Symbol	Related Pins	Conditions	VDD(V)	Limits			Units
					min	typ	max	
Resolution				5.0~6.0		8		Bit
Absolute accuracy			AV+=VDD AV-=VSS AN1: ACZ self bias OFF				±16	LSB
Conversion time	TCAD		AD conversion time: 51 Tcyc period		47 (Tcyc=0.92μs)		204 (Tcyc=4μs)	μsec
Reference input voltage	AV+	AV+			AV-		VDD	V
	AV-	AV-			VSS		AV+	
Reference input current	I _{AV} I _{REF}	AV+ AV-	AV+=VDD AV-=VSS		75	150	300	μA
Analog input voltage	VAIN	AN1~AN8	• AN1/ACZ: Self bias OFF		AV-		AV±	V
Analog port input current	I _{AIN}	AN1~AN8	VAIN=AV+	AN1: Self bias OFF, Including output-OFF leakage current.			1	μA
			VAIN=AV-		-1			
			AV+=VDD AV-=VSS					

3-4 Comparator characteristics /Ta=-30to+70°C, VSS=0V (A/D conversion is used in comparator mode.)

Parameter	Symbol	Related Pins	Conditions	Limits			Units	
				VDD(V)	min	typ		max
Comparison accuracy	VCECON	AN1~AN8	AV+=VDD P21/ACZ: Self bias OFF. AV-=VSS AN1: ACZ self bias OFF	5.0~6.0			±16	LSB
Threshold voltage	VTHCON	AN1~AN8			AV-		AV+	V
Input voltage	VINCON				AV-		AV+	V
Reference input voltage	AV+	AV+					VDD	V
	AV-	AV-					VSS	
Conversion time	TCC		Comparator conversion time: 23 Tcyc period		21 (Tcyc= 0.92μs)		92 (Tcyc= 4μs)	μs

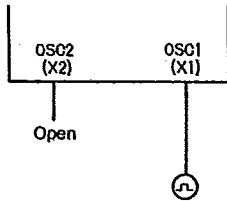
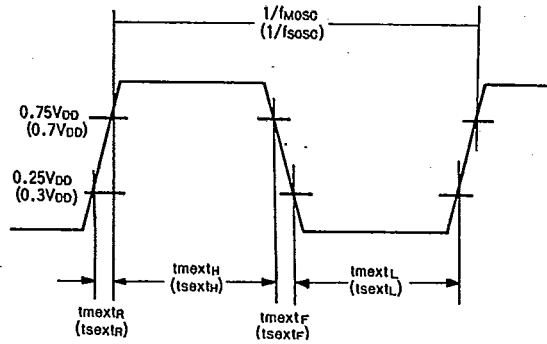
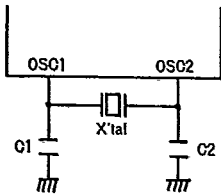


Figure 1 External clock input conditions



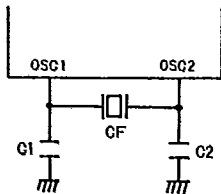
The values in parentheses are the parameters for sub clock oscillation mode.



Frequency	Maker name	X'tal oscillation	C 1	C 2
4.194304kHz	Tokyo Denpa	HC-49/U CL=18pF	22pF	22pF
	Kinseki	HC-49/U CL=16pF	15pF	15pF

C1 and C2 error: Less than 10% (including wire capacitance).
CL = Load capacitance

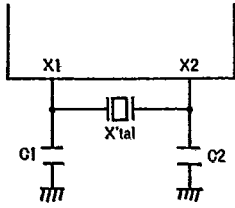
Figure 2 Main clock X'tal oscillation conditions



Frequency	Maker name	Ceramic resonator	C 1	C 2
4 MHz	Murata	CSA4.00MG	33pF	33pF
		CST4.00MGW *1	Not required	Not required
	Kyocera	KBR4.0MS	33pF	33pF
		KBR4.0MES *1	Not required	Not required

C1 and C2 error: Less than 10% (including wire capacitance).
*1: 3-terminal ceramic resonator (with internal C)

Figure 3 Main clock ceramic resonator (CF) oscillation conditions



Frequency	Maker name	X'tal oscillation	C 1	C 2
32.768kHz	Kyocera	KF-38G-13200 C _L =13pF	22pF	22pF
	Daiwa Shinku	DT-38 C _L =12.5pF	15pF	15pF

C1 and C2 error: Less than 10% (including wire capacitance).
C_L = Load capacitance.

Figure 4 Sub clock crystal oscillation conditions

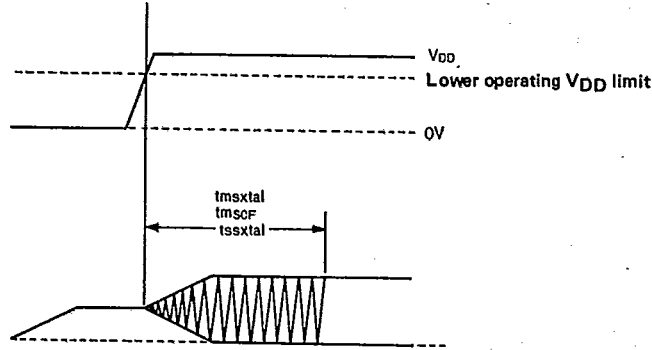


Figure 5 Oscillation stabilization time

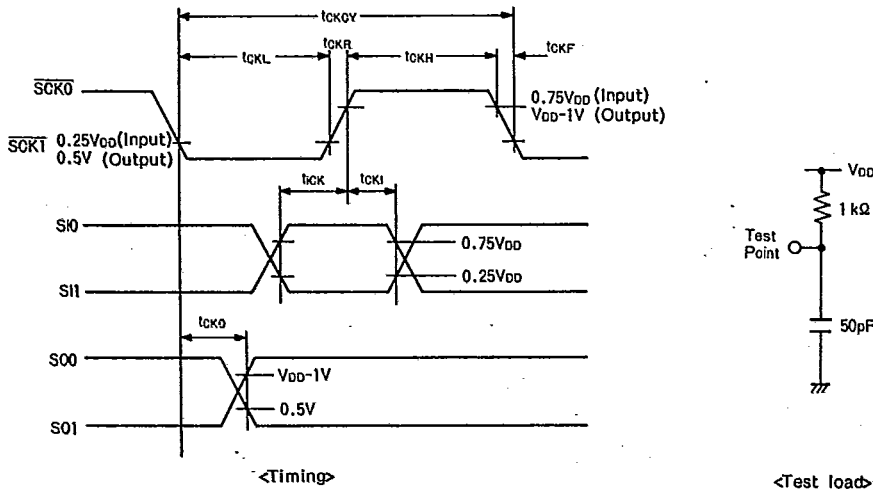


Figure 6 Serial input/output test conditions

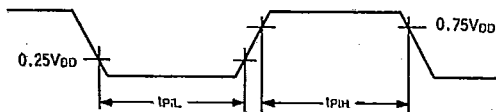


Figure 7 Pulse input timing conditions

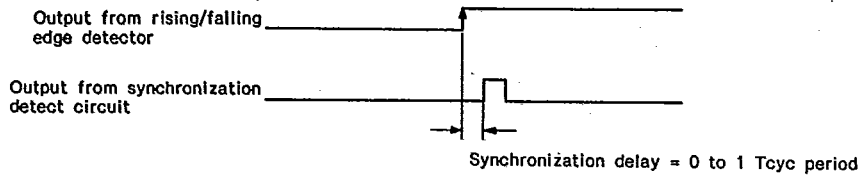
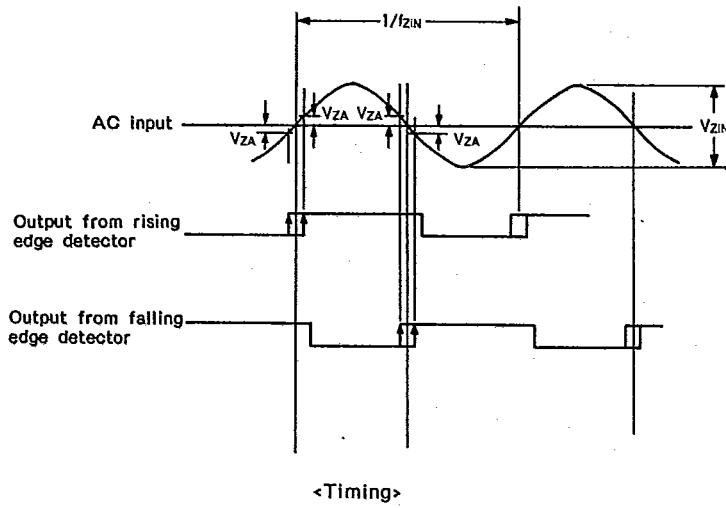
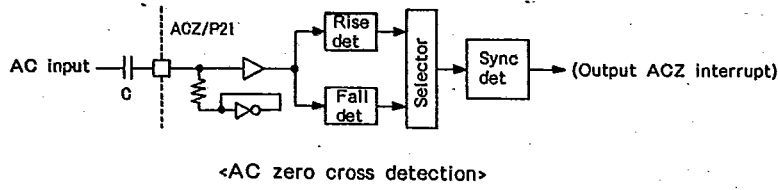


Figure 8 AC zero cross detection

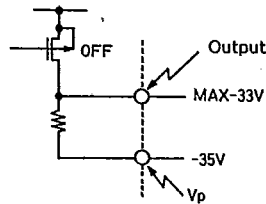


Figure 9 Leakage current at high withstand voltage output

Instruction Set

Instruction group	Mnemonic		Op code		Bytes	Cycles	Operations	Operations description	Affected flag(s)	Remarks
			D ₇ D ₆ D ₅ D ₄	D ₃ D ₂ D ₁ D ₀						
Accumulator Manipulation Instructions	CLA	Clear AC	1 0 0 0	0 0 0 0	1	1	AC ← 0 (same as LAI 0)	Clear the AC.	ZF	Note 1
	DAA	Decimal adjust AC in addition	1 1 0 0 0 0 1 0	1 1 1 1 0 1 1 0	2	2	AC ← (AC) + 6 (same as ADI 6)	Add 6 to the AC.	ZF	
	DAS	Decimal adjust AC in subtraction	1 1 0 0 0 0 1 0	1 1 1 1 1 0 1 0	2	2	AC ← (AC) + 10 (same as ADI 0AH)	Add 10 to the AC.	ZF	
	CLC	Clear CF	0 0 0 1	1 1 1 0	1	1	CF ← 0	Clear the CF (Carry Flag).	CF	
	STC	Set CF	0 0 0 1	1 1 1 1	1	1	CF ← 1	Set the CF.	CF	
	CMA	Complement AC	0 0 0 1	1 0 0 0	1	1	AC ← (AC)	Complement the AC.	ZF	
	IA	Increment AC	0 0 0 1	0 1 0 0	1	1	AC ← (AC) + 1	Increment the AC by 1.	ZF, CF	
	DA	Decrement AC	0 0 1 0	0 1 0 0	1	1	AC ← (AC) - 1	Decrement the AC by 1.	ZF, CF	
	RAR	Rotate AC right through CF	0 0 0 1	0 0 0 0	1	1	AC _n ← (CF), AC _{n-1} ← (AC _n), CF ← (AC ₀)	Rotate the AC right through the CF.	CF	
	RAL	Rotate AC left through CF	0 0 0 0	0 0 0 1	1	1	AC ₀ ← (CF), AC _{n-1} ← (AC _n), CF ← (AC ₀)	Rotate the AC left through the CF.	CF, ZF	
	TAE	Transfer AC to E	0 1 0 0	0 1 0 1	1	1	E ← (AC)	Transfer the AC content to the E register.		
	TEA	Transfer E to AC	0 1 0 0	0 1 1 0	1	1	AC ← (E)	Transfer the E register content to the AC.	ZF	
XAE	Exchange AC with E	0 1 0 0	0 1 0 0	1	1	(AC) ↔ (E)	Exchange the AC content with the E register content.			
Memory Manipulation Instructions	IM	Increment M	0 0 0 1	0 0 1 0	1	1	M(MBR, HL) ← (M(MBR, HL)) + 1	Increment the content of M(MBR, HL) by 1.	ZF, CF	
	DM	Decrement M	0 0 1 0	0 0 1 0	1	1	M(MBR, HL) ← (M(MBR, HL)) - 1	Decrement the content of M(MBR, HL) by 1.	ZF, CF	
	IMDR i8	Increment M direct	1 1 0 0 i ₇ i ₆ i ₅ i ₄	0 1 1 1 i ₃ i ₂ i ₁ i ₀	2	2	M(MBR, i8) ← (M(MBR, i8)) + 1	Increment the content of M(MBR, i8) by 1. i8 is 8-bit immediate data.	ZF, CF	
	DMDR i8	Decrement M direct	1 1 0 0 i ₇ i ₆ i ₅ i ₄	0 0 1 1 i ₃ i ₂ i ₁ i ₀	2	2	M(MBR, i8) ← (M(MBR, i8)) - 1	Decrement the content of M(MBR, i8) by 1. i8 is 8-bit immediate data.	ZF, CF	
	SMB i2	Set M data bit	0 0 0 0	1 1 i ₁ i ₀	1	1	(M(MBR, HL), i2) ← 1	Set a specified bit of the content of M(MBR, HL). Note that the two LSBs are used to specify the bit.		
	RMB i2	Reset M data bit	0 0 1 0	1 1 i ₁ i ₀	1	1	(M(MBR, HL), i2) ← 0	Reset a specified bit of the content of M(MBR, HL). Note that the two LSBs are used to specify the bit.	ZF	
Operations and Comparison Instructions	AD	Add M to AC	0 0 0 0	0 1 1 0	1	1	AC ← (AC) + (M(MBR, HL))	Add the AC content and that of the M(MBR, HL) together in binary and then store the resulted sum into the AC.	ZF, CF	
	ADDR i8	Add M direct to AC	1 1 0 0 i ₇ i ₆ i ₅ i ₄	1 0 0 1 i ₃ i ₂ i ₁ i ₀	2	2	AC ← (AC) + (M(MBR, i8))	Add the AC content and that of the M(MBR, i8) together in binary and then store the resulted sum into the AC. i8 is 8-bit immediate data.	ZF, CF	
	ADC	Add M to AC with CF	0 0 0 0	0 0 1 0	1	1	AC ← (AC) + (M(MBR, HL)) + (CF)	Add the AC content and those of the M(MBR, HL) and the carry flag (CF) together in binary and then store the resulted sum into the AC.	ZF, CF	
	ADI i4	Add immediate data to AC	1 1 0 0 0 0 1 0	1 1 1 1 i ₃ i ₂ i ₁ i ₀	2	2	AC ← (AC) + i ₃ i ₂ i ₁ i ₀	Add the AC content and immediate data in binary and then store the resulted sum into the AC.	ZF	
	SUBC	Subtract AC from M with CF	0 0 0 1	0 1 1 1	1	1	AC ← (M(MBR, HL)) - (AC) - (CF)	Subtract the AC content plus the inverted CF content from the M(MBR, HL) content in binary and then store resulted difference into the AC.	ZF, CF	If there has been a borrow, the carry flag (CF) is set to '0'. Otherwise, the flag is set to '1'.
	ANDA	And M with AC then store AC	0 0 0 0	0 1 1 1	1	1	AC ← (AC) ∧ (M(MBR, HL))	Logically AND the M(MBR, HL) content with the AC content and then store the resulted logical product into the AC.	ZF	
	ORA	Or M with AC then store AC	0 0 0 0	0 1 0 1	1	1	AC ← (AC) ∨ (M(MBR, HL))	Logically OR the M(MBR, HL) content with the AC content and then store the resulted logical sum into the AC.	ZF	
	EXL	Exclusive or M with AC then store AC	0 0 0 1	0 1 0 1	1	1	AC ← (AC) ⊕ (M(MBR, HL))	Logically X-AND the M(MBR, HL) content with the AC content and then store the resulted logical product into the AC.	ZF	
ANDM	And M with AC then store M	0 0 0 0	0 0 1 1	1	1	M(MBR, HL) ← (AC) ∧ (M(MBR, HL))	Logically AND the M(MBR, HL) content with the AC content and then store the resulted logical product into the M(MBR, HL).	ZF		
ORM	Or M with AC then store M	0 0 0 0	0 1 0 0	1	1	M(MBR, HL) ← (AC) ∨ (M(MBR, HL))	Logically OR the M(MBR, HL) content with the AC content and then store the resulted logical sum into the M(MBR, HL).	ZF		

Note 1: If multiple CLA instructions are used in a row, only the execution of the instructions following the first CLA can be skipped.

Mnemonic	Op code	D ₇ D ₆ D ₅ D ₄	D ₃ D ₂ D ₁ D ₀	Bytes	Cycles	Operations	Operations description	Affected flag(s)	Remarks																
										Op code															
CM	Compare AC with M	0 0 0 1	0 1 1 0	1	1	$(M(\text{MBR,HL})) + (\text{AO}) + 1$	Compare the AC content with that of M(MBR,HL) and set or reset the carry flag (CF) and the zero flag (ZF). <table border="1"> <tr><td colspan="2">Compare operations</td><td>CF</td><td>ZF</td></tr> <tr><td>$(M(\text{MBR,HL})) > (\text{AC})$</td><td></td><td>0</td><td>0</td></tr> <tr><td>$(M(\text{MBR,HL})) = (\text{AC})$</td><td></td><td>1</td><td>1</td></tr> <tr><td>$(M(\text{MBR,HL})) < (\text{AC})$</td><td></td><td>1</td><td>0</td></tr> </table>	Compare operations		CF	ZF	$(M(\text{MBR,HL})) > (\text{AC})$		0	0	$(M(\text{MBR,HL})) = (\text{AC})$		1	1	$(M(\text{MBR,HL})) < (\text{AC})$		1	0	ZF, CF	
Compare operations		CF	ZF																						
$(M(\text{MBR,HL})) > (\text{AC})$		0	0																						
$(M(\text{MBR,HL})) = (\text{AC})$		1	1																						
$(M(\text{MBR,HL})) < (\text{AC})$		1	0																						
CI i4	Compare AC with immediate data	1 1 0 0 1 0 1 0	1 1 1 1 i ₃ i ₂ i ₁ i ₀	2	2	$i_3 i_2 i_1 i_0 + (\text{AC}) + 1$	Compare the AC content with immediate data (i ₃ i ₂ i ₁ i ₀) and set or reset the carry flag (CF) and the zero flag (ZF). <table border="1"> <tr><td colspan="2">Compare operations</td><td>CF</td><td>ZF</td></tr> <tr><td>$i_3 i_2 i_1 i_0 > (\text{AC})$</td><td></td><td>0</td><td>0</td></tr> <tr><td>$i_3 i_2 i_1 i_0 = (\text{AC})$</td><td></td><td>1</td><td>1</td></tr> <tr><td>$i_3 i_2 i_1 i_0 < (\text{AC})$</td><td></td><td>1</td><td>0</td></tr> </table>	Compare operations		CF	ZF	$i_3 i_2 i_1 i_0 > (\text{AC})$		0	0	$i_3 i_2 i_1 i_0 = (\text{AC})$		1	1	$i_3 i_2 i_1 i_0 < (\text{AC})$		1	0	ZF, CF	
Compare operations		CF	ZF																						
$i_3 i_2 i_1 i_0 > (\text{AC})$		0	0																						
$i_3 i_2 i_1 i_0 = (\text{AC})$		1	1																						
$i_3 i_2 i_1 i_0 < (\text{AC})$		1	0																						
CLI i4	Compare DP _L with immediate data	1 1 0 0 1 0 1 1	1 1 1 1 i ₃ i ₂ i ₁ i ₀	2	2	ZF ← 1 if (DP _L) = i ₃ i ₂ i ₁ i ₀ ZF ← 0 if (DP _L) ≠ i ₃ i ₂ i ₁ i ₀	Compare the DP _L content with immediate data (i ₃ i ₂ i ₁ i ₀). If they are equal to each other, the zero flag (ZF) will be set. Otherwise, the flag will be reset.	ZF																	
CMB i2	Compare AC bit with M data bit	1 1 0 0 1 1 0 1	1 1 1 1 0 0 t ₁ t ₀	2	2	ZF ← 1 if (AC, t ₂) = (M (MBR,HL), t ₂) ZF ← 0 if (AC, t ₂) ≠ (M (MBR,HL), t ₂)	Compare the AC content with the content of a bit of M(MBR,HL), specified by the two LSBs (t ₁ t ₀). If they are equal to each other, the zero flag (ZF) will be set. Otherwise, it will be reset.	ZF																	
LAE	Load AC and E from M2 (MBR,HL)	0 1 0 1	1 1 0 0	1	1	AC ← M(MBR,HL) E ← M(MBR,HL + 1)	Load the content of M(MBR,HL) into the AC and the E register.																		
LAI i4	Load AC with immediate data	1 0 0 0	i ₃ i ₂ i ₁ i ₀	1	1	AC ← i ₃ i ₂ i ₁ i ₀	Load immediate data into the AC.	ZF	Note 1																
LADR i8	Load AC from M direct	1 1 0 0 i ₇ i ₆ i ₅ i ₄	0 0 0 1 i ₃ i ₂ i ₁ i ₀	2	2	AC ← (M(MBR, i ₈))	Load the content of M(MBR, i ₈) into the AC. Note that i ₈ means 8-bit immediate data.	ZF																	
S	Store AC to M	0 1 0 0	0 1 1 1	1	1	M(MBR,HL) ← (AC)	Store the AC content into M(MBR,HL).																		
SAE	Store AC and E to M2 (MBR,HL)	0 1 0 1	1 1 1 0	1	1	M(MBR,HL) ← (AC) M(MBR,HL + 1) ← (E)	Store the content of M2(MBR,HL) into the AC and the E register.																		
LA reg	Load AC from M (MBR,reg)	0 1 0 0	1 0 t ₀ 0	1	1	AC ← (M(MBR,reg))	Load the content of M(MBR,reg) into the AC. Note that 'reg' indicates the HL or XY.	ZF																	
LA reg, i	Load AC from M (MBR,reg) then increment reg	0 1 0 0	1 0 t ₀ 1	1	2	AC ← (M(MBR,reg)) DP _L ← (DP _L) + 1 Or i ₂ DP _Y ← (DP _Y) + 1	Load the content of M(MBR,reg) into the AC. Note that 'reg' indicates the HL or XY. After loading, the content of DP _L or DP _Y will be incremented by 1. The relationship between reg and t ₀ is the same as that shown in the LA reg instruction.	ZF	The zero flag (ZF) will be set or reset accordingly after the content of the DP _L or the DP _Y is incremented by 1.																
LA reg, D	Load AC from M (MBR,reg) then decrement reg	0 1 0 1	1 0 t ₀ 1	1	2	AC ← (M(MBR,reg)) DP _L ← (DP _L) - 1 Or DP _Y ← (DP _Y) - 1	Load the content of M(MBR,reg) into the AC. Note that 'reg' indicates the HL or XY. After loading, the content of DP _L or DP _Y will be decremented by 1. The relationship between reg and t ₀ is the same as that shown in the LA reg instruction.	ZF	The zero flag (ZF) will be set or reset accordingly after the content of the DP _L or the DP _Y is decremented by 1.																
XA reg	Exchange AC with M(MBR,reg)	0 1 0 0	1 1 t ₀ 0	1	1	(AC) ↔ (M(MBR,reg))	Exchange the AC content with that of M(MBR,reg). Note that 'reg' indicates the HL or XY.																		
XA reg, i	Exchange AC with M (MBR,reg) then increment reg	0 1 0 0	1 1 t ₀ 1	1	2	(AC) ↔ (M(MBR,reg)) DP _L ← (DP _L) + 1 Or i ₂ DP _Y ← (DP _Y) + 1	Exchange the AC content with that of M(MBR,reg). Note that 'reg' indicates the HL or XY. After exchange, the content of the DP _L or the DP _Y will be incremented by 1. The relationship between reg and t ₀ is the same as that shown in the LA reg instruction.	ZF	The zero flag (ZF) will be set or reset accordingly after the content of the DP _L or the DP _Y is incremented by 1.																
XA reg, D	Exchange AC with M (MBR,reg) then decrement reg	0 1 0 1	1 1 t ₀ 1	1	2	(AC) ↔ (M(MBR,reg)) DP _L ← (DP _L) - 1 Or DP _Y ← (DP _Y) - 1	Exchange the AC content with that of M(MBR,reg). Note that 'reg' indicates the HL or XY. After exchange, the content of the DP _L or the DP _Y will be decremented by 1. The relationship between reg and t ₀ is the same as that shown in the LA reg instruction.	ZF	The zero flag (ZF) will be set or reset accordingly after the content of the DP _L or the DP _Y is decremented by 1.																
XADR i8	Exchange AC with M direct	1 1 0 0 i ₇ i ₆ i ₅ i ₄	1 0 0 0 i ₃ i ₂ i ₁ i ₀	2	2	(AC) ↔ (M(MBR, i ₈))	Exchange the AC content with the that of M(MBR, i ₈). Note that i ₈ means 8-bit immediate data.																		

Note 1: If multiple LAI i4 instructions are used in a row, the execution of the instructions following the first LAI instruction can be skipped.

LC67216A

T-49-19-04

Instruction	Mnemonic		Op code				Bytes	Cycles	Operations	Operations description	Affected flag(s)	Remarks
			D ₇ D ₆ D ₅ D ₄	D ₃ D ₂ D ₁ D ₀								
Load and Store Instructions	LEAI r8	Load E & AC with immediate data	1 1 0 0 l ₇ l ₆ l ₅ l ₄	0 1 1 0 l ₃ l ₂ l ₁ l ₀	2	2	E ← l ₇ l ₆ l ₅ l ₄ AC ← l ₃ l ₂ l ₁ l ₀	Load immediate data l8 into the AC and the E register.				
	RTBL	Read table data from program ROM	0 1 0 1	1 0 1 0	1	2	E, AC ← (ROM(PCh, E, AC))	Replace the lower PC 8 bits with the E and AC contents. Then load the content of a ROM address specified by the PC content into the AC and the E register.				
Data Pointer Manipulation Instructions	LZD r4	Load DP _H with zero and DP _L with immediate data respectively	0 1 1 0	l ₃ l ₂ l ₁ l ₀	1	1	DP _H ← 0 DP _L ← l ₃ l ₂ l ₁ l ₀	Load 0 into the DP _H and immediate data l4 into the DP _L .				
	LHI r4	Load DP _H with immediate data	1 1 0 0 0 0 0 0	l ₃ l ₂ l ₁ l ₀	2	2	DP _H ← l ₃ l ₂ l ₁ l ₀	Load immediate data l4 into the DP _H .				
	LLI r4	Load DP _L with immediate data	1 1 0 0 0 0 0 1	l ₃ l ₂ l ₁ l ₀	2	2	DP _L ← l ₃ l ₂ l ₁ l ₀	Load immediate data l4 into the DP _L .				
	LHLI r8	Load DP _H , DP _L with immediate data	1 1 0 0 l ₇ l ₆ l ₅ l ₄	0 0 0 0 l ₃ l ₂ l ₁ l ₀	2	2	DP _H ← l ₇ l ₆ l ₅ l ₄ DP _L ← l ₃ l ₂ l ₁ l ₀	Load immediate data into the DP _H and the DP _L .				
	LXYI r8	Load DP _X , DP _Y with immediate data	1 1 0 0 l ₇ l ₆ l ₅ l ₄	0 0 1 0 l ₃ l ₂ l ₁ l ₀	2	2	DP _X ← l ₇ l ₆ l ₅ l ₄ DP _Y ← l ₃ l ₂ l ₁ l ₀	Load immediate data into the DP _X and the DP _Y .				
	IL	Increment DP _L	0 0 0 1	0 0 0 1	1	1	DP _L ← (DP _L) + 1	Increment the DP _L by 1.	ZF			
	DL	Decrement DP _L	0 0 1 0	0 0 0 1	1	1	DP _L ← (DP _L) - 1	Decrement the DP _L by 1.	ZF			
	IY	Increment DP _Y	0 0 0 1	0 0 1 1	1	1	DP _Y ← (DP _Y) + 1	Increment the DP _Y by 1.	ZF			
	DY	Decrement DP _Y	0 0 1 0	0 0 1 1	1	1	DP _Y ← (DP _Y) - 1	Decrement the DP _Y by 1.	ZF			
	TAH	Transfer AC to DP _H	1 1 0 0 1 1 1 1	1 1 1 1 0 0 0 0	2	2	DP _H ← (AC)	Transfer the AC content into the DP _H .				
	THA	Transfer DP _H to AC	1 1 0 0 1 1 1 0	1 1 1 1 0 0 0 0	2	2	AC ← (DP _H)	Transfer the DP _H content into the AC.	ZF			
	XAH	Exchange AC with DP _H	0 1 0 0	0 0 0 0	1	1	(AC) ↔ (DP _H)	Exchange AC content with that of the DP _H .				
	TAL	Transfer AC to DP _L	1 1 0 0 1 1 1 1	1 1 1 1 0 0 0 1	2	2	DP _L ← (AC)	Transfer the AC content into the DP _L .				
	TAL	Transfer DP _L to AC	1 1 0 0 1 1 1 0	1 1 1 1 0 0 0 1	2	2	AC ← (DP _L)	Transfer the DP _L content into the AC.	ZF			
	XAL	Exchange AC with DP _L	0 1 0 0	0 0 0 1	1	1	(AC) ↔ (DP _L)	Exchange the AC content with that of the DP _L .				
	TAX	Transfer AC to DP _X	1 1 0 0 1 1 1 1	1 1 1 1 0 0 1 0	2	2	DP _X ← (AC)	Transfer the AC content into the DP _X .				
	TXA	Transfer DP _X to AC	1 1 0 0 1 1 1 0	1 1 1 1 0 0 1 0	2	2	AC ← (DP _X)	Transfer the DP _X content into the AC.	ZF			
	XAX	Exchange AC with DP _X	0 1 0 0	0 0 1 0	1	1	(AC) ↔ (DP _X)	Exchange the AC content with that of the DP _X .				
	TAY	Transfer AC to DP _Y	1 1 0 0 1 1 1 1	1 1 1 1 0 0 1 1	2	2	DP _Y ← (AC)	Transfer the AC content into the DP _Y .				
	TYA	Transfer DP _Y to AC	1 1 0 0 1 1 1 0	1 1 1 1 0 0 1 1	2	2	AC ← (DP _Y)	Transfer the DP _Y content into the AC.	ZF			
XAY	Exchange AC with DP _Y	0 1 0 0	0 0 1 1	1	1	(AC) ↔ (DP _Y)	Exchange the AC content with that of the DP _Y .					
Flag Manipulation Instructions	SFB r4	Set flag bit	0 1 1 1	n ₃ n ₂ n ₁ n ₀	1	1	Fn ← 1	Set the flag specified by immediate data r4.				
	RFB r4	Reset flag bit	0 0 1 1	n ₃ n ₂ n ₁ n ₀	1	1	Fn ← 0	Reset the flag specified by immediate data r4.	ZF			
Jump and Subroutine Instructions	JMP addr	Jump in the current bank	1 1 1 0 P ₇ P ₆ P ₅ P ₄	P ₁₁ P ₁₀ P ₉ P ₈ P ₃ P ₂ P ₁ P ₀	2	2	PC13-PC13 PC11-0 ← P ₁₁ -P ₀	Program jump to an address within the same bank area, specified by immediate data P ₁₁ to P ₀ .			If this instruction is executed immediately after the SB instruction, the upper bits P ₁₁ to P ₁₀ (P ₁₁ and P ₁₀) are replaced by immediate data l10. See the SB instruction for more details.	
	JPEA	Jump to the address stored at E and AC in the current page	0 0 1 0	0 1 1 1	1	1	PC13-PC8 ← PC13-PC8 PC7-4 ← (E) PC3-0 ← (AC)	Replace the lower 8 PC bits with the AC and the E register contents and jump to an address pointed to by the new program counter (PC) value.				

Instruction group	Mnemonic	Op code		Bytes	Cycles	Operations	Operations description	Affected flag(s)	Remarks															
		D ₇ D ₆ D ₅ D ₄	D ₃ D ₂ D ₁ D ₀																					
Jump and Subroutine Instructions	CAL addr	Call subroutine	1 0 1 0 P ₇ P ₆ P ₅ P ₄	P ₁₁ P ₁₀ P ₉ P ₈ P ₃ P ₂ P ₁ P ₀	2	2	PC13, 12-0 PC11-0-P ₁₁ -P ₈ M4(SP)-(CF, ZF, PC13-0) SP-(SP)-4	Call a subroutine.																
	PUSH reg	Push reg on M2(SP)	1 1 0 0 1 1 1 1	1 1 1 1 1 i ₁ i ₀ 0	2	2	M2(SP)-(reg) SP-(SP)-2	Store the 'reg' content into the M2(SP) and then decrement the SP content by 2. <table border="1" style="margin-left: 20px;"> <tr> <td>reg</td> <td>i₁</td> <td>i₀</td> </tr> <tr> <td>HL</td> <td>0</td> <td>0</td> </tr> <tr> <td>XY</td> <td>0</td> <td>1</td> </tr> <tr> <td>AE</td> <td>1</td> <td>0</td> </tr> <tr> <td>BR</td> <td>1</td> <td>1</td> </tr> </table>	reg	i ₁	i ₀	HL	0	0	XY	0	1	AE	1	0	BR	1	1	
	reg	i ₁	i ₀																					
	HL	0	0																					
	XY	0	1																					
AE	1	0																						
BR	1	1																						
POP reg	Pop reg off M2(SP)	1 1 0 0 1 1 1 0	1 1 1 1 1 i ₁ i ₀ 0	2	2	SP-(SP)+2 reg-(M2(SP))	Increment the SP content by 2 and then load the content of M2(SP) into the 'reg'. The relationship between the 'i ₁ ' and 'i ₀ ' is the same as that shown in PUSH reg instruction.																	
RT	Return from subroutine	0 0 0 1	1 1 0 0	1	2	SP-(SP)+4 PC-(M4(SP))	Return to a main routine from a subroutine or interrupt servicing routine. The zero flag (ZF) and the carry flag (CF) are not affected by this instruction.																	
RTI	Return from interrupt routine	0 0 0 1	1 1 0 1	1	2	SP-(SP)+4 PC-(M4(SP)) CF, ZF-(M4(SP))	Return to a main routine from a subroutine or interrupt servicing routine. The previous contents of the ZF and CF are restored.	ZF, CF																
Branch Instructions	BAI2 addr	Branch on AC bit	1 1 0 1 P ₇ P ₆ P ₅ P ₄	0 0 i ₁ i ₀ P ₃ P ₂ P ₁ P ₀	2	2	PC7-0-P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if(AC, i ₂) = 1	Check an AC bit specified by immediate data i ₁ i ₀ to see if it has been set to '1'. If set to '1', program execution is passed to an address within the same page. Note the address is specified by the lower 8 PC bits (P ₇ to P ₀).																
	BNAI2 addr	Branch on no AC bit	1 0 0 1 P ₇ P ₆ P ₅ P ₄	0 0 i ₁ i ₀ P ₃ P ₂ P ₁ P ₀	2	2	PC7-0-P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if(AC, i ₂) = 0	Check an AC bit specified by immediate data i ₁ i ₀ to see if it has been set to '0'. If set to '0', program execution is passed to an address within the same page. Note the address is specified by the lower 8 PC bits (P ₇ to P ₀).																
	BMI2 addr	Branch on M bit	1 1 0 1 P ₇ P ₆ P ₅ P ₄	0 1 i ₁ i ₀ P ₃ P ₂ P ₁ P ₀	2	2	PC7-0-P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if(M(MBR, HL), i ₂) = 1	Check an M(MBR, HL) bit specified by immediate data i ₁ i ₀ to see if it has been set to '1'. If set to '1', program execution is passed to an address within the same page. Note the address is specified by the lower 8 PC bits (P ₇ to P ₀).																
	BNMI2 addr	Branch on no M bit	1 0 0 1 P ₇ P ₆ P ₅ P ₄	0 1 i ₁ i ₀ P ₃ P ₂ P ₁ P ₀	2	2	PC7-0-P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if(M(MBR, HL), i ₂) = 0	Check an M(MBR, HL) bit specified by immediate data i ₁ i ₀ to see if it has been set to '0'. If set to '0', program execution is passed to an address within the same page. Note the address is specified by the lower 8 PC bits (P ₇ to P ₀).																
	BPI2 addr	Branch on Port bit	1 1 0 1 P ₇ P ₆ P ₅ P ₄	1 0 i ₁ i ₀ P ₃ P ₂ P ₁ P ₀	2	2	PC7-0-P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if(P(RBR, DP _L), i ₂) = 1	Check a port or register (RBR, DP _L) bit specified by immediate data i ₁ i ₀ to see if it has been set to '1'. If set to '1', program execution is passed to an address within the same page. Note the address is specified by the lower 8 PC bits (P ₇ to P ₀).																
	BNPI2 addr	Branch on no Port bit	1 0 0 1 P ₇ P ₆ P ₅ P ₄	1 0 i ₁ i ₀ P ₃ P ₂ P ₁ P ₀	2	2	PC7-0-P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if(P(RBR, DP _L), i ₂) = 0	Check a port or register (RBR, DP _L) bit specified by immediate data i ₁ i ₀ to see if it has been set to '0'. If set to '0', program execution is passed to an address within the same page. Note the address is specified by the lower 8 PC bits (P ₇ to P ₀).																
	BC addr	Branch on CF	1 1 0 1 P ₇ P ₆ P ₅ P ₄	1 1 0 0 P ₃ P ₂ P ₁ P ₀	2	2	PC7-0-P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if(CF) = 1	Check the carry flag (CF) to see if it has been set to '1'. If set to '1', program execution is passed to an address within the same page. Note that the address is specified by the lower 8 PC bits (P ₇ to P ₀).																
	BNC addr	Branch on no CF	1 0 0 1 P ₇ P ₆ P ₅ P ₄	1 1 0 0 P ₃ P ₂ P ₁ P ₀	2	2	PC7-0-P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if(CF) = 0	Check the carry flag (CF) to see if it has been set to '0'. If set to '0', program execution is passed to an address within the same page. Note that the address is specified by the lower 8 PC bits (P ₇ to P ₀).																
	BZ addr	Branch on ZF	1 1 0 1 P ₇ P ₆ P ₅ P ₄	1 1 0 1 P ₃ P ₂ P ₁ P ₀	2	2	PC7-0-P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if(ZF) = 1	Check the zero flag (ZF) to see if it has been set to '1'. If set to '1', program execution is passed to an address within the same page. Note that the address is specified by the lower 8 PC bits (P ₇ to P ₀).																
	BNZ addr	Branch on no ZF	1 0 0 1 P ₇ P ₆ P ₅ P ₄	1 1 0 1 P ₃ P ₂ P ₁ P ₀	2	2	PC7-0-P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ if(ZF) = 0	Check the zero flag (ZF) to see if it has been set to '0'. If set to '0', program execution is passed to an address within the same page. Note that the address is specified by the lower 8 PC bits (P ₇ to P ₀).																

LC67216A

T-49-19-04

Instruction group	Mnemonic	Op code		Bytes	Cycles	Operations	Operations description	Affected flag(s)	Remarks
		D ₇ D ₆ D ₅ D ₄	D ₃ D ₂ D ₁ D ₀						
Branch instructions	BFn4 addr	1 1 1 1 P ₇ P ₆ P ₅ P ₄	n ₃ n ₂ n ₁ n ₀ P ₃ P ₂ P ₁ P ₀	2	2	PC7-0 ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ If(Fn) = 1	Check a flag specified by n ₀ n ₁ n ₂ n ₃ to see if it has been set to '1'. If set to '1', program execution is passed to an address within the same page. Note that the total number of specifiable flags is 16 and that the address is specified by the lower 8 PC bits (P ₇ to P ₀).		
	BNFn4 addr	1 0 1 1 P ₇ P ₆ P ₅ P ₄	n ₃ n ₂ n ₁ n ₀ P ₃ P ₂ P ₁ P ₀	2	2	PC7-0 ← P ₇ P ₆ P ₅ P ₄ P ₃ P ₂ P ₁ P ₀ If(Fn) = 0	Check a flag specified by n ₀ n ₁ n ₂ n ₃ to see if it has been set to '0'. If set to '0', program execution is passed to an address within the same page. Note that the total number of specifiable flags is 16 and that the address is specified by the lower 8 PC bits (P ₇ to P ₀).		
Input/output instructions	IP0	0 0 1 0	0 0 0 0	1	1	AC ← (P(RBR, 0))	Input the content of port or register P(RBR, 0) to the AC.	ZF	
	IP	0 0 1 0	0 1 1 0	1	1	AC ← (P(RBR, DP _L))	Input the content of port or register P(RBR, DP _L) to the AC.	ZF	
	IPM	0 0 0 1	1 0 0 1	1	1	M(HL) ← (P(RBR, DP _L))	Input the content of port or register P(RBR, DP _L) to M(MBR, HL).		
	IPDRP4	1 1 0 0 0 1 1 0	1 1 1 1 P ₃ P ₂ P ₁ P ₀	2	2	AC ← (P(RBR, P ₄))	Input the content of P(RBR, P ₄) to the AC.	ZF	
	OP	0 0 1 0	0 1 0 1	1	1	P(RBR, DP _L) ← (AO)	Output the AC content to port or register P(RBR, DP _L).		
	OPM	0 0 0 1	1 0 1 0	1	1	P(RBR, DP _L) ← (M(MBR, HL))	Output the content of M(MBR, HL) to port P(RBR, DP _L).		
	OPDRP4	1 1 0 0 0 1 1 1	1 1 1 1 P ₃ P ₂ P ₁ P ₀	2	2	P(RBR, P ₄) ← (AC)	Output the AC content to P(RBR, P ₄).		
	SPB i2	0 0 0 0	1 0 i ₁ i ₀	1	1	(P(RBR, DP _L), i2) ← 1	Set a specified bit of port or register P(RBR, DP _L). Note that the bit is specified by immediate data i ₁ i ₀ .		
	RPB i2	0 0 1 0	1 0 i ₁ i ₀	1	1	(P(RBR, DP _L), i2) ← 0	Reset a specified bit of port or register P(RBR, DP _L). Note that the bit is specified by immediate data i ₁ i ₀ .	ZF	
	ANDPDR i ₄ , p ₄	1 1 0 0 i ₃ i ₂ i ₁ i ₀	0 1 0 1 P ₃ P ₂ P ₁ P ₀	2	2	P(RBR, P ₃ -P ₀) ← (P(RBR, P ₃ -P ₀) & i ₃ ~i ₀)	Logically AND the content of P(RBR, P ₃ to P ₀) with immediate data i ₃ i ₂ i ₁ i ₀ and then output the resulted logical product to P(RBR, P ₃ to P ₀).	ZF	
	ORPDR i ₄ , p ₄	1 1 0 0 i ₃ i ₂ i ₁ i ₀	0 1 0 0 P ₃ P ₂ P ₁ P ₀	2	2	P(RBR, P ₃ -P ₀) ← (P(RBR, P ₃ -P ₀) i ₃ ~i ₀)	Logically OR the content of P(RBR, P ₃ to P ₀) with immediate data i ₃ i ₂ i ₁ i ₀ and then output the resulted logical product to P(RBR, P ₃ to P ₀).	ZF	
	IP8	Input 8bit data to E and AC	1 1 0 0 1 1 0 1	1 1 1 1 1 0 0 0	2	2	AC ← (P(RBR, DP _L))	Input 8-bit data to the AC and E register from a port or register P(RBR, DP _L).	
OP8	Output 8bit E and AC to Port	1 1 0 0 1 1 0 1	1 1 1 1 1 0 0 1	2	2	P(RBR, DP _L) ← (AC), (E)	Output 8-bit data to a port or register P(RBR, DP _L) from the AC and the E register.		

Instruction group	Mnemonic		Op code		Bytes	Cycles	Operations	Operations description	Affected flag(s)	Remarks
			D ₇ D ₆ D ₅ D ₄	D ₃ D ₂ D ₁ D ₀						
Interrupt control instructions	MSET	Set Interrupt Master Enable Flag	1 1 0 0 0 1 0 1	1 1 0 1 0 0 0 0	2	2	MSE ← 1	Set the interrupt master enable flag.		
	MRESET	Reset Interrupt Master Enable Flag	1 1 0 0 1 0 0 1	1 1 0 1 0 0 0 0	2	2	MSE ← 0	Reset the interrupt master enable flag.	ZF	
	EIH i4	Enable interrupt high	1 1 0 0 0 1 0 1	1 1 0 1 i ₃ i ₂ i ₁ i ₀	2	2	EDIH ← (EDIH) ∨ i ₄	Set the interrupt enable flag.		
	EIL i4	Enable interrupt low	1 1 0 0 0 1 0 0	1 1 0 1 i ₃ i ₂ i ₁ i ₀	2	2	EDIL ← (EDIL) ∨ i ₄	Set the interrupt enable flag.		
	DIH i4	Disable interrupt high	1 1 0 0 1 0 0 1	1 1 0 1 i ₃ i ₂ i ₁ i ₀	2	2	EDIH ← (EDIH) ∧ i ₄	Reset the interrupt enable flag.	ZF	
	DIL i4	Disable interrupt low	1 1 0 0 1 0 0 0	1 1 0 1 i ₃ i ₂ i ₁ i ₀	2	2	EDIL ← (EDIL) ∧ i ₄	Reset the interrupt enable flag.	ZF	
	WTSP	Write SP	1 1 0 0 1 1 0 1	1 1 1 1 1 0 1 0	2	2	SP ← (E), (AC)	Transfer the contents of the AC and the E register to the SP.		
	RSP	Read SP	1 1 0 0 1 1 0 1	1 1 1 1 1 0 1 1	2	2	E, AC ← (SP)	Transfer the SP content to the AC and the E register.		
Standby control instructions	HALT	HALT	1 1 0 0 1 1 0 1 0 0 0 0	1 1 1 1 1 1 1 0 0 0 0 0	3	3	HALT	Start the HALT mode.		
	HOLD	HOLD	1 1 0 0 1 1 0 1 0 0 0 0	1 1 1 1 1 1 1 1 0 0 0 0	3	3	HOLD	Start the HOLD mode.		
Other instructions	NOP	No operation	0 0 0 0	0 0 0 0	1	1	No operation	Nothing will be done during 1 machine cycle.		
	SB i3	Select bank	0 1 0 1	D ₁ i ₂ i ₁ i ₀	1	1	PC13, PC12 ← i ₁ i ₀	SB ← JMP: The two PG MSBs (P13 and P12) are replaced with immediate data i ₁ i ₀ . SB ← SRBA: Immediate data i ₂ i ₁ i ₀ will be set in the RBR. SB ← SMBA: Immediate data i ₂ i ₁ i ₀ will be set in the MBR.		
	SRBA	Set Register Bank Address	1 1 0 0	1 0 1 1	1	1	RBR ← i ₂ i ₁ i ₀	SB ← SRBA: Immediate data i ₂ i ₁ i ₀ will be set in the RBR.		
	SMBA	Set Memory Bank Address	1 1 0 0	1 0 1 0	1	1	MBR ← i ₂ i ₁ i ₀	SB ← SMBA: Immediate data i ₂ i ₁ i ₀ will be set in the MBR.		

Option code specification for the LC67216A microcomputer

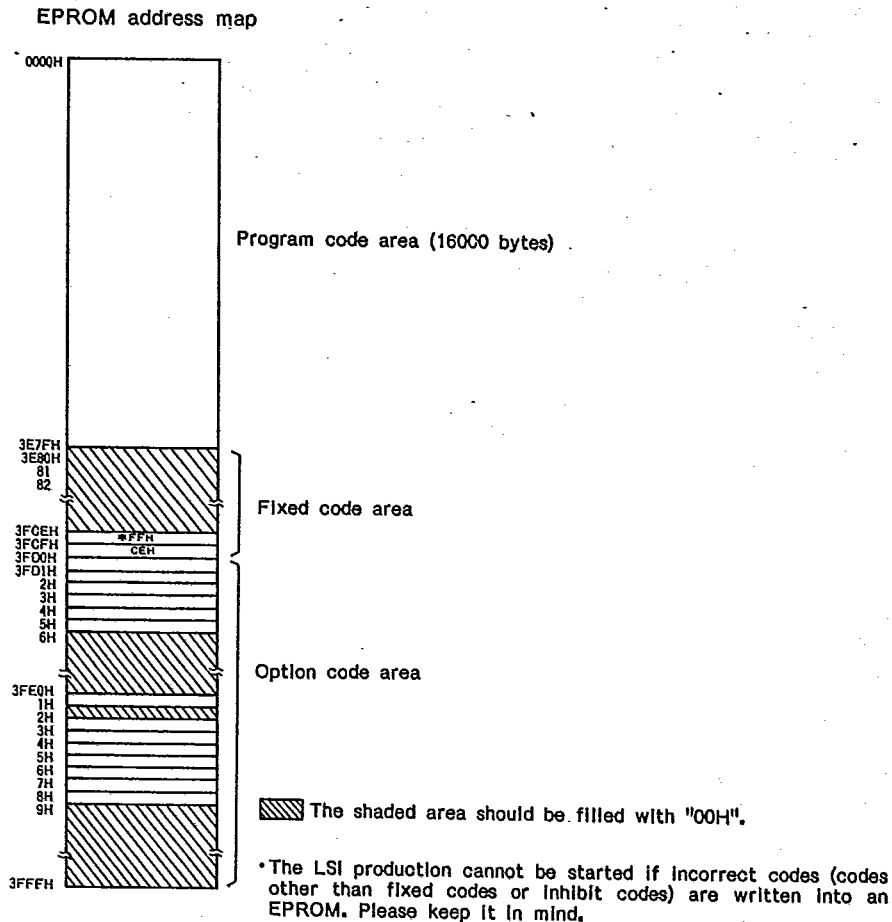
The EPROM which is to be sent to Sanyo should contain various mask option codes and program codes for the LC67216A microcomputer.

In order to write option codes into the EPROM, we provide the LC67216A cross assembler. This cross assembler would enable the user to enter the option codes in interactive operation mode.

In case where the cross assembler provided by Sanyo is not used for the above purpose, the required option codes should be entered in the following manner. If you enter the codes in the manner, the same option codes as those generated by the LC67216A cross assembler can be set in the EPROM.

When placing your order, please provide us with an option code list and the EPROM (27128) containing program codes and option codes.

For detailed information on the option codes, please refer to section 9, "Specifying User Options" of the manual, 'EVA850/800-LC67216 Development Tool Manual'. However, the main clock oscillation circuit option for the RC (resistor- capacitor) oscillation is not provided for the LC67216A microcomputer. Please keep it in mind.



Notes on the evaluation of user programs for the LC67216A microcomputer

If the user programs for the LC67216A microcomputer are evaluated on the evaluation chip (LC67999 or LC67PG216), please read carefully section 5.3 "considerations in Program Evaluation" of the 'LC67216A User's Manual'. In addition, please keep in mind the following cautions.

Notes on program code area: The program code area of the production chip is 16000 bytes in size. That is, its address starts from address 0000H, ending at address 3E7FH. However, the accessible area of an evaluation chip is in the range between address 0000H and address 3FFFH. That is, it can be said that the program code area of the evaluation chip is 16383 bytes in size. As a result, the code area after address 3E80H should not be used for storing program codes. Please keep the following two points in mind.

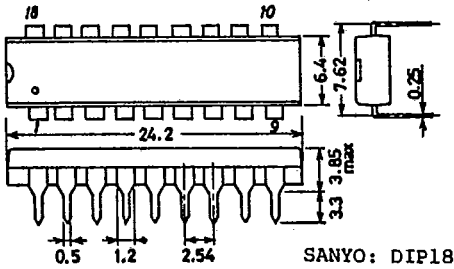
- (1) No program codes in the area after address 3E80H.
- (2) No program jump to the area after address 3E80H.

T-90-20

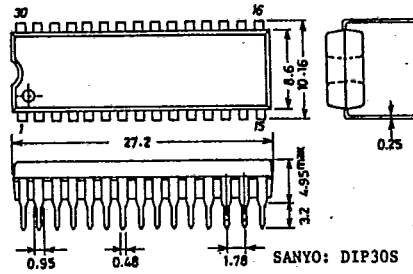
CASE OUTLINES OF 8/4-BIT MICROCOMPUTERS, GATE ARRAYS

- All of Sanyo microcomputer case outlines are illustrated below.
- All dimensions are in mm, and dimensions which are not followed by min. or max. are represented by typical values.
- No marking is indicated.

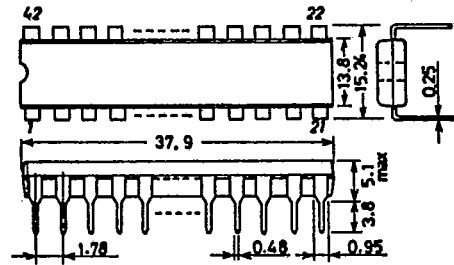
Case Outline—[3007A] unit: mm



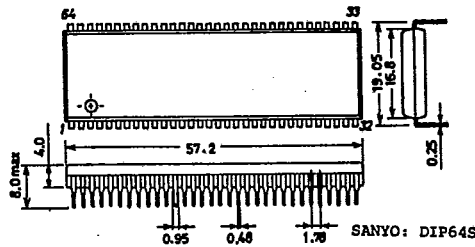
Case Outline—[3061] unit: mm



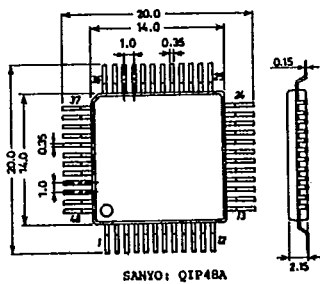
Case Outline—[3025B] unit: mm



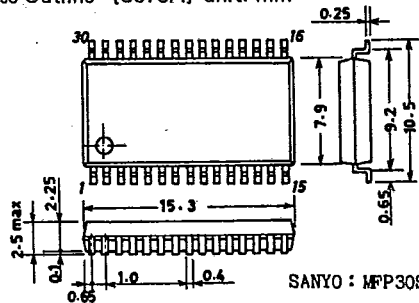
Case Outline—[3071] unit: mm



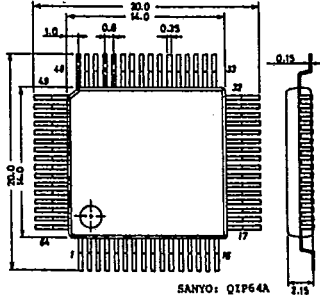
Case Outline—[3052A] unit: mm



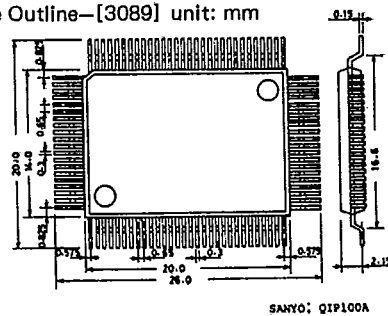
Case Outline—[3073A] unit: mm



Case Outline—[3057] unit: mm

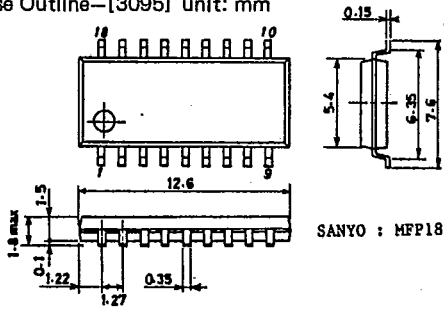


Case Outline—[3089] unit: mm



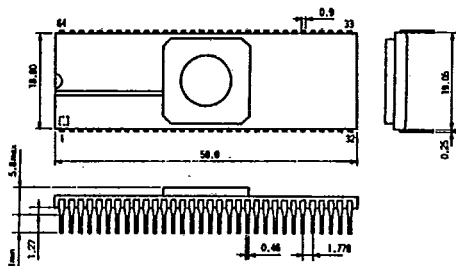
T-90-20

Case Outline-[3095] unit: mm



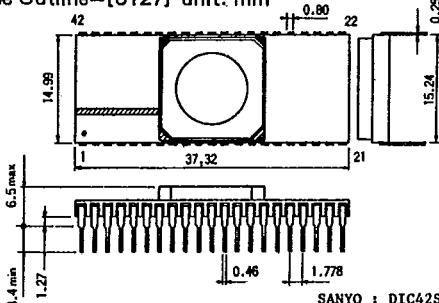
SANYO : MFP18

Case Outline-[3126] unit: mm



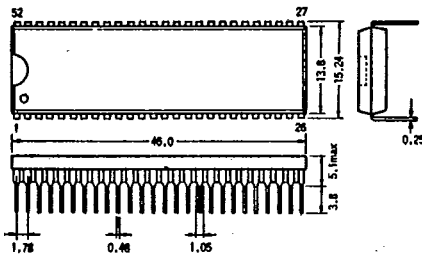
SANYO : DIC64S

Case Outline-[3127] unit: mm



SANYO : DIC42S

Case Outline-[3128] unit: mm



SANYO : DIP52S