

1/2-Inch Megapixel CMOS Digital Image Sensor

MT9M001C12STM (Monochrome)

For the latest data sheet, refer to Micron's Web site: www.micron.com/imaging

Features

- DigitalClarity™ CMOS Imaging Technology
- Array Format (5:4): 1,280H x 1,024V (1,310,720 active pixels). Total (incl. dark pixels): 1,312H x 1,048V (1,374,976 pixels)
- Frame Rate: 30 fps progressive scan; programmable
- Shutter: Electronic Rolling Shutter (ERS)
- Window Size: SXGA; programmable to any smaller format (VGA, QVGA, CIF, QCIF, etc.)
- Programmable Controls: Gain, frame rate, frame size

Applications

- Digital still cameras
- Digital video cameras
- PC cameras

General Description

The Micron® Imaging MT9M001 is an SXGA-format with a 1/2-inch CMOS active-pixel digital image sensor. The active imaging pixel array of 1,280H x 1,024V. It incorporates sophisticated camera functions on-chip such as windowing, column and row skip mode, and snapshot mode. It is programmable through a simple two-wire serial interface.

This megapixel CMOS image sensor features DigitalClarity—Micron's breakthrough low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

Table 1: Key Performance Parameters

Parameter		Typical Value
Optical format		1/2-inch (5:4)
Active imager size		6.66mm(H) x 5.32mm(V)
Active pixels		1,280H x 1,024V
Pixel size		5.2µm x 5.2µm
Shutter type		Electronic rolling shutter (ERS)
Maximum data rate/ master clock		48 MPS/48 MHz
Frame rate	SXGA (1280 x 1024)	30 fps progressive scan; programmable
ADC resolution		10-bit, on-chip
Responsivity		2.1 V/lux-sec
Dynamic range		68.2dB
SNR _{MAX}		45dB
Supply voltage		3.0V–3.6V, 3.3V nominal
Power consumption		325mW at 3.3V; Standby 275µW
Operating temperature		0°C to +70°C
Packaging		48-pin CLCC

The sensor can be operated in its default mode or programmed by the user for frame size, exposure, gain setting, and other parameters. The default mode outputs an SXGA-size image at 30 frames per second (fps). An on-chip analog-to-digital converter (ADC) provides 10 bits per pixel. FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a pixel clock that is synchronous with valid data.

Ordering Information

Table 2: Available Part Numbers

Part Number	Description
MT9M001C12STM	46-pin CLCC



Table of Contents

Applications	1
General Description	1
Ordering Information	1
List of Tables	3
List of Figures	4
General Description	5
Pixel Data Format	7
Pixel Array Structure	7
Output Data Format	7
Output Data Timing	8
Frame Timing Formulas	9
Serial Bus Description	10
Protocol	10
Sequence	10
Bus Idle State	10
Start Bit	10
Stop Bit	10
Slave Address	11
Data Bit Transfer	11
Acknowledge Bit	11
No-Acknowledge Bit	11
Two-Wire Serial Interface Sample Write and Read Sequences	12
16-Bit Write Sequence	12
16-Bit Read Sequence	12
Registers	13
Register Map	13
Feature Description	20
Signal Path	20
Programmable Gain Stage	20
Programmable Analog Offset Stage	21
Column and Row Mirror Image	21
Column and Row Skip	21
Black Level Calibration	22
Registers	23
Still Image Capture with External Synchronization	25
LINE_VALID Signal	25
Electrical Specifications	26
Data Output and Propagation Delays	26
Two-wire Serial Bus Timing	28
Quantum Efficiency	29
Image Center Offset and Orientation	30
Revision History	32
Rev C, 06/2005	32
Rev B, 05/2005	32
Rev A, Preliminary 11/2003	32



List of Tables

Table 1:	Key Performance Parameters.....	1
Table 2:	Available Part Numbers.....	1
Table 2:	Pin Descriptions.....	6
Table 3:	Frame Timing.....	9
Table 4:	Frame Time—Long Integration Time.....	9
Table 5:	Register List and Default Values.....	13
Table 6:	Register Description.....	14
Table 7:	Recommended Gain Settings at 48 MHz.....	20
Table 8:	Black Level Registers.....	23
Table 9:	DC Electrical Characteristics.....	26
Table 10:	AC Electrical Characteristics.....	27
Table 11:	Absolute Maximum Ratings.....	27
Table 12:	Optical Area Dimensions.....	30

List of Figures

Figure 1:	48-Pin CLCC Package Pinout Diagram	5
Figure 2:	Block Diagram	5
Figure 3:	Pixel Array Description	7
Figure 4:	Pixel Pattern Detail (Top Right Corner)	7
Figure 5:	Spatial Illustration of Image Readout	8
Figure 6:	Timing Example of Pixel Data	8
Figure 7:	Row Timing and FRAME_VALID/LINE_VALID Signals	8
Figure 8:	Timing Diagram Showing a Write to Reg0x09 with the Value 0x0284	12
Figure 9:	Timing Diagram Showing a Read from Reg0x09; Returned Value 0x0284	12
Figure 10:	Signal Path	20
Figure 11:	Readout of Six Columns in Normal and Column Mirror Output Mode	21
Figure 12:	Readout of Six Rows in Normal and Row Mirror Output Mode	21
Figure 13:	Readout of Eight Pixels in Normal and Column Skip Output Mode	22
Figure 14:	Black Level Calibration Flow Chart	22
Figure 15:	General Timing for Snapshot Mode	25
Figure 16:	Different LINE_VALID Formats	25
Figure 17:	Data Output Timing Diagram	26
Figure 18:	Serial Host Interface Start Condition Timing	28
Figure 19:	Serial Host Interface Stop Condition Timing	28
Figure 20:	Serial Host Interface Data Timing for Write	28
Figure 21:	Serial Host Interface Data Timing for Read	28
Figure 22:	Acknowledge Signal Timing After an 8-Bit Write to the Sensor	29
Figure 23:	Acknowledge Signal Timing After an 8-Bit Read from the Sensor	29
Figure 24:	Quantum Efficiency—Monochrome	29
Figure 25:	Image Center Offset	30
Figure 26:	Optical Orientation	30
Figure 27:	48-pin CLCC Package Outline Drawing	31

General Description

Figure 1: 48-Pin CLCC Package Pinout Diagram

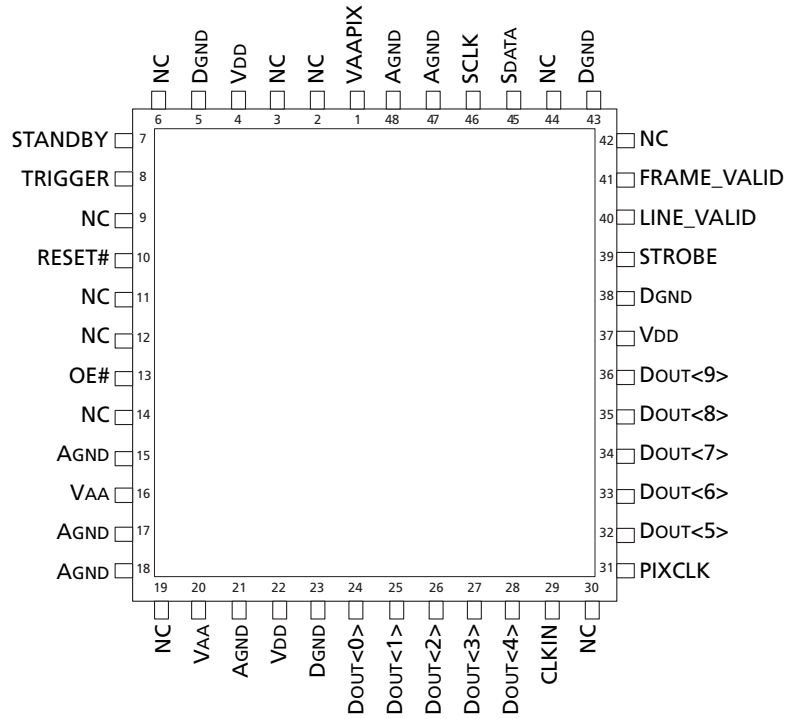


Figure 2: Block Diagram

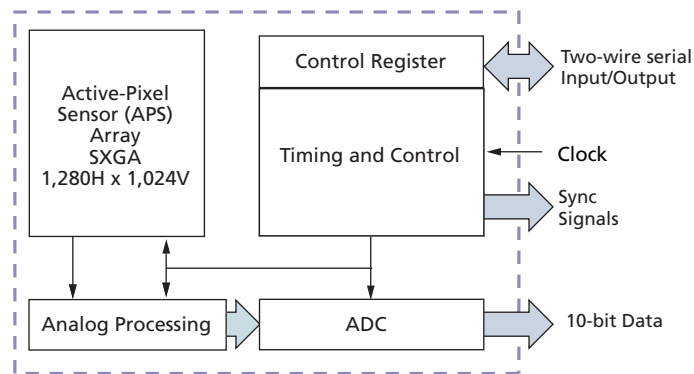


Table 2: Pin Descriptions

Pin Numbers	Symbol	Type	Description
29	CLKIN	Input	Clock in. Master clock into sensor (48 MHz maximum).
13	OE#	Input	Output enable. OE# when HIGH places outputs DOUT<0:9>, FRAME_VALID, LINE_VALID, PIXCLK, and STROBE into a tri-state configuration.
10	RESET#	Input	Reset. Activates (LOW) asynchronous reset of sensor. All registers assume factory defaults.
46	SCLK	Input	Serial clock. Clock for serial interface.
7	STANDBY	Input	Standby. Activates (HIGH) standby mode, disables analog bias circuitry for power saving mode.
8	TRIGGER	Input	Trigger. Activates (HIGH) snapshot sequence.
45	SDATA	Input/Output	Serial data. Serial data bus, requires 1.5K Ω resistor to 3.3V for pull-up.
24–28, 32–36	DOUT<0–9>	Output	Data out. Pixel data output bits 0:9, DOUT<9> (MSB), DOUT<0> (LSB).
41	FRAME_VALID	Output	Frame valid. Output is pulsed HIGH during frame of valid pixel data.
40	LINE_VALID	Output	Line valid. Output is pulsed HIGH during line of selectable valid pixel data (see Reg0x20 for options).
31	PIXCLK	Output	Pixel clock. Pixel data outputs are valid during falling edge of this clock. Frequency = (master clock).
39	STROBE	Output	Strobe. Output is pulsed HIGH to indicate sensor reset operation of pixel array has completed.
15,17,18,21, 47, 48	AGND	Supply	Analog ground. Provide isolated ground for analog block and pixel array.
5,23,38,43	DGND	Supply	Digital ground. Provide isolated ground for digital block.
16,20	VAA	Supply	Analog power. Provide power supply for analog block, 3.3V \pm 0.3V.
1	VAAPIX	Supply	Analog pixel power. Provide power supply for pixel array, 3.3V \pm 0.3V (3.3V).
4,22,37	VDD	Supply	Digital power. Provide power supply for digital block, 3.3V \pm 0.3V.
2,3,6,9,11,12, 14,19,30,42,44	NC	—	No connect. These pins must be left unconnected.

Pixel Data Format

Pixel Array Structure

The MT9M001 pixel array is configured as 1,312 columns by 1,048 rows (shown in Figure 3). The first 16 columns and the first eight rows of pixels are optically black, and can be used to monitor the black level. The last seven columns and the last seven rows of pixels are also optically black. The black row data is used internally for the automatic black level adjustment. However, the black rows can also be read out by setting the sensor to raw data output mode (Reg0x20, bit 11 = 1). There are 1,289 columns by 1,033 rows of optically active pixels, which provides a four-pixel boundary around the SXGA (1,280 x 1,024) image.

Figure 3: Pixel Array Description

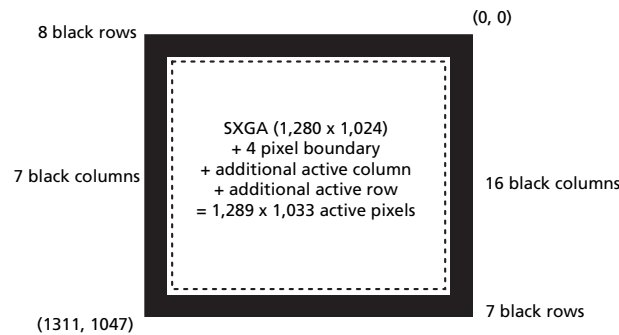
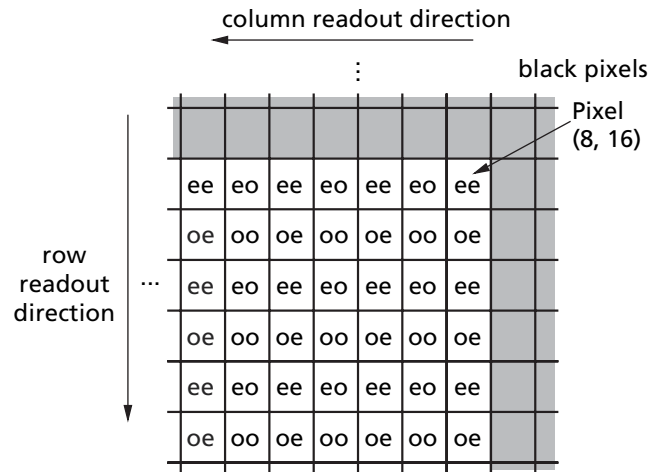


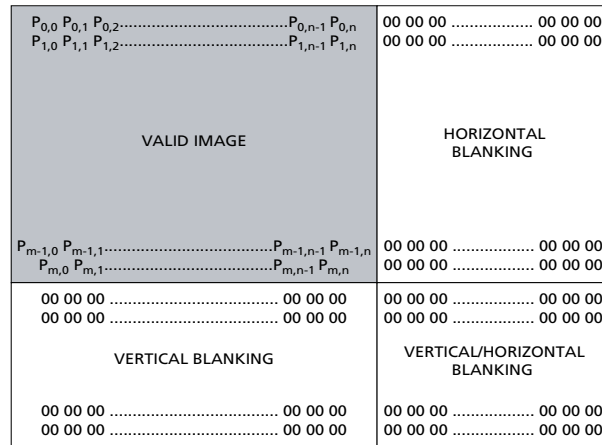
Figure 4: Pixel Pattern Detail (Top Right Corner)



Output Data Format

The MT9M001 image data is read out in a progressive scan. Valid image data is surrounded by horizontal blanking and vertical blanking, as shown in Figure 5. The amount of horizontal blanking and vertical blanking is programmable through Reg0x05 and Reg0x06, respectively. LINE_VALID is HIGH during the shaded region of the figure. FRAME_VALID timing is described in “Output Data Timing” on page 8.

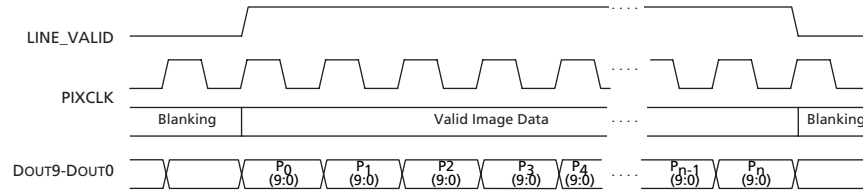
Figure 5: Spatial Illustration of Image Readout



Output Data Timing

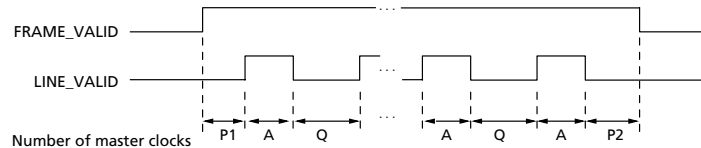
The data output of the MT9M001 is synchronized with the PIXCLK output. When LINE_VALID is HIGH, one 10-bit pixel datum is output every PIXCLK period.

Figure 6: Timing Example of Pixel Data



The rising edges of the PIXCLK signal are nominally timed to occur on the rising DOUT edges. This allows PIXCLK to be used as a clock to latch the data. DOUT data is valid on the falling edge of PIXCLK. The PIXCLK is HIGH while master clock is HIGH and then LOW while master clock is LOW. It is continuously enabled, even during the blanking period. The parameters P1, A P2, and Q in Figure 7 are defined in Table 3.

Figure 7: Row Timing and FRAME_VALID/LINE_VALID Signals



**Frame Timing Formulas
Table 3: Frame Timing**

Parameter	Name	Equation (MASTER CLOCK)	Default Timing	Notes
A	Active Data Time	$(\text{Reg0x04} + 1)$	1,280 pixel clocks = 26.7 μ s	1
P ₁	Frame Start Blanking	(242)	242 pixel clocks = 5.04 μ s	
P ₂	Frame End Blanking	$(2 + \text{Reg0x05} - 19)$ (MIN Reg0x05 value = 19)	2 pixel clocks = 0.042 μ s	2
Q = P ₁ + P ₂	Horizontal Blanking	$(244 + \text{Reg0x05} - 19)$ (MIN Reg0x05 value = 19)	244 pixel clocks = 5.08 μ s	2
A + Q	Row Time	$((\text{Reg0x04} + 1) + (244 + \text{Reg0x05} - 19))$	1,524 pixel clocks = 31.75 μ s	
V	Vertical Blanking	$(\text{Reg0x06} + 1) \times (A + Q)$ (MIN Reg0x06 value = 15)	39,624 pixel clocks = 825.5 μ s	
N _{ROWS} x (A + Q)	Frame Valid Time	$(\text{Reg0x03} + 1) \times (A + Q)$	1,560,576 pixel clocks = 32.51ms	
F	Total Frame Time	$(\text{Reg0x03} + 1 + \text{Reg0x06} + 1) \times (A + Q)$	1,600,200 pixel clocks = 33.34ms	

Notes: 1. Row skip mode should have no effect on the integration time. Column skip mode changes the effective value of Column Size (Reg0x04) as follows:

Column Skip 2 => R4eff = $(\text{int}(R4 / 4) \times 2) + 1$

Column Skip 4 => R4eff = $(\text{int}(R4 / 8) \times 2) + 1$

Column Skip 8 => R4eff = $(\text{int}(R4 / 16) \times 2) + 1$

where the int() function truncates to the next lowest integer. Now use R4eff in the equation for row time instead of R4

2. Default for Reg0x05 = 9. However, sensor ignores any value for Reg0x05 less than 19.

Sensor timing is shown above in terms of pixel clock and master clock cycles (please refer to Figure 6). The recommended master clock frequency is 48 MHz. The vertical blank and total frame time equations assume that the number of integration rows (bits 13 through 0 of Reg0x09) is less than the number of active plus blanking rows ($\text{Reg0x03} + 1 + \text{Reg0x06} + 1$). If this is not the case, the number of integration rows must be used instead to determine the frame time, as shown in Table 4.

Table 4: Frame Time—Long Integration Time

Parameter	Name	Equation (master clock)	Default Timing
V'	Vertical Blanking (long integration time)	$(\text{Reg0x09} - \text{Reg0x03}) \times (A + Q)$	39,624 pixel clocks = 82.5 μ s
F'	Total Frame Time (long integration time)	$(\text{Reg0x09} + 1) \times (A + Q)$	1,600,200 pixel clocks = 33.34ms

Serial Bus Description

Registers are written to and read from the MT9M001 through the two-wire serial interface bus. The sensor is a two-wire serial interface slave and is controlled by the serial clock (SCLK), which is driven by the serial interface master. Data is transferred into and out of the MT9M001 through the serial data (SDATA) line. The SDATA line is pulled up to 3.3V off-chip by a 1.5K Ω resistor. Either the slave or master device can pull the SDATA line down—the serial interface protocol determines which device is allowed to pull the SDATA line down at any given time.

Protocol

The two-wire serial interface defines several different transmission codes, as follows:

- a start bit
- the slave device eight-bit address
- a(an) (no) acknowledge bit
- an 8-bit message
- a stop bit

Sequence

A typical read or write sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's eight-bit address. The last bit of the address determines if the request will be a read or a write, where a "0" indicates a write and a "1" indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data eight bits at a time, with the slave sending an acknowledge bit after each eight bits. The MT9M001 uses 16-bit data for its internal registers, thus requiring two 8-bit transfers to write to one register. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address, just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data eight bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Bus Idle State

The bus is idle when both the data and clock lines are HIGH. Control of the bus is initiated with a start bit, and the bus is released with a stop bit. Only the master can generate the start and stop bits.

Start Bit

The start bit is defined as a HIGH-to-LOW transition of the data line while the clock line is HIGH.

Stop Bit

The stop bit is defined as a LOW-to-HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a two-wire serial interface device consists of seven bits of address and 1 bit of direction. A “0” (0xBA) in the LSB (least significant bit) of the address indicates the write mode, and a “1” (0xBB) indicates read mode.

Data Bit Transfer

One data bit is transferred during each clock pulse. The serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the two-wire serial interface clock—it can only change when the serial clock is LOW. Data is transferred eight bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The master generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and the receiver indicates an acknowledge bit by pulling the data line LOW during the acknowledge clock pulse.

No-Acknowledge Bit

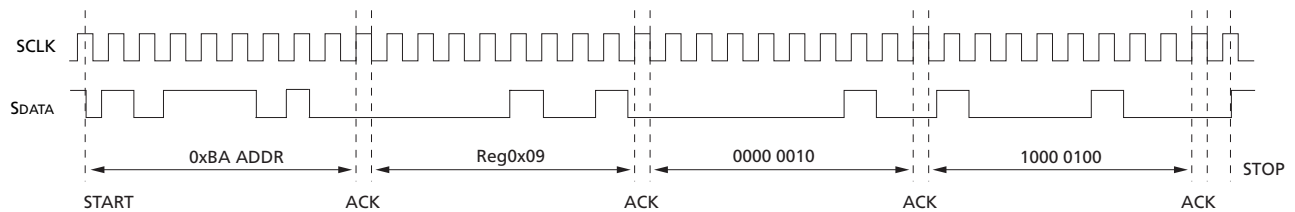
The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Two-Wire Serial Interface Sample Write and Read Sequences

16-Bit Write Sequence

A typical write sequence for writing 16 bits to a register is shown in Figure 8. A start bit given by the master, followed by the write address, starts the sequence. The image sensor will then give an acknowledge bit and expects the register address to come first, followed by the 16-bit data. After each eight-bit transfer, the image sensor will give an acknowledge bit. All 16 bits must be written before the register will be updated. After 16 bits are transferred, the register address is automatically incremented so that the next 16 bits are written to the next register. The master stops writing by sending a start or stop bit.

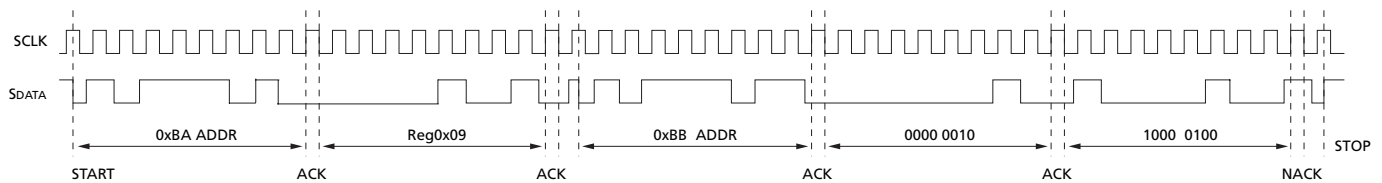
Figure 8: Timing Diagram Showing a Write to Reg0x09 with the Value 0x0284



16-Bit Read Sequence

A typical read sequence is shown in Figure 9. First the master has to write the register address, as in a write sequence. Then a start bit and the read address specifies that a read is about to happen from the register. The master then clocks out the register data eight bits at a time. The master sends an acknowledge bit after each eight-bit transfer. The register address should be incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Figure 9: Timing Diagram Showing a Read from Reg0x09; Returned Value 0x0284



Registers

Register Map

Table 5: Register List and Default Values

Register # (Hex)	Description	Data Format (Binary)	Default Value (Hex)
0x00	Chip Version	1000 0100 0001 0001	0x8431
0x01	Row Start	0000 0ddd dddd dddd	0x000C
0x02	Column Start	0000 0ddd dddd dddd	0x0014
0x03	Row Size (Window Height)	0000 0ddd dddd dddd	0x03FF
0x04	Col Size (Window Width)	0000 0ddd dddd dddd	0x04FF
0x05	Horizontal Blanking	0000 0ddd dddd dddd	0x0009
0x06	Vertical Blanking	0000 0ddd dddd dddd	0x0019
0x07	Output Control	0000 0000 0d00 00dd	0x0002
0x09	Shutter Width	00dd dddd dddd dddd	0x0419
0x0B	Restart	0000 0000 0000 000d	0x0000
0x0C	Shutter Delay	0000 0ddd dddd dddd	0x0000
0x0D	Reset	0000 0000 0000 000d	0x0000
0x1E	Read Options 1	1000 dddd 00dd dd00	0x8000
0x20	Read Options 2	dd01 0dd1 d00d d10d	0x1104
0x2B	Even Row, Even Column	0000 0000 0ddd dddd	0x0008
0x2C	Odd Row, Even Column	0000 0000 0ddd dddd	0x0008
0x2D	Even Row, Odd Column	0000 0000 0ddd dddd	0x0008
0x2E	Odd Row, Odd Column	0000 0000 0ddd dddd	0x0008
0x35	Global Gain	0000 0000 0ddd dddd	0x0008
0x5F	Cal Threshold	dddd dddd d0dd dddd	0x0904
0x60	Even Row, Even Column	0000 000d dddd dddd	0x0000
0x61	Odd Row, Odd Column	0000 000d dddd dddd	0x0000
0x62	Cal Ctrl	d00d d100 1001 1ddd	0x0498
0x63	Even Row, Odd Column	0000 000d dddd dddd	0x0000
0x64	Odd Row, Even Column	0000 000d dddd dddd	0x0000
0xF1	Chip Enable	0000 0000 0000 00dd	0x0001

Note: 1 = always 1
0 = always 0
d = programmable

Table 6: Register Description

Register	Bit	Description
Chip ID		
0x00	15:0	This register is read-only and gives the chip identification number: 0x8431.
Window Control		
These registers control the size of the window.		
0x01	10:0	First row to be read out—default = 0x000C (12).
0x02	10:0	First column to be read out—default = 0x0014 (20). Register value must be an even number.
0x03	10:0	Window height (number of rows - 1)—default = 0x03FF (1023). Minimum value for 0x03 = 0x0002.
0x04	10:0	Window width (number of columns - 1)—default = 0x04FF (1279). Register value must be an odd number. Minimum value for 0x04 = 0x0003.
Blanking Control		
These registers control the blanking time in a row (called column fill-in or horizontal blanking) and between frames (vertical blanking). Horizontal blanking is specified in terms of pixel clocks. Vertical blanking is specified in terms of row readout times. The actual imager timing can be calculated using Table 3, Frame Timing, on page 9.		
0x05	10:0	Horizontal Blanking—default = 0x0009 (9 pixels).
0x06	10:0	Vertical Blanking—default = 0x0019 (25 rows).
Output Control		
This register controls various features of the output format for the sensor.		
0x07	0	Synchronize changes (copied to Reg0xF1, bit1). 0 = normal operation. Update changes to registers that affect image brightness (integration time, integration delay, gain, horizontal blanking and vertical blanking, window size, row/column skip or row mirror) at the next frame boundary. The “frame boundary” is 8 row_times before the rising edge of FRAME_VALID. (If “Show Dark Rows” is set, it will be coincident with the rising edge of FRAME_VALID.) 1 = do not update any changes to these settings until this bit is returned to “0.”
	1	Chip Enable (copied to Reg0xF1, bit0). 1 = normal operation. 0 = stop sensor readout. When this is returned to “1,” sensor readout restarts at the starting row in a new frame. The digital power consumption can then also be reduced to less than 5uA by turning off the master clock.
	2	Reserved—default is 0; set to zero at all times.
	3	Reserved—default is 0; set to zero at all times.
	6	Use Test Data. When set, a test pattern will be output instead of the sampled image from the sensor array. The value sent to the DOUT[9:0] pins will alternate between the Test Data register (Reg0x32) in even columns and the inverse of the Test Data register for odd columns. The output “image” will have the same width, height, and frame rate as it would otherwise have. No digital processing (gain or offset) is applied to the data. When clear (the default), sampled pixel values are output normally.

Table 6: Register Description (continued)

Register	Bit	Description
Pixel Integration Control		
<p>These registers (along with the window sizing and blanking registers) control the integration time for the pixels. The actual total integration time (t_{INT}) is:</p> $t_{INT} = \text{Reg0x09} \times \text{row time} - \text{overhead time} - \text{reset delay, where:}$ $\text{Row time} = ((\text{Reg0x04} + 1) + 244 + \text{Reg0x05} - 19) \text{ pixel clock periods}$ $\text{Overhead time} = 180 \text{ pixel clock periods}$ <p>Reset delay = 4 x Reg0x0C pixel clock periods If the value in Reg0x0C exceeds (row time - 548)/4 pixel clock cycles, the row time will be extended by (4 x Reg0x0C - (row time - 548)) pixel clock cycles.</p> <p>In this expression, the row time term, Reg0x09 x ((number of columns) + 244 + horizontal blanking register - 19), corresponds to the number of rows integrated. The overhead time (180 pixel clocks) is the overhead time between the READ cycle and the RESET cycle, and the final term is the effect of the reset delay. Typically, the value of Reg0x09 is limited to the number of rows per frame (which includes vertical blanking rows) such that the frame rate is not affected by the integration time. If Reg0x09 is increased beyond the total number of rows per frame, the MT9M001 will add additional blanking rows as needed. A second constraint is that t_{INT} must be adjusted to avoid banding in the image from light flicker. Under 60Hz flicker, this means t_{INT} must be a multiple of 1/120 of a second. Under 50Hz flicker, t_{INT} must be a multiple of 1/100 of a second.</p>		
0x09	13:0	Number of rows of integration—default = 0x0419 (1049).
0x0C	10:0	Shutter delay—default = 0x0000 (0). This is the number of master clocks times four that the timing and control logic waits before asserting the reset for a given row.
Frame Restart		
0x0B	0	Setting bit 0 to "1" of Reg0x0B will cause the sensor to abandon the readout of the current frame and restart from the first row. This register automatically resets itself to 0x0000 after the frame restart. The first frame after this event is considered to be a "bad frame" (see description for Reg0x20, bit0).
Reset		
0x0D	0	This register is used to reset the sensor to its default, power-up state. To put the MT9M001 in reset mode first write a "1" into bit 0 of this register, then write a "0" into bit 0 to resume operation.

Table 6: Register Description (continued)

Register	Bit	Description
Read Mode 1		
In read mode 1, this register is used to control many aspects of the readout of the sensor.		
0x1E	0	Reserved—default is 0; set to zero at all times.
	1	Reserved—default is 0; set to zero at all times.
	2	Column Skip 4—default is 0 (disable). 1 = enable.
	3	Row Skip 4—default is 0 (disable). 1 = enable.
	4	Column Skip 8—default is 0 (disable). 1 = enable.
	5	Row Skip 8—default is 0 (disable). 1 = enable.
	6	Reserved—default is 0; do not change.
	7	Reserved—default is 0; do not change.
	8	Snapshot Mode—default is 0 (continuous mode). 1 = enable (wait for TRIGGER; TRIGGER can come from outside signal (TRIGGER pin on the sensor) or from serial interface register restart, i.e. programming a “1” to bit 0 of Reg0x0B.
	9	STROBE Enable—default is 0 (no STROBE signal). 1 = enable STROBE (signal output from the sensor during the time all rows are integrating. See STROBE width for more information).
	10	STROBE Width—default is 0 (STROBE signal width at minimum length, 1 row of integration time, prior to line valid going HIGH). 1 = extend STROBE width (STROBE signal width extends to entire time all rows are integrating).
	11	Strobe Override—default is 0 (STROBE signal created by digital logic). 1 = override STROBE signal (STROBE signal is set HIGH when this bit is set, LOW when this bit is set LOW. It is assumed that STROBE enable is set to “0” if STROBE override is being used).
	12	Reserved—default is 0; do not change.
	13	Reserved—default is 0; do not change.
14	Reserved—default is 0; do not change.	
15	Reserved—default is 1; do not change.	
Gain Settings		
The gain is individually controllable for each of the four groups of pixels that lie in odd rows and columns, even rows and columns, odd rows and even columns, and even rows and odd columns. This is shown in the register chart.		
Formula for gain setting:		
Gain ≤ 8		
Gain = (bit[6] + 1) x (bit[5-0] x 0.125)		
Gain > 8 (bit[6] = 1 and bit[5] = 1)		
Gain = 8.0 + bit[2-0]		
Since bit[6] of the gain registers are multiplicative factors for the gain settings, there are alternative ways of achieving certain gains. Some settings offer superior noise performance to others, despite the same overall gain. The following lists the recommended gain settings:		
<u>Gain</u>	<u>Increments</u>	<u>Recommended Settings</u>
1.000 to 4.000	0.125	0x08 to 0x20
4.25 to 8.00	0.25	0x51 to 0x60
9.0 to 15.0	1.0	0x61 to 0x67
0x2B	6:0	Even row, even column—default = 0x08 (8) = 1x gain.
0x2C	6:0	Odd row, even column—default = 0x08 (8) = 1x gain.

Table 6: Register Description (continued)

Register	Bit	Description
0x2D	6:0	Even row, odd column—default = 0x08 (8) = 1x gain.
0x2E	6:0	Odd row, odd column—default = 0x08 (8) = 1x gain.
0x35	6:0	Global gain—default = 0x08 (8) = 1x gain. This register can be used to set all four gains at once.
Test Data		
0x32	11:2	Test Data. The value used to produce a test pattern in "Use Test Data" mode (Reg0x07 bit 6).
Read Mode 2		
This register is used to control many aspects of the readout of the sensor.		
0x20	0	No bad frames—1 = output all frames (including bad frames). 0 (default) = only output good frames. A bad frame is defined as the first frame following a change to: window size or position, horizontal blanking, row or column skip, or mirroring.
	1	Reserved—default is 0; do not change.
	2	Reserved—default is 1; set to "1" at all times.
	3	Column skip—1= read out two columns, and then skip two columns (for example, col 0, col 1, col 4, col 5...). 0 = normal readout (default).
	4	Row skip—1 = read out two rows, and then skip two rows (for example, row 0, row 1, row 4, row 5...). 0 = normal readout (default).
	5	Reserved—default is 0; do not change.
	6	Reserved—default is 0; set to zero at all times.
	7	Flip Row—1 = readout starting 1 row later (alternate color pair). 0 (default) = normal readout.
	8	Reserved—default is 1; set to "1" at all times.
	9	1 = "Continuous" LINE_VALID (continue producing LINE_VALID during vertical blanking). 0 = normal LINE_VALID (default, no LINE_VALID during vertical blanking).
	10	1 = LINE_VALID = "Continuous" LINE_VALID XOR FRAME_VALID. 0 = LINE_VALID determined by bit 9.
	11	Reserved—default is 0; do not change.
	12	Reserved—default is 1; do not change.
	13	Reserved—default is 0; do not change.
	14	Reserved—default is 0; do not change.
15	Mirror Row—1 = read out from bottom to top (upside down). 0 (default) = normal readout (top to bottom).	
Test Data		
0x32	11:2	Test Data. The value used to produce a test pattern in "Use Test Data" mode (Reg0x07 bit 6).
Black Level Calibration		
These registers are used in the black level calibration. Their functionality is described in detail in the next section.		

Table 6: Register Description (continued)

Register	Bit	Description
0x5F	5:0	Thres_lo—Lower threshold for black level in ADC LSBs—default = 000100.
	7	1 = override automatic Thres_hi and Thres_lo adjust (Thres_hi always = bits 14:8; Thres_lo always = bits 5:0). Default = 0 = Automatic Thres_hi and Thres_lo adjustment.
	14:8	Thres_hi—Maximum allowed black level in ADC LSBs (default = Thres_lo + 5). Black level maximum is set to this value when bit 7 = 1; black level maximum is reset to this value after every black level average restart if bit 15 = 1 and bit 7 = 0.
	15	No gain dependence. 1 = Thres_lo is set by the programmed value of bits 5:0, Thres_hi is reset to the programmed value (bits 14:8) after every black level average restart. 0 = Thres_lo and Thres_hi are set automatically, as described above.
0x60	8:0	Even row, even column—analog offset correction value for even row, even column, bits 0:7 sets magnitude, bit 8 set sign. 0 = positive; 1 = negative. two's complement, if bit 8 = 1, Offset = bits [0:7] - 256.
0x61	8:0	Odd row, odd column—analog offset correction value for odd row, odd column, bits 0:7 sets magnitude, bit 8 set sign. 0 = positive; 1 = negative. two's complement, if bit 8 = 1, Offset = bits [0:7] - 256.
0x62	0	Manual override of black level correction. 1 = override automatic black level correction with programmed values. 0 = normal operation (default).
	2:1	Force/disable black level calibration. 00 = apply black level calibration during ADC operation only (default). 10 = apply black level calibration continuously. X1 = disable black level correction (Offset Correction Voltage = 0.0V). (In this case, no black level correction is possible).
	4:3	Reserved—default is 1; do not change.
	6:5	Reserved—default is 0; do not change.
	7	Reserved—default is 1; do not change.
	9:8	Reserved—default is 0; do not change.
	10	Reserved—default is 1; do not change.
	11	1 = do not reset the upper threshold after a black level recalculation sweep. 0 = reset the upper threshold after a black level recalculation sweep (default).
	12	1 = start a new running digitally filtered average for the black level (this is internally reset to "0" immediately), and do a rapid sweep to find the new starting point. 0 = normal operation (default).
	14:3	Reserved—default is 0; set to zero at all times.
0x63	15	1 = do not perform the rapid black level sweep on new gain settings. 0 = normal operation.
	8:0	Even row, odd column—analog offset correction value for even row, odd column, bits 0:7 sets magnitude, bit 8 set sign. 0 = positive; 1 = negative. two's complement, if bit 8 = 1, Offset = bits [0:7] - 256.
0x64	8:0	Odd row, even column—analog offset correction value for odd row, even column, bits 0:7 sets magnitude, bit 8 set sign. 0 = positive; 1 = negative. two's complement, if bit 8 = 1, Offset = bits [0:7] - 256.

Table 6: Register Description (continued)

Register	Bit	Description
Chip Enable and Two-Wire Serial Interface Write Synchronize.		
0xF1	0	Mirrors the functionality of Reg0x07 bit1 (Chip Enable). 1 = normal operation. 0 = stop sensor readout; when this is returned to "1," sensor readout restarts at the starting row in a new frame.

Feature Description

Signal Path

The MT9M001 signal path consists of two stages, a programmable gain stage and a programmable analog offset stage.

Programmable Gain Stage

A total programmable gain of 15 is available and can be calculated using the following formula:

$$\text{Gain 1 to 8: Gain} = (\text{bit}[6] + 1) \times (\text{bit}[5:0] \times 0.125)$$

For gain higher than eight, the user would need to set bit[6:5] = 11 and use the lower 3 LSB's bit[2:0] to set the higher gain values. The formula for obtaining gain greater than eight is as follows:

$$\text{Total gain} = 8 + \text{bit}[2:0]$$

For example, for total gain = 12, the value to program is bit[6-0] = 1100100.

The maximum total gain = 15, i.e. bit[6:0] = 1100111.

The gain circuitry in the MT9M001 is designed to offer signal gains from one to 15. The minimum gain of one corresponds to the lowest setting where the pixel signal is guaranteed to saturate the ADC under all specified operating conditions. Any reduction of the gain below this value may cause the sensor to saturate at ADC output values less than the maximum, under certain conditions. It is recommended that this guideline be followed at all times.

Since bit[6] of the gain registers are multiplicative factors for the gain settings, there are alternative ways of achieving certain gains. Some settings offer superior noise performance to others, despite the same overall gain. Recommended gain settings are listed in Table 7.

Figure 10: Signal Path

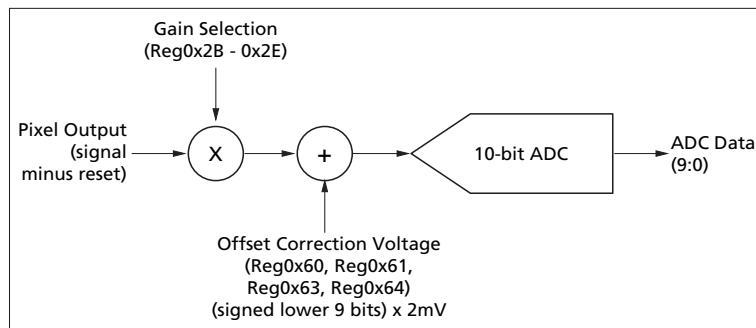


Table 7: Recommended Gain Settings at 48 MHz

Nominal Gain	Increments	Recommended Settings
1 to 4.000	0.125	0x08 to 0x20
4.25 to 8.00	0.25	0x51 to 0x60
9 to 15	1.0	0x61 to 0x67

Programmable Analog Offset Stage

The programmable analog offset stage corrects for analog offset that might be present in the analog signal. The user would need to program register 0x62 appropriately to enable the analog offset correction.

The lower eight bits (bit[7:0]) determines the absolute value of the analog offset to be corrected and bit[8] determines the sign of the correction. When bit[8] is “1”, the sign of the correction is negative and vice versa. The analog value of the correction relative to the analog gain stage can be determined from the following formula:

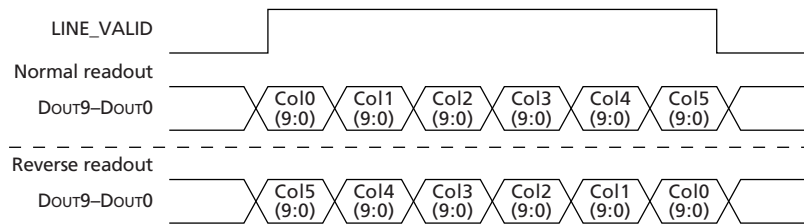
$$\text{Analog offset (bit[8] = 0)} = \text{bit[7:0]} \times 2\text{mV}$$

$$\text{Analog offset (bit[8] = 1)} = -(\text{bit[7:0]} \times 2\text{mV})$$

Column and Row Mirror Image

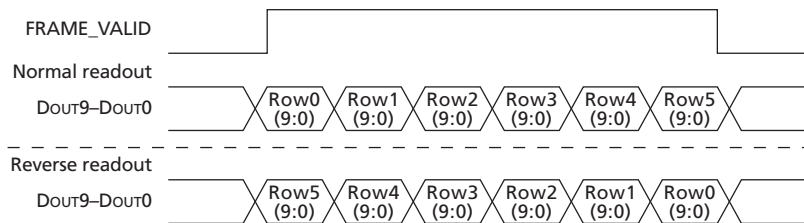
By setting bit 14 of Reg0x20, the readout order of the columns will be reversed, as shown in Figure 11.

Figure 11: Readout of Six Columns in Normal and Column Mirror Output Mode



By setting bits 15 of Reg0x20 the readout order of the rows will be reversed, as shown in Figure 12.

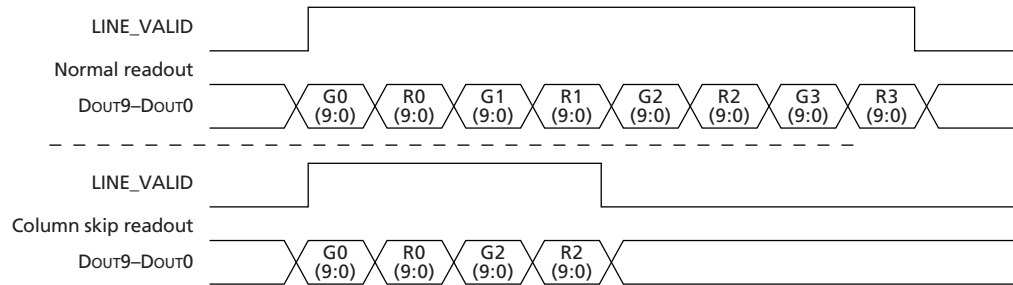
Figure 12: Readout of Six Rows in Normal and Row Mirror Output Mode



Column and Row Skip

By setting bit 3 of Reg0x20, only half of the columns set will be read out. An example is shown in Figure 13. Only columns with bit 1 equal to “0” will be read out (xxxxxxx0x). The row skip works in the same way and will only read out rows with bit 1 equal to “0.” Row skip mode is enabled by setting bit 4 of Reg0x20. For both row and column skips, the number of rows or columns read out will be half of what is set in Reg0x03 or Reg0x04, respectively.

Figure 13: Readout of Eight Pixels in Normal and Column Skip Output Mode



Black Level Calibration

The MT9M001 has automatic black level calibration on-chip which can be overridden by the user, as described below and shown in Figure 14.

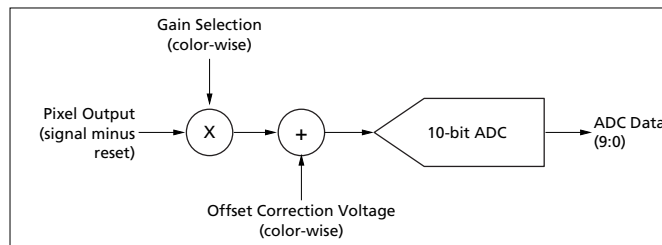
The automatic black level calibration measures the average value of 256 pixels from two dark rows of the chip for each of the four colors. The pixels are averaged as if they were light-sensitive and passed through the appropriate color gain. This average is then digitally filtered over many frames.

For each color, the new filtered average is compared to a minimum acceptable level (to screen for too low a black level) and a maximum acceptable level. If the average is lower than the minimum acceptable level, the offset correction voltage for that color is increased by one offset LSB (offset LSBs do not match ADC LSBs; typically, one offset LSB is approximately 2mV). If it is above the maximum level, the level is decreased by 1 LSB (2mV). The upper threshold is automatically adjusted whenever an upward shift in the black level from below the minimum results in a new black level above the maximum. This prevents black level oscillation from below the minimum to above the maximum. The lower threshold is increased with the maximum gain setting according to the formula described under Reg0x5F. This prevents clipping of the black level.

Whenever the gain or any of the readout timing registers is changed (shutter width, vertical blanking, number of rows or columns, or the shutter delay) or if the black level recalculation bit, reset bit or restart bit is set, the running digitally filtered average is reset to the first average of the dark pixels. The digital filtering over many frames is then restarted. Whenever the gain or the readout timing registers are changed, the upper threshold is restored to its default value.

After changes to the sensor configuration, large shifts in the black level calibration can result. To quickly adapt to this shift, a rapid sweep of the black level during the dark-row readout is performed on the first frame after certain changes to the sensor registers. Any changes to the registers listed above will cause this recalculation. The data from this sweep allows the sensor to choose an accurate new starting point for the running average. This procedure can be disabled as described under Reg0x5F.

Figure 14: Black Level Calibration Flow Chart



Registers

Table 8: Black Level Registers

Register	bit	Description
Reg0x5F		
This register controls the operation of the black level calibration thresholds.		
	15	No gain dependence. 1 = Thres_lo is set by the programmed value of bits 5:0, Thres_hi is reset to the programmed value (bits 14:8) after every black level average restart. 0 = Thres_lo and Thres_hi are set automatically as described below.
	14:8	Thres_hi—maximum allowed black level in ADC LSBs (default = Thres_lo + 5). Black level maximum is set to this value when bit 7 = 1, black level maximum is reset to this value after every black level average restart if bit 15 = 1 and bit 7 = 0.
	7	1 = override automatic Thres_hi and Thres_lo adjust (Thres_hi always = bits 14:8, Thres_lo always = bits 5:0). 0 = automatic Thres_hi and Thres_lo adjustment.
	5:0	Thres_lo—Lower threshold for black level in ADC LSBs. Under default automatic operation (bit 7 = 0, bit 15 = 0), $\text{Thres_lo} = \text{RegGain}_{\text{max}}/4 \times (\text{RegGain}_{\text{max}}, \text{bit } 6 + 1) \times (\text{RegGain}_{\text{max}}, \text{bit } 7 + 1)$, where $\text{RegGain}_{\text{max}}$ is the maximum of the four independent gain register settings. Whenever a jump in the calibration causes the black level data to change from below Thres_lo to above Thres_hi, Thres_hi is adjusted according to the following: If new black level < 64: $\text{Thres_hi} = \text{Thres_lo} + 2 + (2 \times \text{Delta})$, where $\text{Delta} = \text{new black level} - \text{Thres_lo}$ If new black level > 63 and < 119: $\text{Thres_hi} = \text{new black level} + 4$ If new black level > 119: $\text{Thres_hi} = 123$ After any recalculation of the black level and average restart, Thres_hi is reset to either Thres_lo + 5 (automatic, default mode), Thres_hi (bit 7 = 1). Reg0x62, bit 11 will override this.
Reg0x62		
This register is used to control the automatic black level calibration circuitry.		
	15	1 = do not perform the rapid black level sweep on new gain settings. 0 = normal operation.
	14	Reserved—default is 0; do not change.
	13	Reserved—default is 0; do not change.
	12	1 = start a new running digitally filtered average for the black level (this is internally reset to "0" immediately), and do a rapid sweep to find the new starting point.
	11	1 = do not reset the upper threshold after a black level recalculation sweep. 0 = reset the upper threshold after a black level recalculation sweep (default).
	10:3	Reserved—default is 1; do not change.
	2:1	Force/disable black level calibration. 00 = apply black level calibration during ADC operation only (default). 10 = apply black level calibration continuously. X1 = disable black level correction (Offset Correction Voltage = Skew Voltage = 0.0V). (In this case, no black level correction is possible).
	0	Manual override of black level correction. 1 = override automatic black level correction with programmed values. 0 = normal operation (default).

Registers

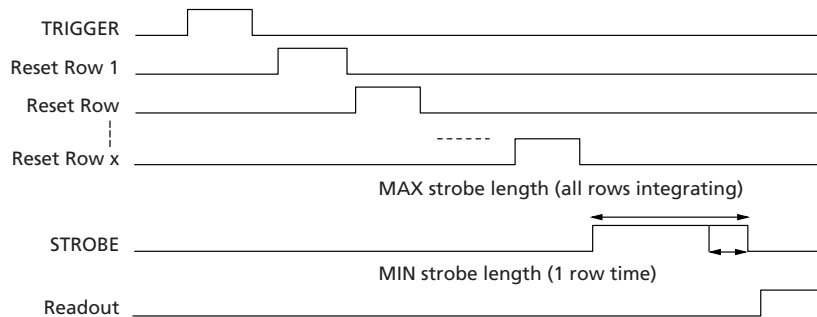
Table 8: Black Level Registers (continued)

Register	bit	Description
Reg0x60, Reg0x61, Reg0x63, Reg0x64		<p>These registers contain the 9-bit signed black level calibration values. In normal operation, these values are calculated at the beginning of each frame. However, if Reg0x62, bit 0 is set to "1," these registers can be written to, overriding the automatic black level calculation. This feature can be used in conjunction with readout of the black rows (Reg0x20, bit 11) if the user would like to use an external black level calibration circuit. The offset correction voltage is generated according to the following formula:</p> $\text{Offset Correction Voltage} = (9\text{-bit signed calibration value, } -256 \text{ to } 255) \times (2\text{mV} \times \text{Enable bit two's complement, if bit } 8 = 1, \text{ Offset} = \text{bits } [0:7] - 256$ $\text{ADC input voltage} = \text{Pixel Output Voltage} \times \text{Analog Gain} - \text{Offset Correction Voltage}$

Still Image Capture with External Synchronization

In continuous mode video image capture, the TRIGGER signal should be held LOW or “0.” To capture a still image, the sensor must first be put into snapshot mode by programming a “1” in register 0x1E, bit 8. In snapshot mode, the sensor waits for a TRIGGER signal (FRAME_VALID, LINE_VALID signals are LOW, pixel clock signal continues). When the TRIGGER signal is received (active HIGH), one frame is read out (a TRIGGER signal can also be achieved by programming a restart—for example, program a “1” to bit 0 of Reg0x0B). The reset, readout timing for that frame will be the same as for a continuous frame with similar register settings; the only difference is that only one frame is read out. General timing for the snapshot mode is shown in Figure 15.

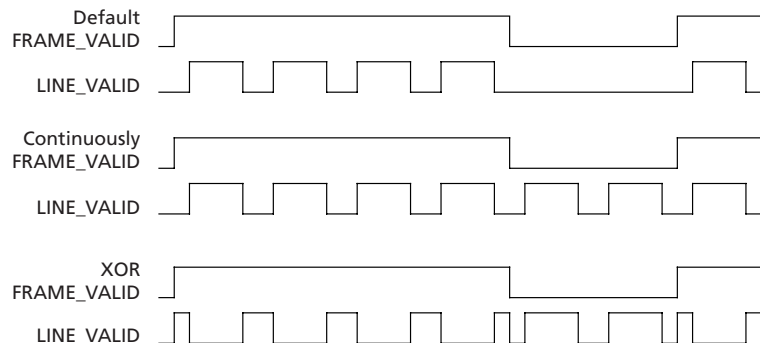
Figure 15: General Timing for Snapshot Mode



LINE_VALID Signal

By setting bit 9 and 10 of Reg0x20 the line valid signal can get three different output formats. The formats are shown when reading out four rows and two vertical blanking rows (Figure 16). In the last format, the LINE_VALID signal is the XOR between the continuously LINE_VALID signal and the FRAME_VALID signal.

Figure 16: Different LINE_VALID Formats



Electrical Specifications

Data Output and Propagation Delays

By default, the MT9M001 launches pixel data, FRAME_VALID and LINE_VALID with the rising edge of PIXCLK. The expectation is that the user captures DOUT[7:0], FRAME_VALID and LINE_VALID using the rising edge of PIXCLK.

Figure 17: Data Output Timing Diagram

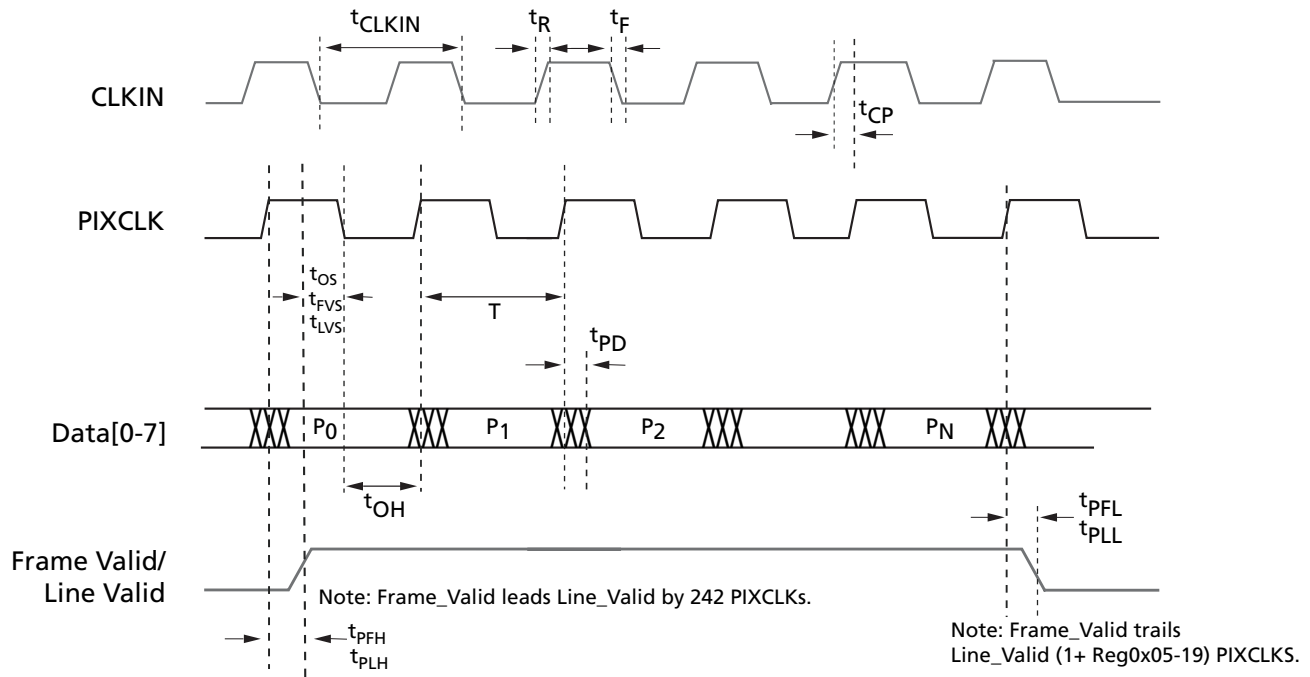


Table 9: DC Electrical Characteristics

(DC Setup Conditions: $f_{CLKIN} = 48 \text{ MHz}$, $V_{DD} = 3.3\text{V}$, $V_{AA} = 3.3\text{V}$, $V_{AAPIX} = 3.3\text{V}$, $T_A = 25^\circ\text{C}$)

Symbol	Definition	Condition	Min	Typ	Max	Units
VDD	Core digital voltage		3	3.3	3.6	V
VAA	Analog voltage		3	3.3	3.6	V
VAAPIX	Pixel supply voltage		3	3.3	3.6	V
VIH	Input high voltage		$V_{PWR} - 0.3$		$V_{PWR} + 0.3$	V
VIL	Input low voltage		-0.3		0.8	V
IIN	Input leakage current	No Pull-up Resistor; $V_{IN} = V_{DD}$ or DGND	-15		15	μA
VOH	Output high voltage		$V_{PWR} - 0.2$		—	V
VOL	Output low voltage				0.2	V
IOZ	Tri-state output leakage current		—		15	μA
IDD	Digital operating current		—	20	24	mA
IAA	Analog operating current		—	85	110	mA
IAAPIX	Pixel supply current		—	5	10	mA

Table 9: DC Electrical Characteristics (continued)

 (DC Setup Conditions: $f_{CLKIN} = 48 \text{ MHz}$, $V_{DD} = 3.3\text{V}$, $V_{AA} = 3.3\text{V}$, $V_{AAPIX} = 3.3\text{V}$, $T_A = 25^\circ\text{C}$)

Symbol	Definition	Condition	Min	Typ	Max	Units
ISTDBYD	Digital standby current	STDBY = V_{DD} , CLKIN = 0 MHz	—	9	20	mA
ISTDBYD w/CLK	Digital standby current	STDBY = V_{DD} , CLKIN = 48 MHz	—	55	125	μA
ISTDBYDA	Analog standby current	STDBY = V_{DD}	—	80	100	μA

Table 10: AC Electrical Characteristics

 (AC Setup Conditions: $f_{CLKIN} = 48 \text{ MHz}$, $V_{DD} = 3.3\text{V}$, $V_{AA} = 3.3\text{V}$, $V_{AAPIX} = 3.3\text{V}$, Output Load = 30pF, $T_A = 25^\circ\text{C}$)

Symbol	Definition	Condition	Min	Typ	Max	Unit
f_{CLKIIN}	Input clock frequency		1	—	48	MHz
t_{CLKIN}	Input clock period		1000	—	20.83	ns
T	PIXCLK period		1000	—	20.83	ns
t_R	Input clock rise time			4		V/ns
t_F	Input clock fall time		—	4		V/ns
	Clock duty cycle		45/55	50/50	55/45	%
t_{CP}	CLKIN to PIXCLK propagation delay		—	10	—	ns
t_{PD}	PIXCLK to data valid		—	—	1	ns
t_{PFH}	PIXCLK to FV high		—	—	7	ns
t_{PLH}	PIXCLK to LV high		—	—	7	ns
t_{PFL}	PIXCLK to FV low		—	—	3	ns
t_{PLL}	PIXCLK to LV low		—	—	2	ns
t_{OS}	Setup time for data before falling edge of PIXCLK		T/2 - 1	T/2	T/2 + 1	ns
t_{OH}	Hold time for data after falling edge of PIXCLK		T/2 - 1	T/2	T/2 + 1	ns
t_{FVS}	Setup time for FV before falling edge of PIXCLK		2	3	—	ns
t_{LVS}	Setup time for LV before falling edge of PIXCLK		2	3	—	ns
CLOAD	Load capacitance				30	pF

Table 11: Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit
		MIN	MAX	
TOP	Operating temperature	0	70	$^\circ\text{C}$
TSTG ¹	Storage temperature	-40	125	$^\circ\text{C}$

Note: ¹Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Two-wire Serial Bus Timing

The two-wire serial bus operation requires certain minimum master clock cycles between transitions. These are specified in the following diagrams in master clock cycles.

Figure 18: Serial Host Interface Start Condition Timing

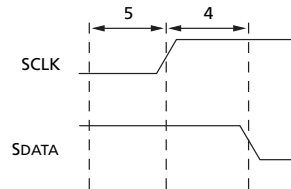
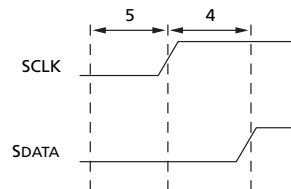
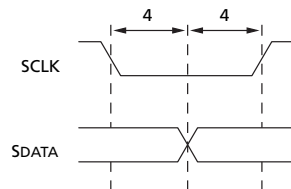


Figure 19: Serial Host Interface Stop Condition Timing



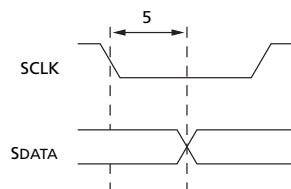
Note: All timing are in units of master clock cycle.

Figure 20: Serial Host Interface Data Timing for Write



Note: SDATA is driven by an off-chip transmitter.

Figure 21: Serial Host Interface Data Timing for Read



Note: SDATA is pulled LOW by the sensor, or allowed to be pulled HIGH by a pull-up resistor off-chip.

Figure 22: Acknowledge Signal Timing After an 8-Bit Write to the Sensor

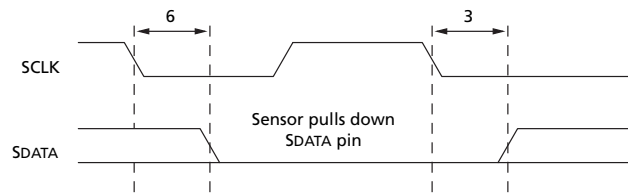
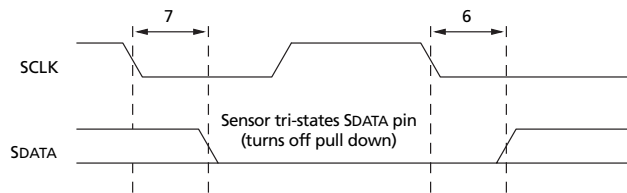


Figure 23: Acknowledge Signal Timing After an 8-Bit Read from the Sensor



Note: After a read, the master receiver must pull down SDATA to acknowledge receipt of data bits. When read sequence is complete, the master must generate a no acknowledge by leaving SDATA to float HIGH. On the following cycle, a start or stop bit may be used.

Quantum Efficiency

Figure 24: Quantum Efficiency—Monochrome

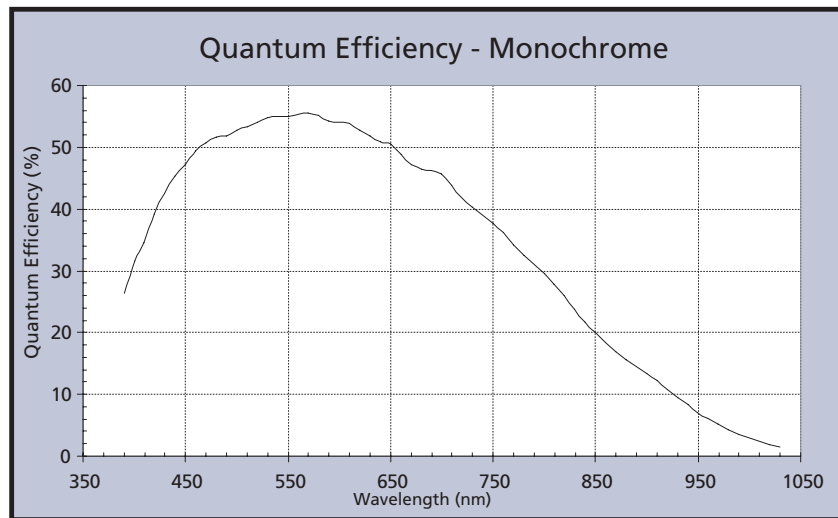


Image Center Offset and Orientation

Figure 25: Image Center Offset

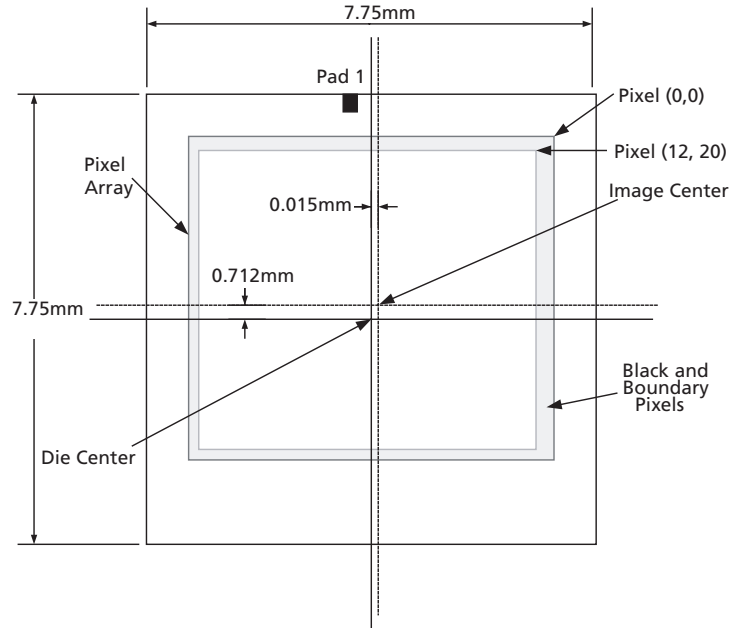


Table 12: Optical Area Dimensions

Optical Area	Pixel	X-Dimension	Y-dimension
SXGA	Center of pixel (20, 12)	3,340.70 μ m	3,372.45 μ m
	Center of Pixel (1299, 1035)	-3,315.2 μ m	-1,952.35 μ m
Chip Size, mm	(including Seal Ring)	7.75mm	7.75mm

- Notes: 1. X and Y coordinates referenced to center of die.
 2. Die center = package center.
 3. Image center offset from package center (x = 0.015mm, y = 0.712mm).

Figure 26: Optical Orientation

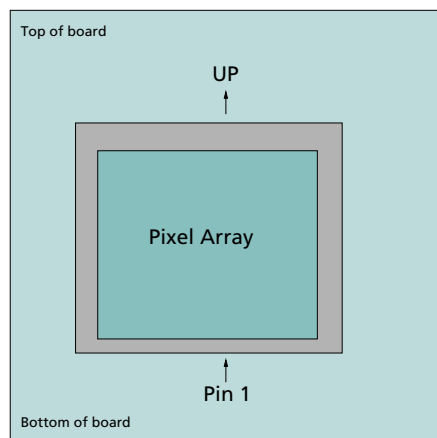
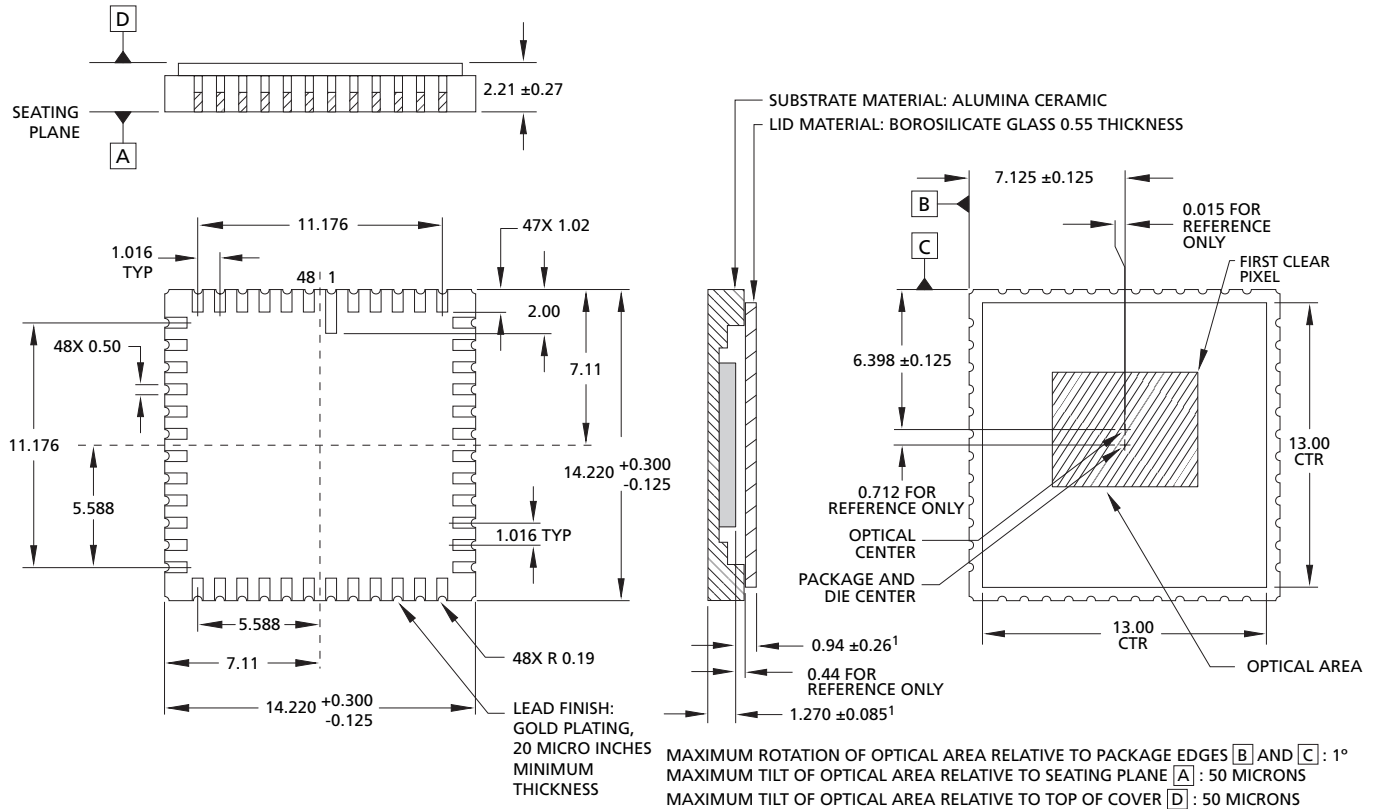


Figure 27: 48-pin CLCC Package Outline Drawing



Note: All dimensions in millimeters.



8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
 prodmktg@micron.com www.micron.com Customer Comment Line: 800-932-4992
 Micron, the M logo, and the Micron logo are trademarks of Micron Technology, Inc.

All other trademarks are the property of their respective owners.

This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

Revision History

Rev C, 06/2005

- Remove color information
- Updated Table 1, Key Performance Parameters, on page 1
- Updated Table 5, Register List and Default Values, on page 13
- Updated Table 6, Register Description, on page 14
- Updated Figure 12, Readout of Six Rows in Normal and Row Mirror Output Mode, on page 21
- Deleted Figure 13, Readout of Eight Pixels in Normal and Column Skip Output Mode, on page 22
- Updated Table 10, AC Electrical Characteristics, on page 27
- Updated Figure 25, Image Center Offset, on page 30
- Updated Figure 27, 48-pin CLCC Package Outline Drawing, on page 31

Rev B, 05/2005

- Page 1, remove PRELIMINARY disclaimer
- Page 1, add Key Performance Parameters table, add APPLICATIONS
- Page 2, add Table of Contents
- Page 6, update Pin Description table
- Page 11, update Serial Bus Description
- Page 12, update Timing Diagram Showing a Read from Reg0x09; Returned Value 0x0284 figure
- Page 13, update Register List and Default Values table
- Page 14, update Register Description Table (add Test Data-Reg0x32[11:2], update Output Control-Reg0x07[6])
- Page 28, update AC and DC Electrical Characteristics table
- Page 29, add Figure 17, Data Output Timing Diagram, and Absolute Maximum Ratings, Table 11
- Page 30, update Propagation Delay for Frame_Valid and Line_Valid Signals (Data Output and Propagation Delays)
- Page 32, delete Quantum Efficiency figure (Color)
- Page 33, update Figure 27, 48-pin CLCC Package Outline Drawing

Rev A, Preliminary 11/2003

- Initial Release of document