CY74FCT16373T
CY74FCT162373T

16-Bit Latches

SCCS054B - August 1994 - Revised September 2001

Features

- **I_{off} supports partial-power-down mode operation**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000V**
- **TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages**
- **Industrial temperature range of −40˚C to +85˚C**
- **V_{CC} = 5V ± 10%**

CY74FCT16373T Features:

- **64 mA sink current, 32 mA source current**
- **Typical V_{OLP} (ground bounce) <1.0V at V_{CC} = 5V, T_A = 25˚C**

CY74FCT162373T Features:

- **Balanced 24 mA output drivers**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, T_A= 25˚C**

Functional Description

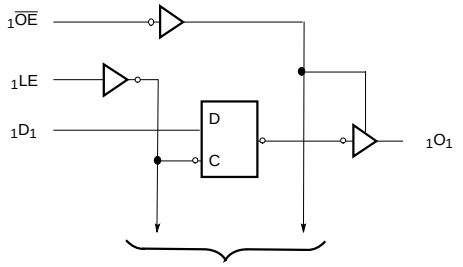
CY74FCT16373T and CY74FCT162373T are 16-bit D-type latches designed for use in bus applications requiring high speed and low power. These devices can be used as two independent 8-bit latches or as a single 16-bit latch by connecting the Output Enable ($\overline{OE}$) and Latch (LE) inputs. Flow-through pinout and small shrink packaging aid in simplifying board layout.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The CY74FCT16373T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162373T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162373T is ideal for driving transmission lines.

Logic Block Diagrams



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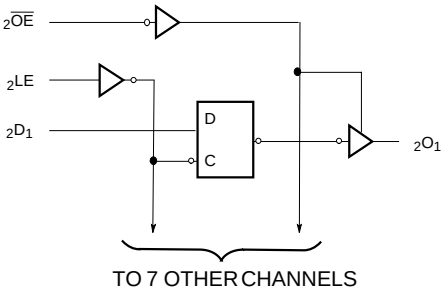
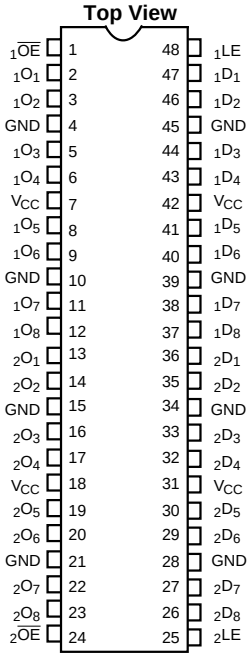


FCT162373-2

Pin Configuration

SSOP/TSSOP
Top View



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Pin Description

Name	Description
D	Data Inputs
LE	Latch Enable Inputs (Active HIGH)
$\overline{OE}$	Output Enable Inputs (Active LOW)
O	Three-State Outputs

Function Table[1]

Inputs			Outputs
D	**LE**	**$\overline{OE}$**	**O**
H	H	L	H
L	H	L	L
X	L	L	Q_0
X	X	H	Z

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... Com'l –55°C to +125°C

Ambient Temperature with Power Applied ..... Com'l –55°C to +125°C

DC Input Voltage .....–0.5V to +7.0V

DC Output Voltage .....–0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .....–60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage.....>2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.[4]	Max.	Unit
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
V_H	Input Hysteresis[5]			100		mV
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=–18 mA		–0.7	–1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_I=V_{CC}			±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_I=GND			±1	µA
I_{OZH}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=2.7V			±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=0.5V			±1	µA
I_{OS}	Short Circuit Current[6]	V_{CC}=Max., V_{OUT}=GND	–80	–140	–200	mA
I_O	Output Drive Current[6]	V_{CC}=Max., V_{OUT}=2.5V	–50		–180	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}≤4.5V[7]			±1	µA

Output Drive Characteristics for CY74FCT16373T

Parameter	Description	Test Conditions	Min.	Typ.[4]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=–3 mA	2.5	3.5		V
		V_{CC}=Min., I_{OH}=–15 mA	2.4	3.5		V
		V_{CC}=Min., I_{OH}=–32 mA	2.0	3.0		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA		0.2	0.55	V

Notes:

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = High Impedance. Q_0=Previous state of flip-flop.
2. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. Typical values are at V_{CC}=5.0V, T_A= +25˚C ambient.
5. This parameter is specified but not tested.
6. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
7. Tested at +25˚C.

Output Drive Characteristics for CY74FCT162373T

Parameter	Description	Test Conditions	Min.	Typ.[4]	Max.	Unit
I_{ODL}	Output LOW Current[6]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	60	115	150	mA
I_{ODH}	Output HIGH Current[6]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=–24 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=24 mA		0.3	0.55	V

Capacitance[5] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ.[4]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Power Supply Characteristics

Parameter	Description	Test Conditions		Typ.[4]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	V_{IN}≤0.2V, V_{IN}≥V_{CC}–0.2V	5	500	µA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max.	V_{IN}=3.4V[8]	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=GND	V_{IN}=V_{CC} or V_{IN}=GND	60	100	µA/MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., f_1=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE}$=GND, LE=V_{CC}	V_{IN}=V_{CC} or V_{IN}=GND	0.6	1.5	mA
			V_{IN}=3.4V or V_{IN}=GND	0.9	2.3	mA
		V_{CC}=Max., f_1=2.5 MHz, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, $\overline{OE}$=GND, LE=V_{CC}	V_{IN}=V_{CC} or V_{IN}=GND	2.4	4.5[11]	mA
			V_{IN}=3.4V or V_{IN}=GND	6.4	16.5[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C= $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
    I_C = I_{CC}+$\Delta I_{CC} D_H N_T$+$I_{CCD}(f_0/2 + f_1 N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input(V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics Over the Operating Range[12]

Parameter	Description	CY74FCT16373AT CY74FCT162373AT		Unit	Fig. No.[13]
		Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay D to O	1.5	5.2	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay LE to O	2.0	6.7	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5	6.1	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	5.5	ns	1, 7, 8
t_{SU}	Set-Up Time HIGH or LOW, D to LE	2.0		ns	9
t_{H}	Hold Time HIGH or LOW, D to LE	1.5		ns	9
t_{W}	LE Pulse Width HIGH	3.3		ns	5
$t_{SK(O)}$	Output Skew[14]		0.5	ns	—

Parameter	Description	CY74FCT16373CT CY74FCT162373CT		Unit	Fig. No.[13]
		Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay D to O	1.5	4.2	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay LE to O	2.0	5.5	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5	5.5	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	5.0	ns	1, 7, 8
t_{SU}	Set-Up Time HIGH or LOW, D to LE	2.0		ns	9
t_{H}	Hold Time HIGH or LOW, D to LE	1.5		ns	9
t_{W}	LE Pulse Width HIGH	3.3		ns	5
$t_{SK(O)}$	Output Skew[14]		0.5	ns	—

Notes:
12. Minimum limits are specified but not tested on Propagation Delays.
13. See “Parameter Measurement Information” in the General Information section.
14. Skew between any two outputs of the same package switching in the same direction. This parameter is ensured by design.

Ordering Information CY74FCT16373

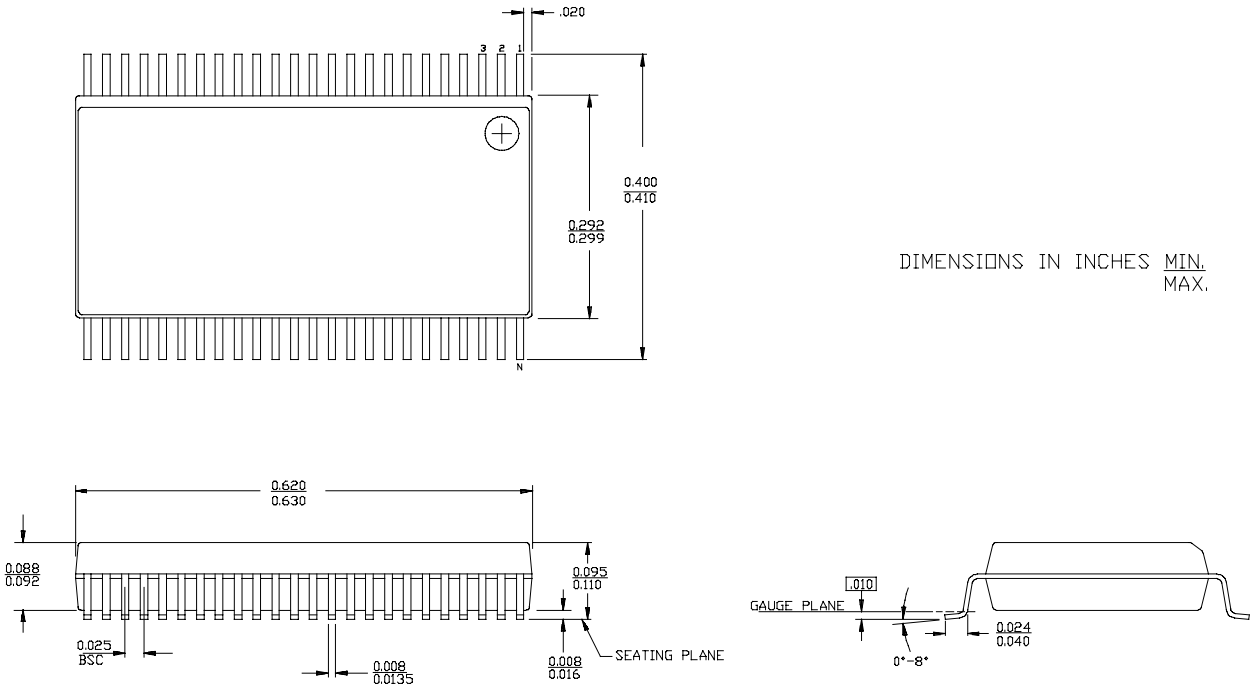
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	CY74FCT16373CTPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16373CTPVC/PVCT	O48	48-Lead (300-Mil) SSOP	
5.2	CY74FCT16373ATPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16373ATPVC/PVCT	O48	48-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162373

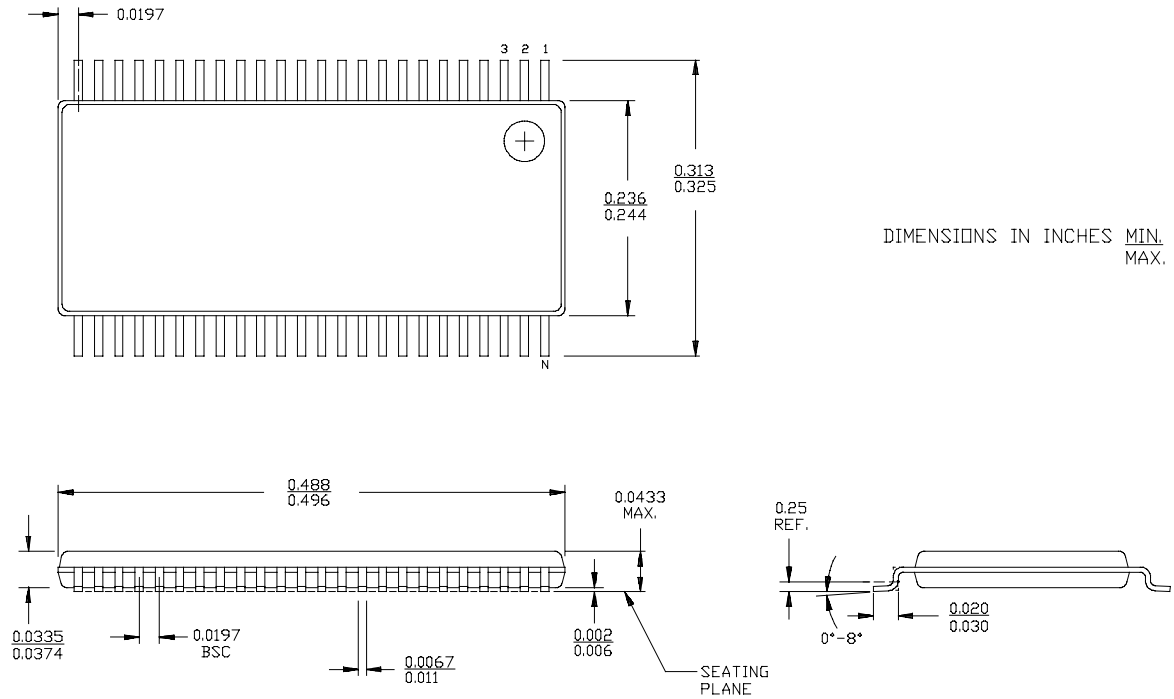
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	74FCT162373CTPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162373CTPVC	O48	48-Lead (300-Mil) SSOP	
	74FCT162373CTPVCT	O48	48-Lead (300-Mil) SSOP	
5.2	74FCT162373ATPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162373ATPVC	O48	48-Lead (300-Mil) SSOP	
	74FCT162373ATPVCT	O48	48-Lead (300-Mil) SSOP	

Package Diagrams

48-Lead Shrunk Small Outline Package O48



48-Lead Thin Shrunk Small Outline Package Z48



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