SONY

CXP750096/750010
CXP750097/750011

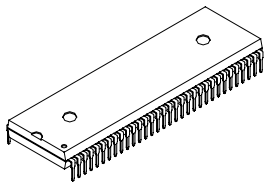
CMOS 8-bit Single Chip Microcomputer

Description

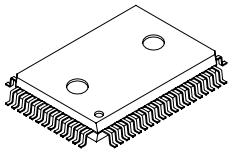
The CXP750096/750010, CXP750097/750011 are the CMOS 8-bit single chip microcomputer integrating on a single chip an A/D converter, serial interface, timer/ counter, time-base timer, on-screen display function, I^2C bus interface, PWM output, remote control reception circuit, HSYNC counter, watchdog timer, 32kHz timer/ counter besides the basic configurations of 8-bit CPU, ROM, RAM, I/O ports.

The CXP750096/750010, CXP750097/750011 also provide a sleep function that enables to lower the power consumption.

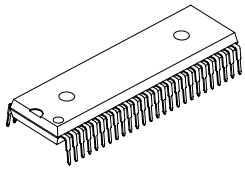
64 pin SDIP (Plastic)



64 pin QFP (Plastic)



52 pin SDIP (Plastic)



Features

- A wide instruction set (213 instructions) which covers various types of data
  - 16-bit operation/multiplication and division/ Boolean bit operation instructions
- Minimum instruction cycle 167ns at 24MHz operation
  122µs at 32kHz operation
- Incorporated ROM 96K bytes (CXP750096/750097)
  120K bytes (CXP750010/750011)
- Incorporated RAM 2496 bytes
  (Excludes VRAM for on-screen display)
- Peripheral functions

– A/D converter	8-bit 6-channel successive approximation method (Conversion time of 3.25µs at 16MHz)
– Serial interface	8-bit clock sync type, 1 channel
– Timer	8-bit timer 8-bit timer/counter 19-bit time-base timer 32 kHz timer/counter
– On-screen display (OSD) function	24 × 32 dots, 512 character types, 15 character colors, 2 lines × 32 characters, frame background 8 colors/ half blanking, background on full screen 15 colors/ half blanking edging/ shadowing/ rounding for every line, background with shadow for every character, double scanning, sprite OSD, 24 × 32 dots, 1 screen, 8 colors for every dot
– I^2C bus interface	
– PWM output	8 bits, 8 channels 14 bits, 1 channel
– Remote control reception circuit	8-bit pulse measurement counter, 6-stage FIFO
– HSYNC counter	2 channels
– Watchdog timer	
• Interruption	13 factors, 13 vectors, multi-interruption possible
• Standby mode	Sleep
• Package	64-pin plastic SDIP/QFP, 52-pin plastic SDIP
• Piggyback/evaluator	CXP750000 64-pin ceramic PQFP/PSDIP (Supports custom font)

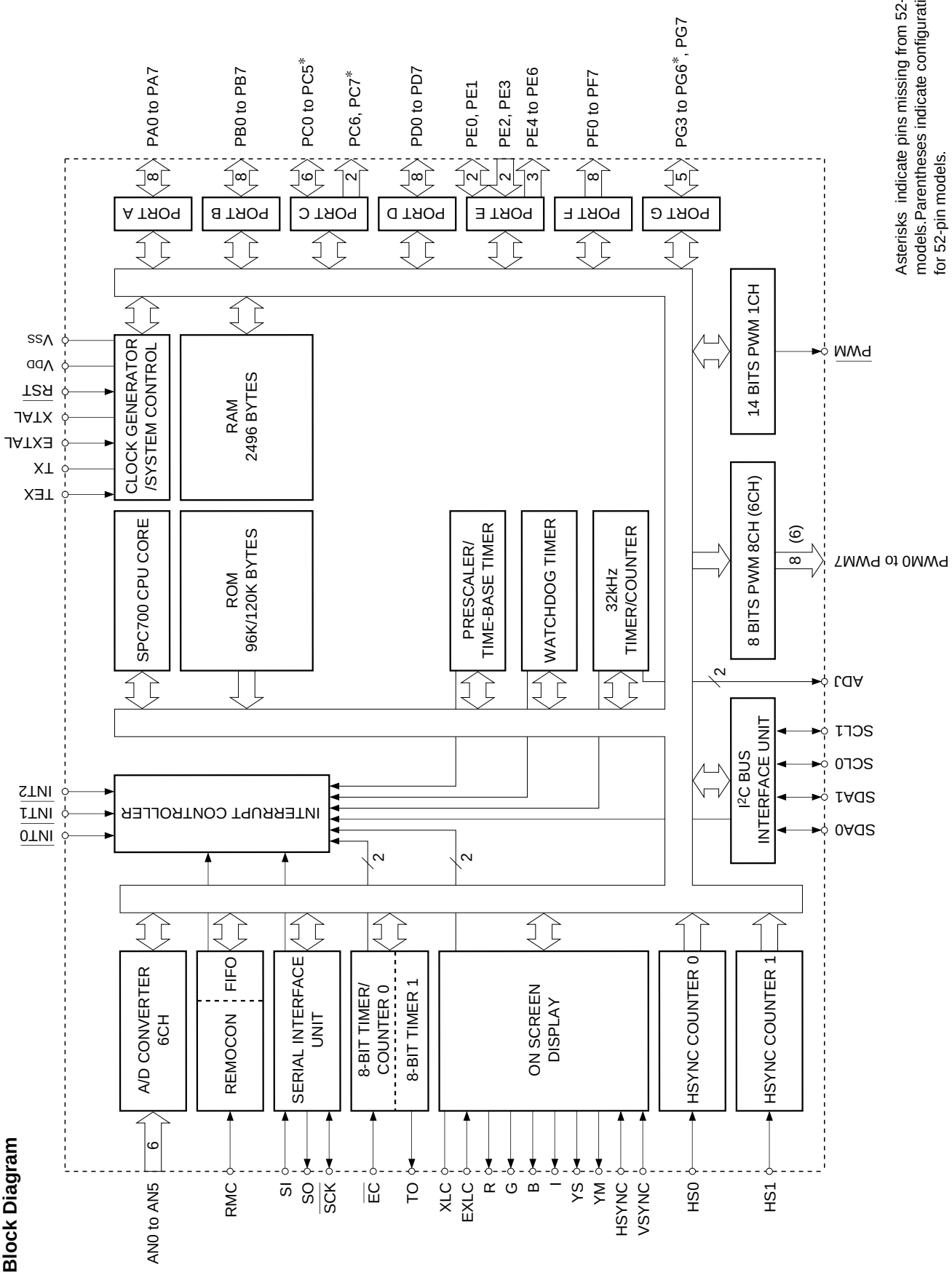
Structure

Silicon gate CMOS IC

Perchase of Sony's I^2C components conveys a licence under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specifications as defined by Philips.

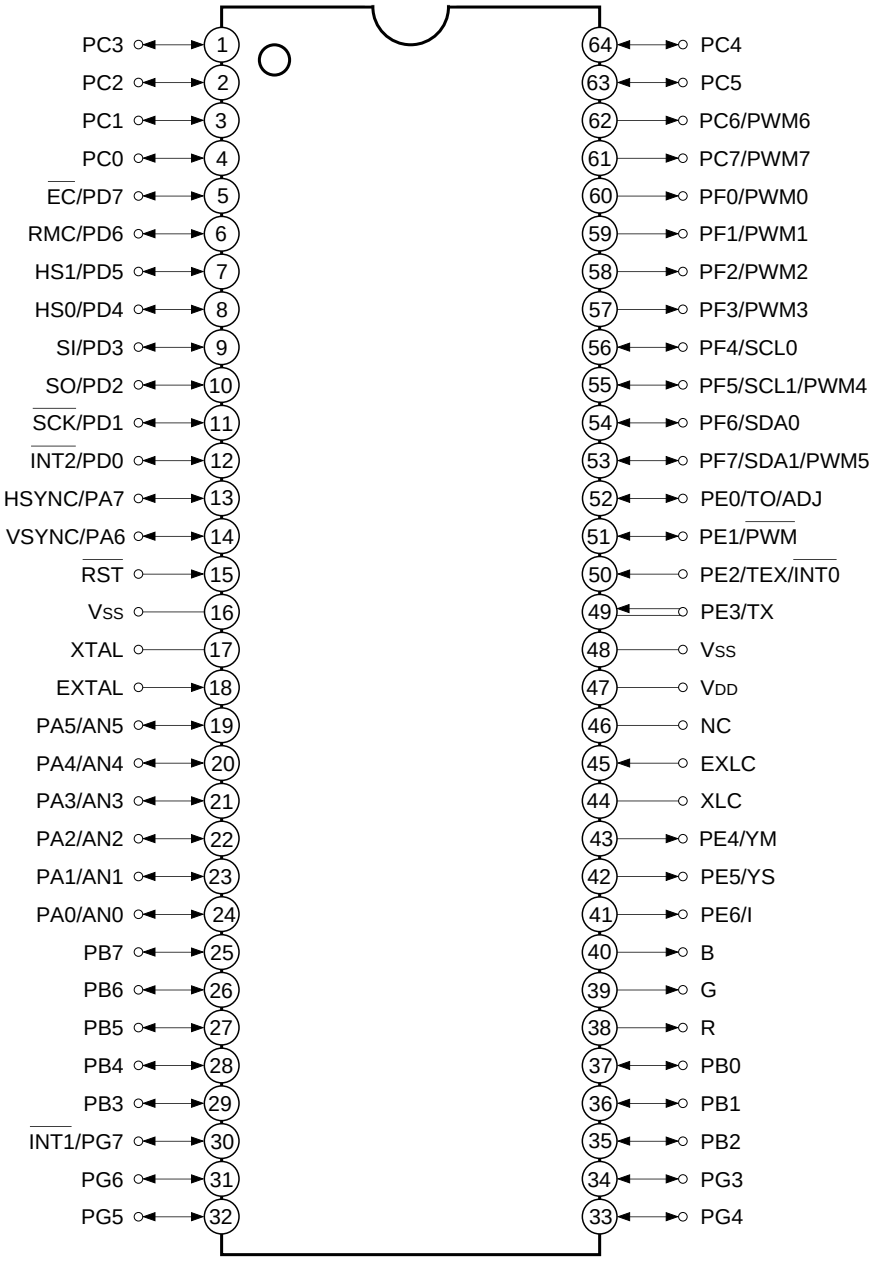
E98767A17-PS

Block Diagram



Asterisks indicate pins missing from 52-pin models. Parentheses indicate configurations for 52-pin models.

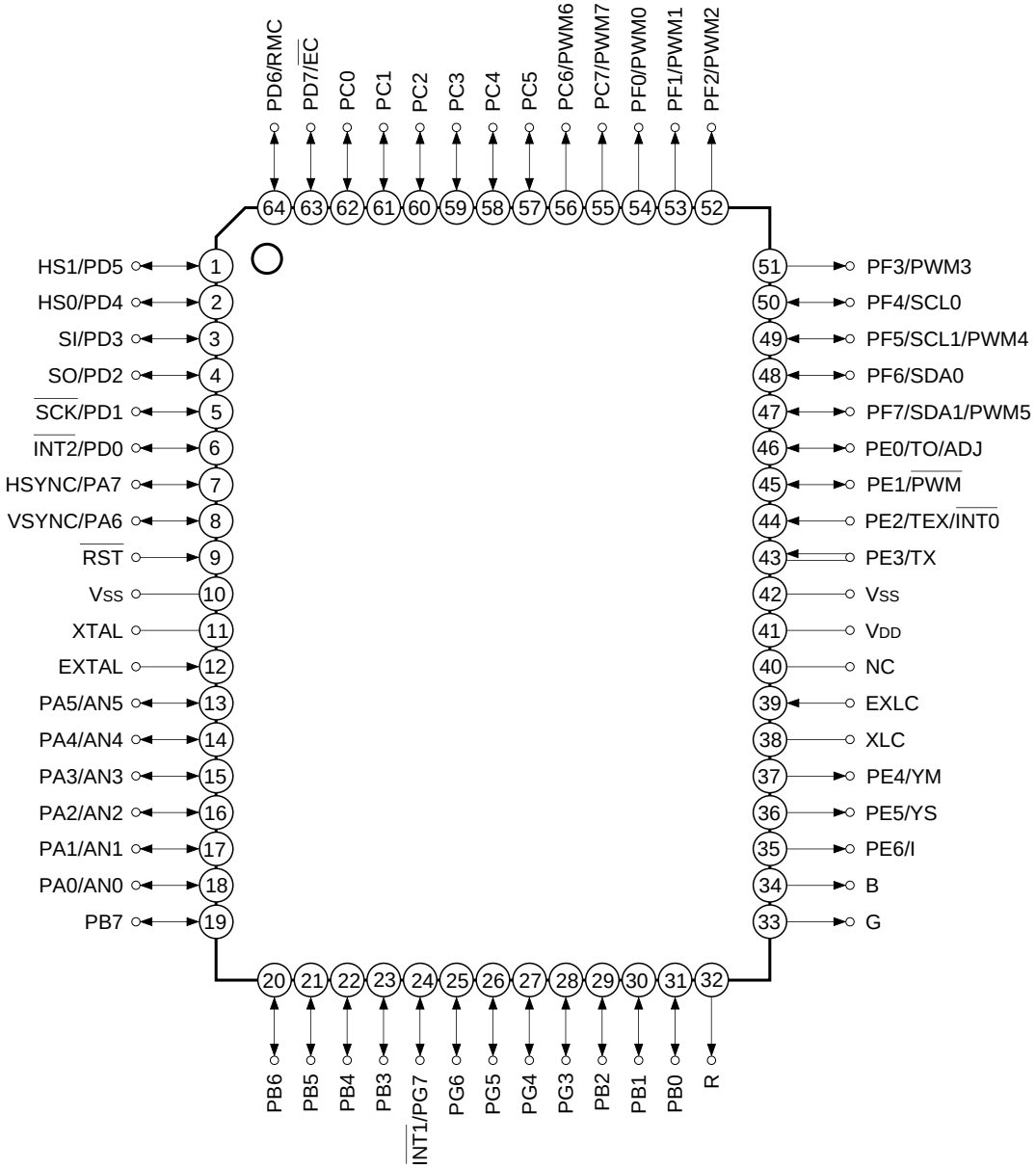
Pin Assignment (Top View) 64-pin SDIP



Note)

1. NC (Pin 46) is left open.
2. Vss (Pins 16 and 48) are both connected to GND.

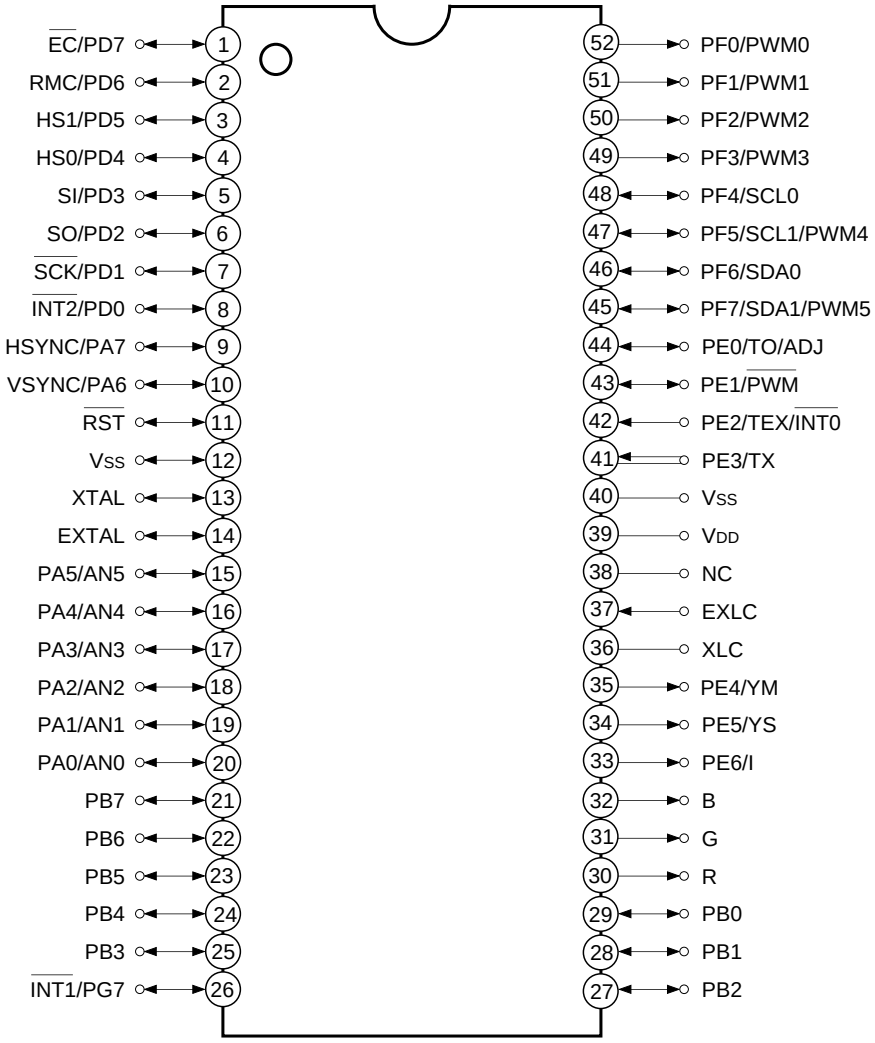
Pin Assignment (Top View) 64-pin QFP



Note)

1. NC (Pin 40) is left open.
2. Vss (Pins 10 and 42) are both connected to GND.

Pin Assignment (Top View) 52-pin SDIP



Note)

1. NC (Pin 38) is left open.
2. Vss (Pins 12 and 40) are both connected to GND.

Pin Description

Symbol	I/O	Description		
PA0/AN0 to PA5/AN5	I/O/ Analog input	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	Analog inputs to A/D converter. (6 pins)	
PA6/VSYNC	I/O/Input		OSD display vertical sync signal input.	
PA7/HSYNC	I/O/Input		OSD display horizontal sync signal input.	
PB0 to PB7	I/O	(Port B) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)		
PC0 to PC5*	I/O	(Port C) Lower 6 bits are I/O ports; I/O can be set in a unit of single bits. Upper 2 bits are output port and large current (12mA) N-channel open drain output. Upper 2 bits are medium drive voltage (12V); lower 6 bits are 5V drive. (8 pins)		
PC6/PWM6* to PC7/PWM7*	Output/Output		8-bit PWM output. (2 pins)	
PD0/$\overline{INT2}$	I/O/Input	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. Can drive 12mA synk current. (8 pins)	External interruption request input. Active at the falling edge.	
PD1/$\overline{SCK}$	I/O/I/O		Serial clock I/O.	
PD2/SO	I/O/Output		Serial data output.	
PD3/SI	I/O/Input		Serial data input.	
PD4/HS0	I/O/Input		HSYNC counter (CH0) input.	
PD5/HS1	I/O/Input		HSYNC counter (CH1) input.	
PD6/RMC	I/O/Input		Remote control reception circuit input.	
PD7/$\overline{EC}$	I/O/Input		External event input for timer/counter.	
PE0/TO/ADJ	I/O/Output/ Output	(Port E) Bits 0 and 1 are I/O port; I/O can be set in a unit of single. Bits 2 and 3 are input port. Bits 4, 5 and 6 are output port. (7 pins)	Rectangular wave output for 8-bit timer/counter.	TEX oscillation frequency dividing output.
PE1/$\overline{PWM}$	I/O/Output		14-bit PWM output.	
PE2/TEX/$\overline{INT0}$	Input/Input/ Input		Connects a crystal for 32kHz timer/counter clock oscillation. When used as an event counter, input to TEX pin and leave TX pin open.	External interruption request input. Active at the falling edge.
PE3/TX	Input/Output			
PE4/YM	Output/Output		OSD display 6-bit output. (6 pins)	
PE5/YS	Output/Output			
PE6/I	Output/Output			
B	Output			
G	Output			
R	Output			

* Not incorporated for Pin 52 package.

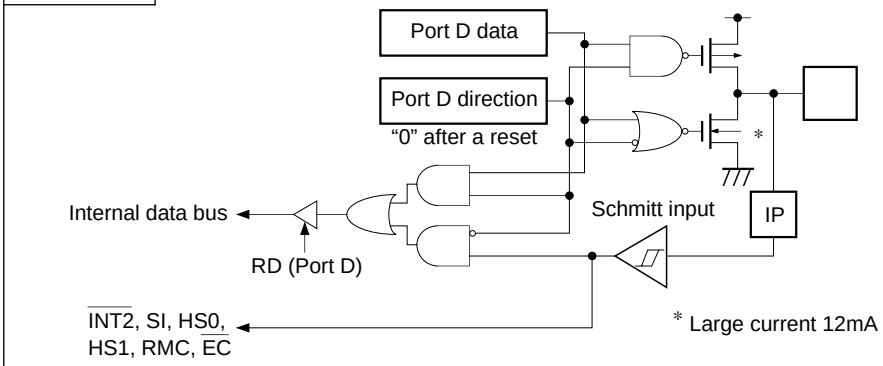
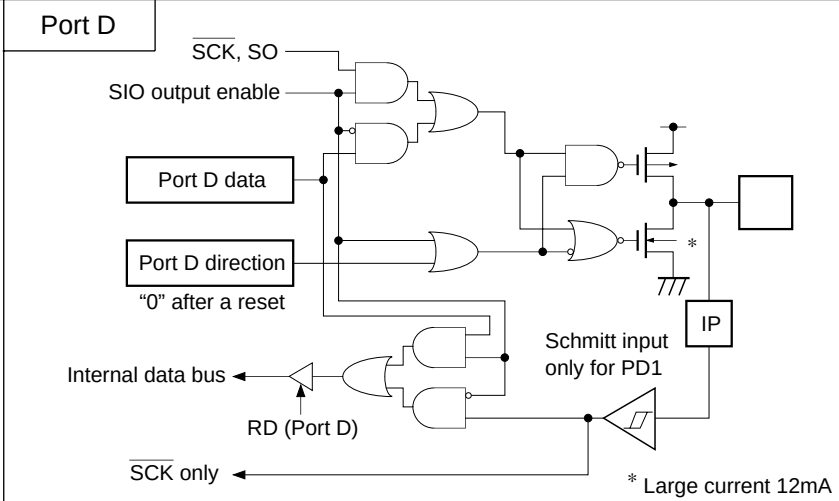
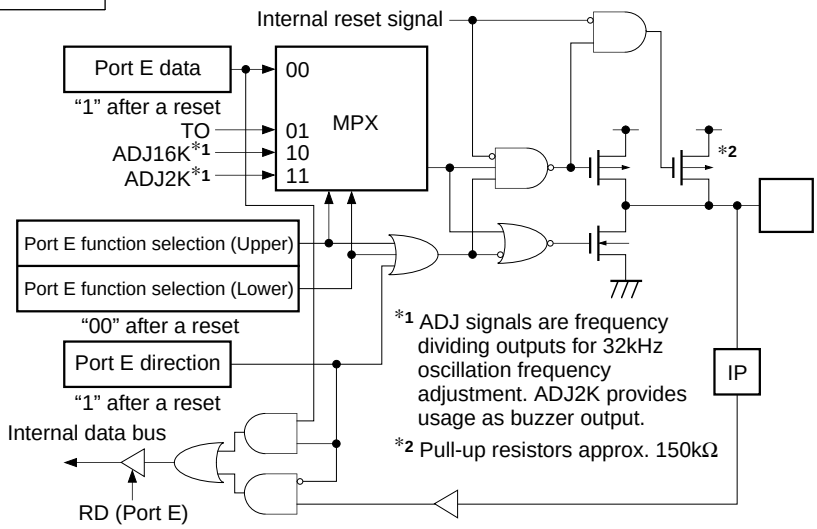
Symbol	I/O	Description		
PF0/PWM0 to PF3/PWM3	Output/Output	(Port F) 8-bit output port and large current (12mA) N-channel open drain output. Lower 4 bits are medium drive voltage (12V); upper 4 bits are 5V drive. (8 pins)	8-bit PWM output. (4 pins)	
PF4/SCL0	Output/I/O		I^2C bus interface transfer clock I/O. (2 pins)	
PF5/SCL1/ PWM4	Output/I/O/ Output			8-bit PWM output.
PF6/SDA0	Output/I/O		I^2C bus interface transfer data I/O. (2 pins)	
PF7/SDA1/ PWM5	Output/I/O/ Output			8-bit PWM output.
PG3 to PG6*	I/O	(Port G) 5-bit I/O port. I/O can be set in a unit of single bits. (5 pins)		
PG7/$\overline{INT1}$	I/O/Input		External interruption request input. Active at the falling edge.	
EXTAL	Input	Connects a crystal for system clock oscillation. When a clock is supplied externally, input to EXTAL pin and input a reversed phase clock to XTAL pin.		
XTAL	Output			
$\overline{RST}$	Input	System reset; active at Low level.		
EXLC	Input	OSD display clock oscillation I/O. Oscillation frequency is determined by the external L and C.		
XLC	Output			
NC		No connected.		
V_{DD}		Positive power supply.		
Vss		GND. Connect two Vss pins to GND.		

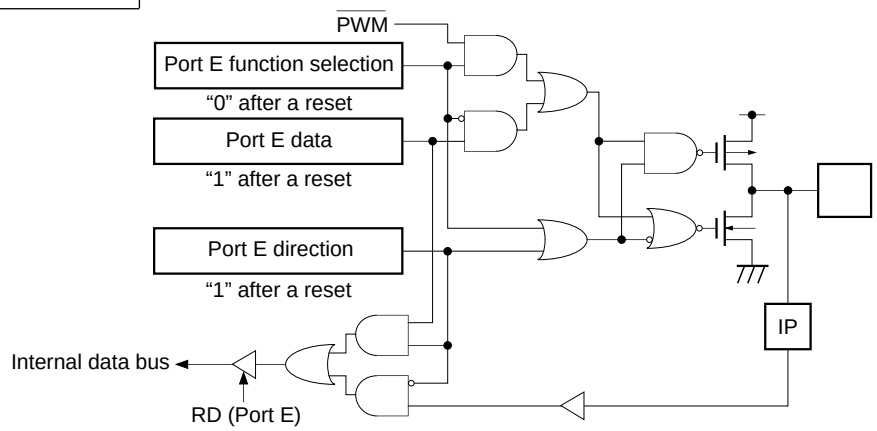
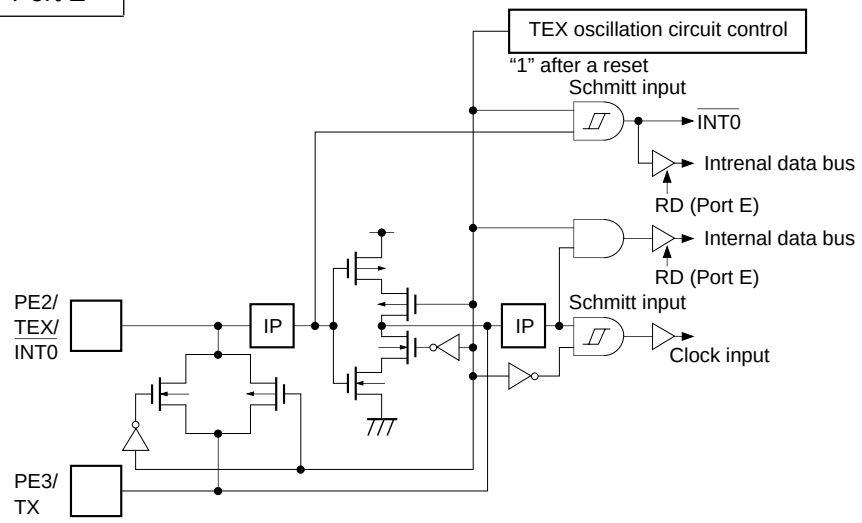
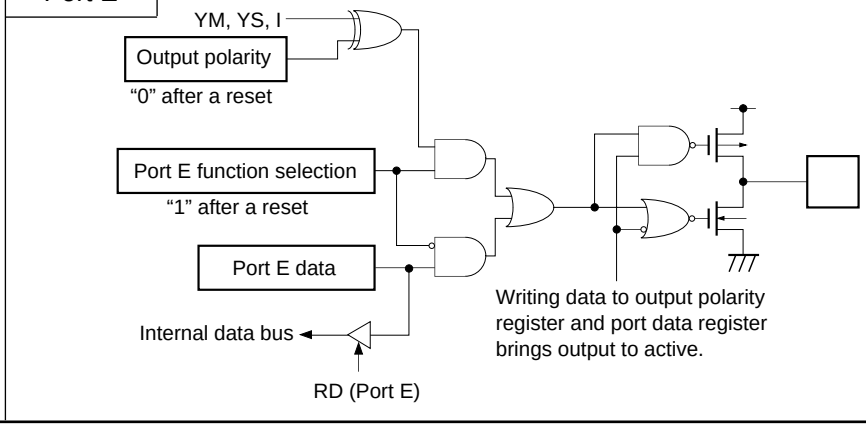
* Not incorporated for Pin 52 package.

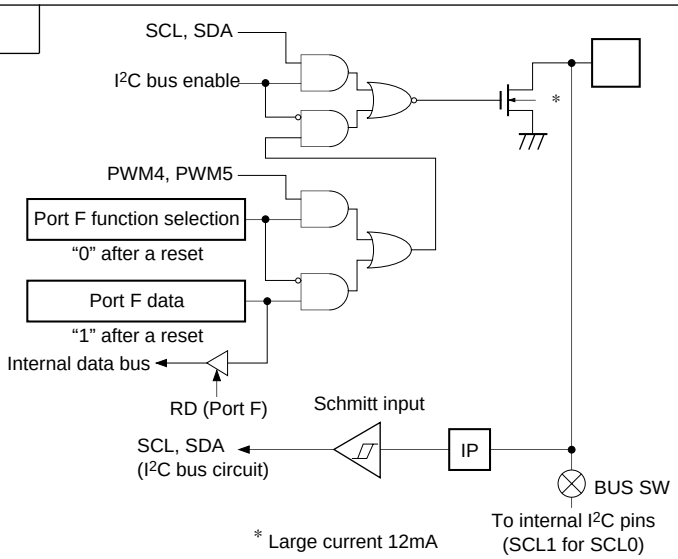
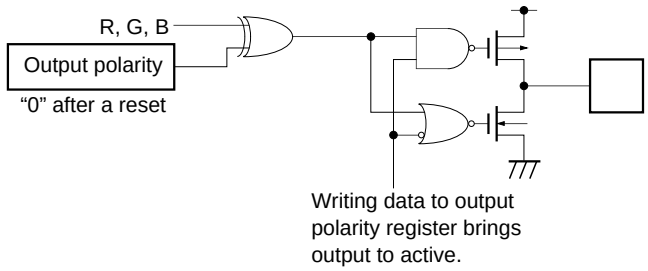
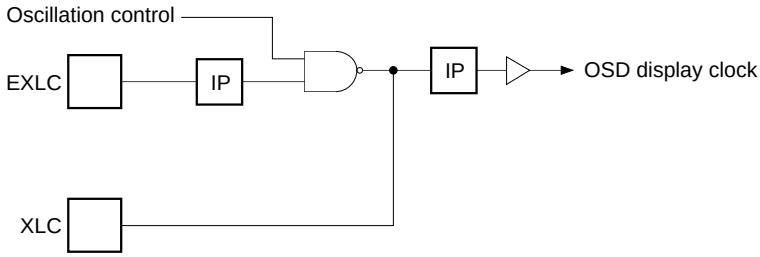
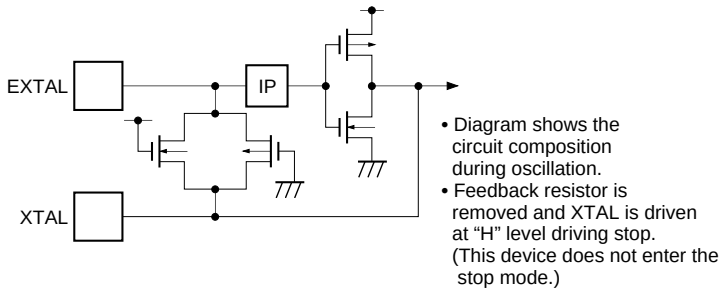
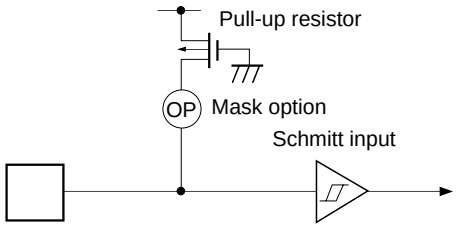
Input/Output Circuit Formats for Pins

Pin	Circuit format	After a reset
PA0/AN0 to PA5/AN5 6 pins	Port A Port A data Port A direction "0" after a reset Internal data bus RD (Port A) IP Input protection circuit Port A function selection "0" after a reset Input multiplexer A/D converter	Hi-Z
PA6/VSYNC PA7/HSYNC 2 pins	Port A Port A data Port A direction "0" after a reset Internal data bus RD (Port A) Schmitt input IP HSYNC, VSYNC Input polarity "0" after a reset	Hi-Z
PB0 to PB7 PC0 to PC5*2 PG3 to PG6*2 PG7/$\overline{\text{INT1}}$ 19 pins	Port B Port C Port G Ports B, C, G data Ports B, C, G direction "0" after a reset Internal data bus RD (Ports B, C, G) PB0 to PB2 Schmitt input only for PG7 IP $\overline{\text{INT1}}$	Hi-Z
PC6/PWM6*2 PC7/PWM7*2 PF0/PWM0 to PF3/PWM3 6 pins	Port C Port F PWM0 to PWM3 PWM6, PWM7 Ports C and F function selection "0" after a reset Ports C and F data "1" after a reset *1 Internal data bus RD (Ports C, F) *1 12V drive voltage Large current 12mA	Hi-Z

*2 Not incorporated for Pin 52 package.

Pin	Circuit format	After a reset
PD0/$\overline{INT2}$ PD3/SI PD4/HS0 PD5/HS1 PD6/RMC PD7/$\overline{EC}$ 6 pins	Port D  	Hi-Z
PD1/$\overline{SCK}$ PD2/SO 2 pins	Port D  	Hi-Z
PE0/TO/ADJ 1 pin	Port E  	High level (H level at ON resistance of pull-up transistor during a reset)

Pin	Circuit format	After a reset
PE1/$\overline{PWM}$ 1 pin	Port E 	High level
PE2/TEX/$\overline{INT0}$ PE3/TX 2 pins	Port E 	Oscillation halted Port input
PE4/YM PE5/YS PE6/I 3 pins	Port E 	Hi-Z

Pin	Circuit format	After a reset
PF4/SCL0 PF5/SCL1/PWM4 PF6/SDA0 PF7/SDA1/PWM5 4 pins	Port F 	Hi-Z
R G B 3 pins		Hi-Z
EXLC XLC 2 pins		Oscillation halted
EXTAL XTAL 2 pins		Oscillation
$\overline{\text{RST}}$ 1 pin		Low level (during a reset)

Absolute Maximum Ratings (Vss = 0V reference)

Item	Symbol	Ratings	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +7.0	V	
Input voltage	V_{IN}	–0.3 to +7.0*1	V	
Output voltage	V_{OUT}	–0.3 to +7.0*1	V	
Medium drive output voltage	V_{OUTP}	–0.3 to +15.0	V	
High level output current	I_{OH}	–5	mA	
High level total output current	$\sum I_{OH}$	–50	mA	Total of all output pins
Low level output current	I_{OL}	15	mA	Ports excluding large current output (value per pin)
	I_{OLC}	20	mA	Large current output ports (value per pin*2)
Low level total output current	$\sum I_{OL}$	130	mA	Total of all output pins
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	1000	mW	SDIP-64P-01
		600	mW	QFP-64P-L01

*1 V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.

*2 The large current output port is Port C (PC6, PC7), Port D (PD) and Port F (PF).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	4.5	5.5	V	Guaranteed operation range for 1/2 and 1/4 frequency dividing modes
		3.5	5.5	V	Guaranteed operation range for 1/16 frequency dividing mode or sleep
		2.7	5.5	V	Guaranteed operation range for TEX mode
		—	—	V	Guaranteed data hold range for stop*5
High level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	*1
	V_{IHS}	0.8V_{DD}	V_{DD}	V	*2
	V_{IHEX}	V_{DD} – 0.4	V_{DD} + 0.3	V	EXTAL pin*3, TEX pin*4
Low level input voltage	V_{IL}	0	0.3V_{DD}	V	*1
	V_{ILS}	0	0.2V_{DD}	V	*2
	V_{ILEX}	–0.3	0.4	V	EXTAL pin*3, TEX pin*4
Operating temperature	Topr	–20	+75	°C	

*1 This device does not enter the stop mode.

*2 PA0 to PA5, PB3 to PB7, PC0 to PC5, PD2, PE0, PE1, PE3, PG3 to PG6, SCL0, SCL1, SDA0, SDA1 pins

*3 VSYNC, HSYNC, $\overline{\text{INT2}}$, $\overline{\text{SCK}}$, SI, HS0, HS1, RMC, $\overline{\text{EC}}$, $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{RST}}$ pins

*4 Specifies only during external clock input.

*5 Specifies only during external event count input.

Electrical Characteristics

DC characteristics

(Ta = –20 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA, PB, PC0 to PC5, PD, PE0 to PE1, PE4 to PE6, PG, R, G, B	V_{DD} = 4.5V, I_{OH} = –0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = –1.2mA	3.5			V
Low level output voltage	V_{OL}	PA to PD, PE0 to PE1, PE4 to PE6, PF0 to PF3, PG, R, G, B	V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PC6, PC7, PD, PF	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
		PF4 to PF7 (SCL0, SCL1, SDA0, SDA1)	V_{DD} = 4.5V, I_{OL} = 3.0mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 4.0mA			0.6	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	µA
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.5		–40	µA
	I_{IHT}	TEX	V_{DD} = 5.5V, V_{IH} = 5.5V	0.1		10	µA
	I_{ILT}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.1		–10	µA
	I_{ILR}	$\overline{RST}$*1		–1.5		–400	µA
I/O leakage current	I_{IZ}	PA, PB, PC0 to PC5, PD, PE, PG, R, G, B, $\overline{RST}$*1	V_{DD} = 5.5V, V_I = 0, 5.5V			±10	µA
Open drain I/O leakage current (in N-ch Tr off state)	I_{LOH}	PC6, PC7, PF0 to PF3	V_{DD} = 5.5V, V_{OH} = 12.0V			50	µA
		PF4 to PF7	V_{DD} = 5.5V, V_{OH} = 5.5V			10	µA
I^2C bus switch connection impedance (in output Tr off state)	R_{BS}	SCL0: SCL1 SDA0: SDA1	V_{DD} = 4.5V V_{SCL0} = V_{SCL1} = 2.25V V_{SDA0} = V_{SDA1} = 2.25V			120	Ω
Supply current*2	I_{DD1}	V_{DD}	1/2 frequency dividing mode V_{DD} = 5.5V, 16MHz crystal oscillation (C_1 = C_2 = 15pF)		20	30	mA
			1/2 frequency dividing mode V_{DD} = 5.5V, 24MHz crystal oscillation		29	45	mA
	I_{DD2}		V_{DD} = 3.3V, 32kHz crystal oscillation (C_1 = C_2 = 47pF)		33	82	µA
	I_{DDS1}		Sleep mode V_{DD} = 5.5V, 24MHz crystal oscillation (C_1 = C_2 = 15pF)		2.2	3.8	mA
	I_{DDS2}		V_{DD} = 3.3V, 32kHz crystal oscillation (C_1 = C_2 = 47pF)		12	35	µA
	I_{DDS3}		Stop mode*3 V_{DD} = 5.5V, termination of 24MHz and 32kHz oscillation	—	—	—	µA

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	PA, PB,PC0 to PC5, PD,PE0 to PE3, PF4 to PF7, PG, EXTAL, EXLC, $\overline{RST}$	Clock 1 MHz 0V other than the measured pins		10	20	pF

*1 For $\overline{RST}$ pin, specifies the input current when pull-up resistance is selected, and specifies the leakage current when non-resistor is selected.

*2 When all output pins are left open. Specifies only when the OSD oscillation is halted.

*3 This device does not enter the stop mode.

AC Characteristics

(1) Clock timing

(Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig.2	8		24	MHz
System clock input pulse width	t_{XL}, t_{XH}	EXTAL	Fig. 1, Fig.2 External clock drive	17			ns
System clock input rise and fall times	t_{CR}, t_{CF}	EXTAL	Fig. 1, Fig.2 External clock drive			200	ns
Event count input clock pulse width	t_{EH}, t_{EL}	$\overline{EC}$	Fig. 3	4tsys*1			ns
Event count input clock rise and fall times	t_{ER}, t_{EF}	$\overline{EC}$	Fig. 3			20	ms
System clock frequency	f_C	TEX TX	V_{DD} = 2.7 to 5.5 V Fig. 2 (32kHz clock applied conditions)		32.768		kHz
Event count input clock input pulse width	t_{TL}, t_{TH}	TEX	Fig. 3	10			µs
Event count input clock rise and fall times	t_{TR}, t_{TF}	TEX	Fig. 3			20	ms

*1 Indicates three values according to the contents of the clock control register (CLC: 000FEh) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2 bits = “00”), 4000/fc (Upper 2 bits = “01”), 16000/fc (Upper 2 bits = “11”)

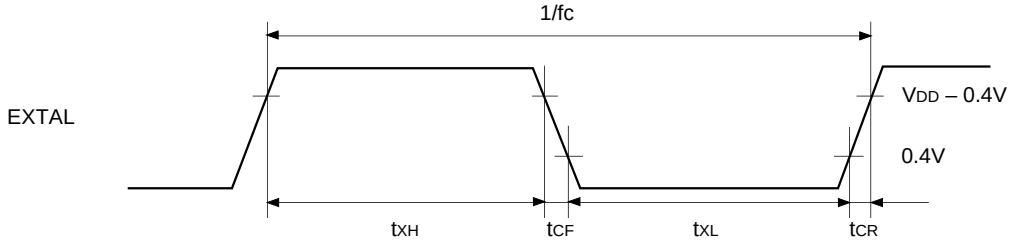


Fig. 1. Clock timing

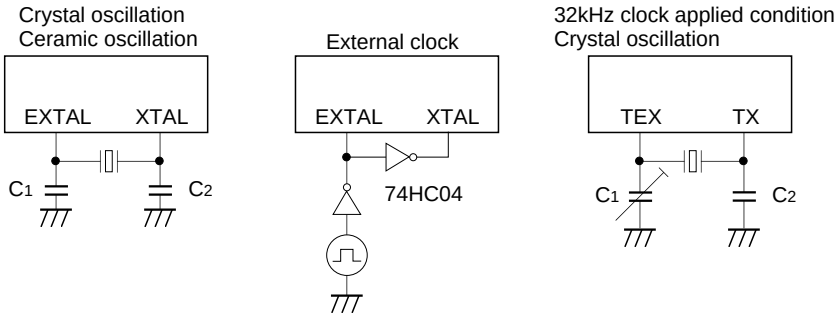


Fig.2. Clock applied conditions

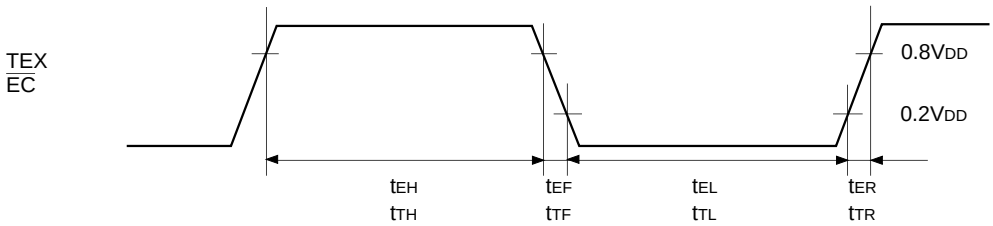


Fig. 3. Event count clock timing

(2) Serial transfer (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK}$	Input mode	1000		ns
			Output mode	8000/fc		ns
$\overline{SCK}$ High and Low level width	t_{KH} t_{KL}	$\overline{SCK}$	$\overline{SCK}$ input mode	400		ns
			$\overline{SCK}$ output mode	4000/fc – 50		ns
SI input setup time (for $\overline{SCK}$ ↑)	t_{SIK}	SI	$\overline{SCK}$ input mode	100		ns
			$\overline{SCK}$ output mode	200		ns
SI hold time (for $\overline{SCK}$ ↑)	t_{KSI}	SI	$\overline{SCK}$ input mode	200		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK}$ ↓ → SO delay time	t_{KSO}	SO	$\overline{SCK}$ input mode		200	ns
			$\overline{SCK}$ output mode		100	ns

Note) The load of $\overline{SCK}$ output mode and SO output delay time is 50pF + 1TTL.

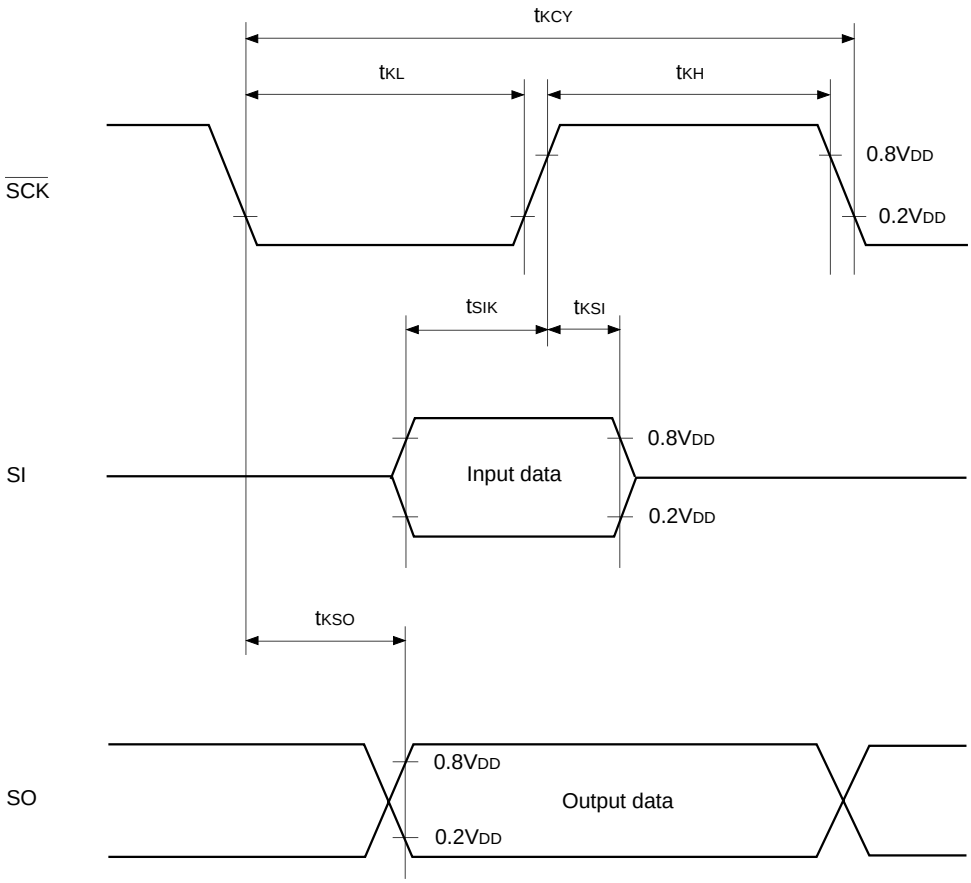
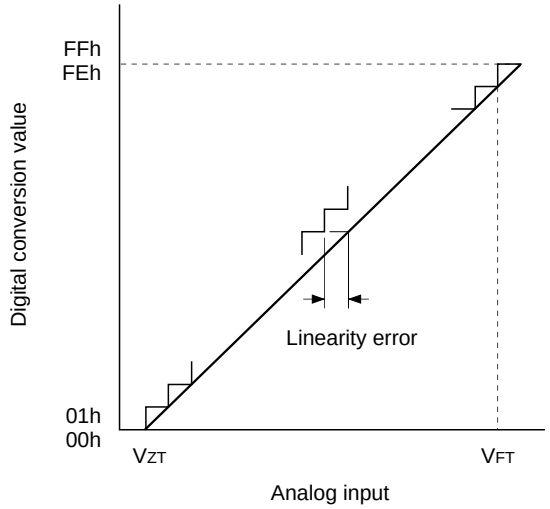


Fig. 4. Serial transfer timing

(3) A/D converter (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V_{DD} = 5.0V Vss = 0V			±3	LSB
Zero transition voltage	V_{ZT}*1			–10	10	70	mV
Full-scale transition voltage	V_{FT}*2			4910	4970	5030	mV
Conversion time	t_{CONV}			26/f_{ADC}*3			µs
Sampling time	t_{SAMP}			6/f_{ADC}*3			µs
Analog input voltage	V_{IAN}	AN0 to AN5		0		V_{DD}	V



*1 V_{ZT}: Value at which the digital conversion value changes from 00h to 01h and vice versa.

*2 V_{FT}: Value at which the digital conversion value changes from FEh to FFh and vice versa.

*3 f_{ADC} indicates the below values due to the contents of bit 6 (CKS) of the A/D control register (ADC: 000F6h):

f_{ADC} = fc (CKS = "0"), fc/2 (CKS = "1")

Fig. 5. Definitions for A/D converter terms

(4) Interruption, reset input (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
External interruption High, Low level width	t_{IH} t_{IL}	$\overline{INT0}$ $\overline{INT1}$ $\overline{INT2}$		1		µs
Reset input Low level width	t_{RSL}	$\overline{RST}$		32/fc		µs

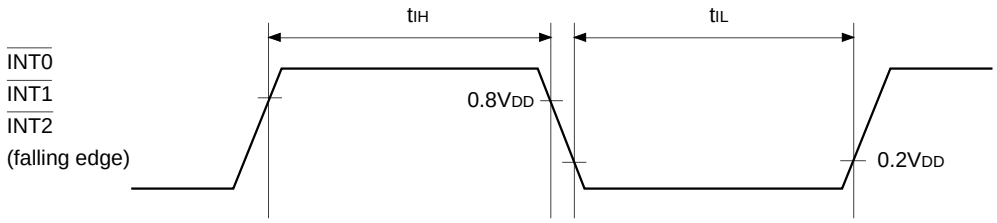


Fig. 6. Interruption input timing

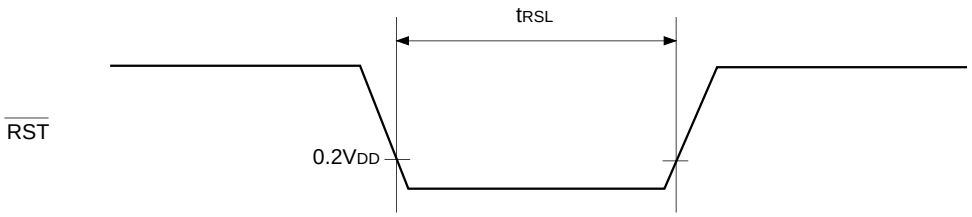


Fig. 7. $\overline{RST}$ input timing

(5) I²C bus timing (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
SCL clock frequency	f_{SLC}	SCL		0	100	kHz
Bus-free time before starting transfer	t_{BUF}	SDA, SCL		4.7		µs
Hold time for starting transfer	$t_{HD;\,STA}$	SDA, SCL		4.0		µs
Clock Low level width	t_{LOW}	SCL		4.7		µs
Clock High level width	t_{HIGH}	SCL		4.0		µs
Setup time for repeated transfers	$t_{SU;\,STA}$	SDA, SCL		4.7		µs
Data hold time	$t_{HD;\,DAT}$	SDA, SCL		0*1		µs
Data setup time	$t_{SU;\,DAT}$	SDA, SCL		250		ns
SDA, SCL rise time	t_R	SDA, SCL			1	µs
SDA, SCL fall time	t_F	SDA, SCL			300	ns
Setup time for transfer completion	$t_{SU;\,STO}$	SDA, SCL		4.7		µs

*1 The data hold time should be 300ns or more because the SCL rise time (300ns Max.) is not included in it.

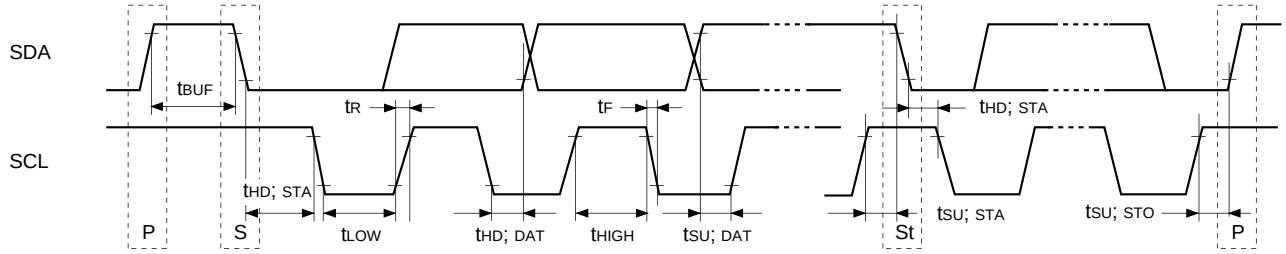


Fig. 8. I²C bus transfer timing

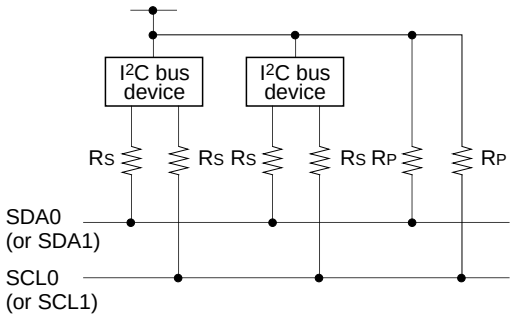


Fig. 9. I²C bus device recommended circuit

- A pull-up resistor (Rp) must be connected to SDA0 (or SDA1) and SCL0 (or SCL1).
- The SDA0 (or SDA1) and SCL0 (or SCL1) series resistance (Rs = 300Ω or less) can be used to reduce the spike noise caused by CRT flashover.

(6) OSD timing (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max	Unit
OSD clock frequency	f_{OSC}	EXLC XLC	Fig. 11	4	40.8	MHz
HSYNC pulse width	t_{HWD}	HSYNC	Fig. 10	30/fc		µs
VSYNC pulse width	t_{VWD}	VSYNC	Fig. 10	1		H*2
HSYNC afterwrite rise and fall times	t_{HCG}	HSYNC	Fig. 10		200	ns
VSYNC beforewrite rise and fall times	t_{VCG}	VSYNC	Fig. 10		1.0	µs

*1 The maximum value of fosc is specified with the following equation.

$fosc\ [max] \leq fc \times 1.7$

*2 H indicates 1HSYNC period.

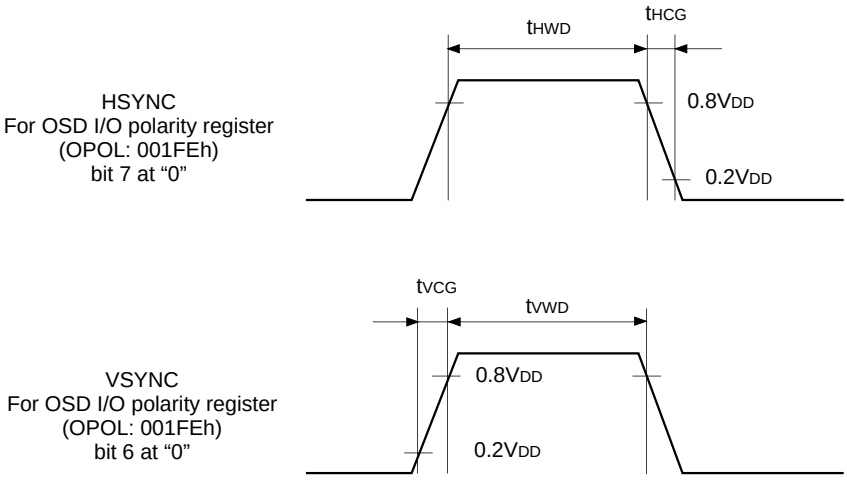


Fig. 10. OSD timing

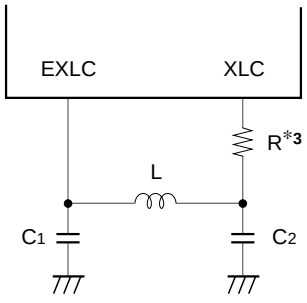


Fig. 11. LC oscillation circuit connection

*3 The series resistor for XLC (R = 1kΩ or less) can reduce the frequency of occurrence of the undesired radiation.

Appendix

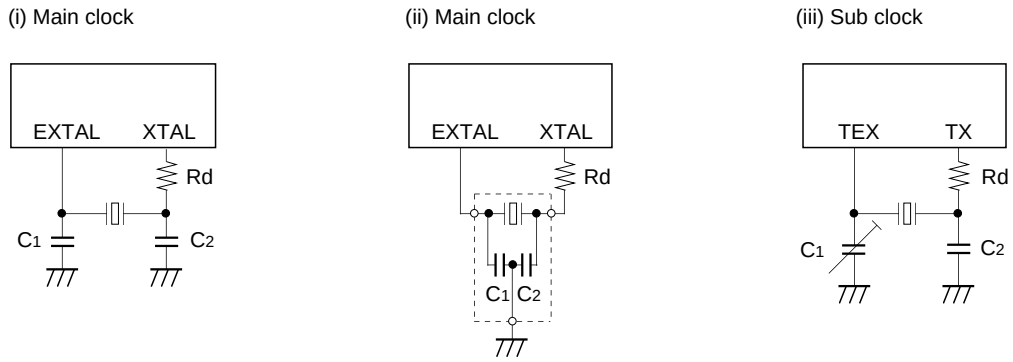


Fig. 12. Recommended oscillation circuit

Manufacture	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example	Remarks
MURATA MFG CO., LTD.	CSA10.0MTZ	10.0	30	30	0 *1	(i)	
	CSA12.0MTZ	12.0					
	CSA16.00MXZ040	16.0	5	5			
	CSA24.00MXZ040	24.0	OPEN	OPEN			
	CST10.0MTW*	10.0	30	30		(ii)	
	CST12.0MTW*	12.0					
	CST16.00MXW0C1*	16.0	5	5			
RIVER ELETEC CO., LTD.	HC-49/U03	8.0	18	18	330 *1	(i)	
		12.0	12	12			
		16.0	10	10			
KINSEKI LTD.	HC-49/U (-S)	8.0	10	10	0 *1		
		12.0	5	5			
		16.0	OPEN	OPEN			
		24.0	3	3			
	P3	32.768kHz	30	33	120k	(iii)	
SEIKO Instruments Inc.	VTC-200 SP-T	32.768kHz	18	18	330k	(iii)	CL = 12.5pF

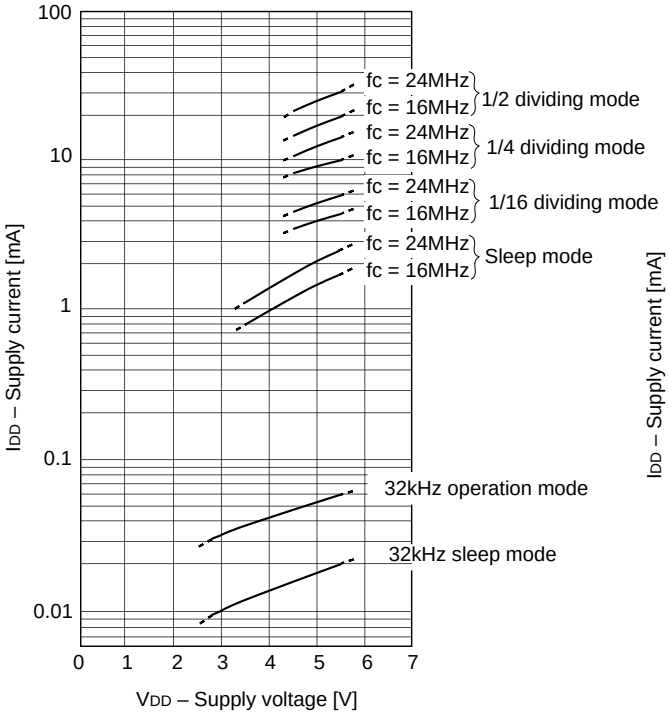
* Models with an astarisk (∗) have the built-in ground capacitance (C_1, C_2).

*1 The series resistor for XTAL (Rd = 500Ω or less) can reduce the effect of the noise caused by the electrostatic discharge.

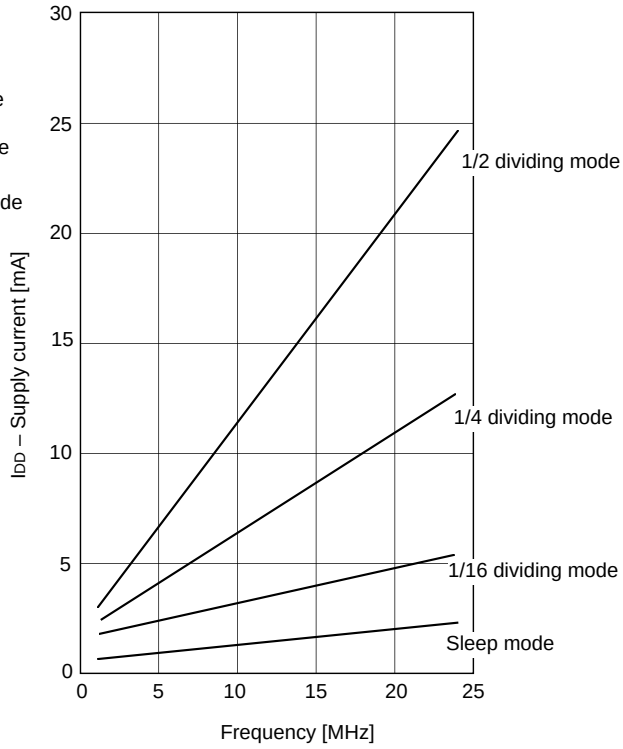
Mask Option Table

Item	Content	
Reset pin pull-up resistor	Non-existent	Existent

IDD vs. VDD
(Ta = 25°C, Typical)



IDD vs. fc
(VDD = 5V, Ta = 25°C, Typical)



Parameter curve for OSD oscillator L vs. C
(Analytically calculated value)

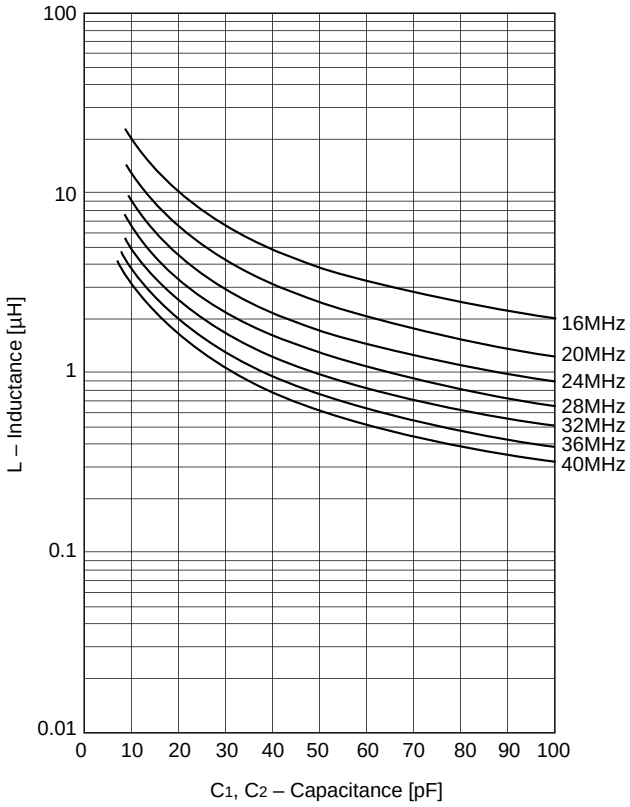
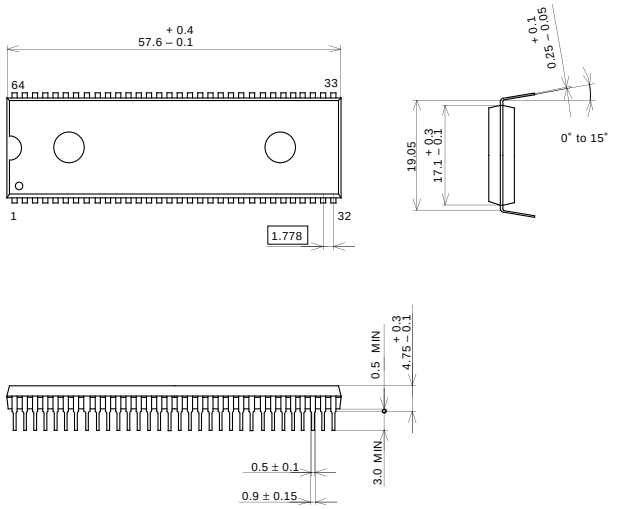


Fig. 13. Characteristic curves

Package Outline Unit: mm

64PIN SDIP (PLASTIC)

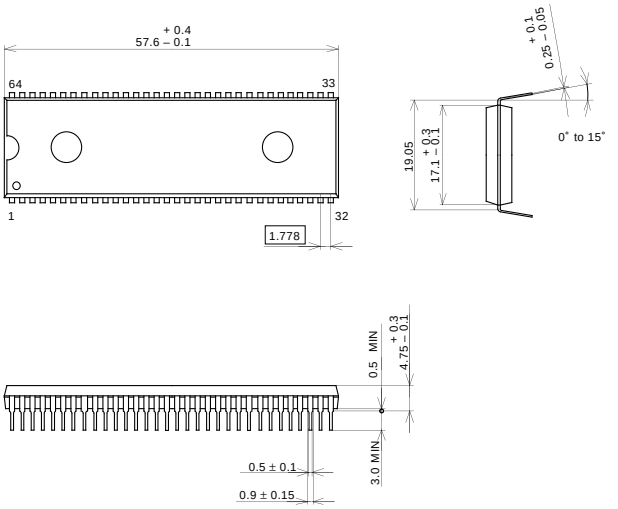


SONY CODE	SDIP-64P-01
EIAJ CODE	P-SDIP64-17.1x57.6-1.778
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	8.6g

64PIN SDIP (PLASTIC)



SONY CODE	SDIP-64P-01
EIAJ CODE	P-SDIP64-17.1x57.6-1.778
JEDEC CODE	

PACKAGE STRUCTURE

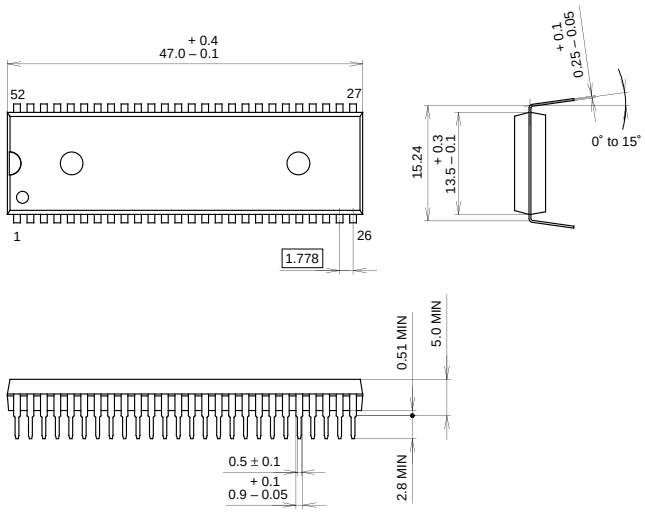
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	8.6g

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18μm

Package Outline Unit: mm

52PIN SDIP (PLASTIC)



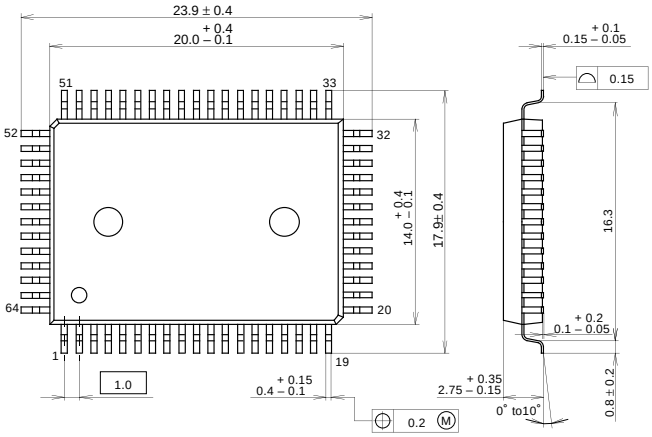
PACKAGE STRUCTURE

SONY CODE	SDIP-52P-01
EIAJ CODE	P-SDIP52-13.5x47.0-1.778
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	5.6g

Package Outline Unit: mm

64PIN QFP (PLASTIC)

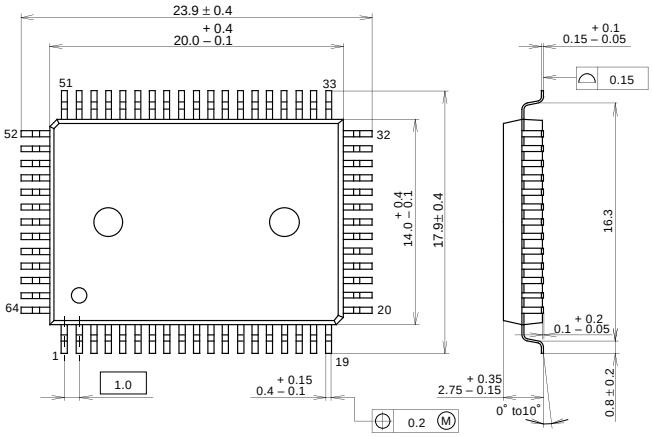


PACKAGE STRUCTURE

SONY CODE	QFP-64P-L01
EIAJ CODE	P-QFP64-14x20-1.0
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g

64PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-64P-L01
EIAJ CODE	P-QFP64-14x20-1.0
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18μm