

GD4013B

DUAL D FLIP-FLOP

DESCRIPTION — The 4013B is a CMOS Dual D Flip-Flop which is edge-triggered and features independent Set Direct, Clear Direct, and Clock inputs. Data is accepted when the Clock is LOW and transferred to the output on the positive-going edge of the Clock. The active HIGH asynchronous Clear Direct (C_D) and Set Direct (S_D) are independent and override the D or Clock inputs. The outputs are buffered for best system performance.

PIN NAMES

D	Data Input
CP	Clock Input (L→H Edge-Triggered)
S_D	Asynchronous Set Direct Input (Active HIGH)
C_D	Asynchronous Clear Direct Input (Active HIGH)
Q	True Output
$\bar{Q}$	Complement Output

4013B TRUTH TABLES

ASYNCHRONOUS INPUTS		OUTPUTS	
S_D	C_D	Q	$\bar{Q}$
L	H	L	H
H	L	H	L
H	H	H	H

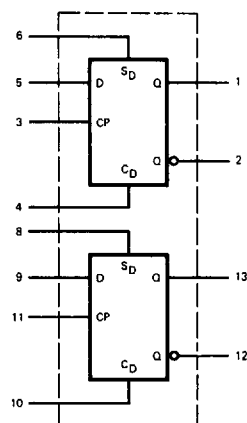
L = LOW Level
H = HIGH Level
↗ = Positive-Going Transition
 Q_{n+1} = State After Clock Positive Transition

SYNCHRONOUS INPUTS		OUTPUTS	
CP	D	Q_{n+1}	$\bar{Q}_{n+1}$
↗	L	L	H
↗	H	H	L

Conditions: $S_D = C_D = \text{LOW}$

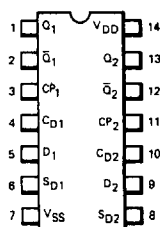
LOGIC SYMBOL

4013B



V_{DD} = Pin 14
 V_{SS} = Pin 7

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The SO Package has the same pinouts (Connection Diagram) as the Dual In-line Package.

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DC CHARACTERISTICS: V_{DD} as shown, $V_{SS} = 0$ V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V _{DD} = 5 V			V _{DD} = 10 V			V _{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I _{DD}	Quiescent Power	XC			4			8			16	μA	MIN, 25°C	All inputs at 0 V or V _{DD}
					30			60			120		MAX	
	Supply Current	XM			1			2			4	μA	MIN, 25°C	
					30			60			120		MAX	

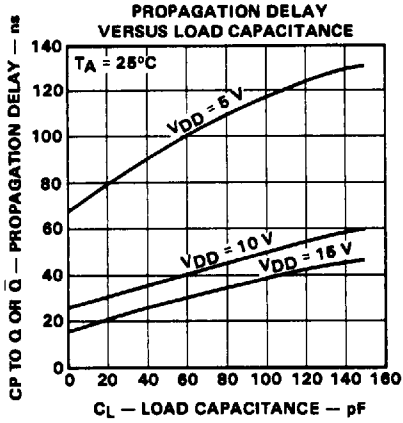
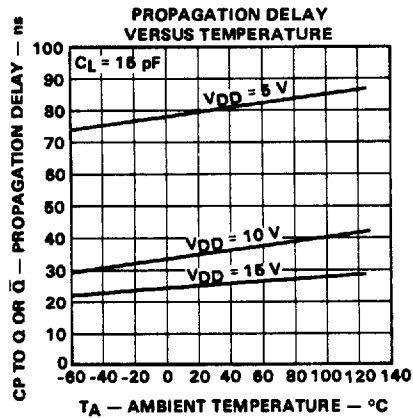
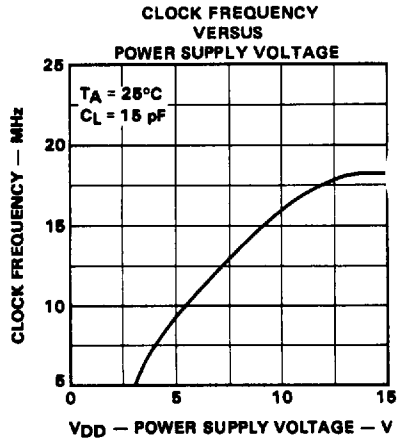
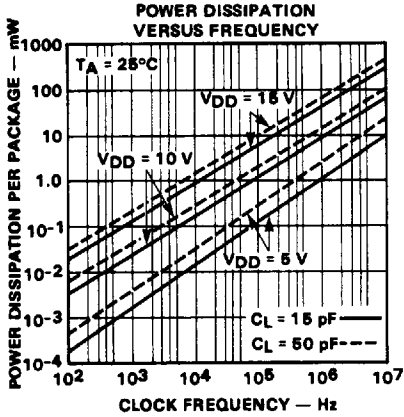
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, $V_{SS} = 0$ V, $T_A = 25^\circ C$ (See Note 3)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V _{DD} = 5 V			V _{DD} = 10 V			V _{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t _{PLH}	Propagation Delay, CP TO Q, $\bar{Q}$		95	200		38	90		29	72	ns	C _L = 50 pF, R _L = 200 kΩ Input Transition Times < 20 ns
t _{PHL}			95	200		38	90		29	72	ns	
t _{PLH}	Propagation Delay, S _D or C _D to $\bar{Q}$		130	225		45	110		32	88	ns	
t _{PHL}			75	225		35	110		20	88	ns	
t _{PLH}	Propagation Delay, S _D or C _D to Q		115	225		50	110		35	88	ns	
t _{PHL}			115	225		50	110		35	88	ns	
t _{TLH}	Output Transition Time		60	135		30	70		20	45	ns	
t _{THL}			60	135		30	70		20	45	ns	
t _s	Set-Up Time, Data to CP	60	30		30	15		24	8		ns	
t _h	Hold Time, Data to CP	0	-25		0	-12		0	-6		ns	
t _{wCP(L)}	Minimum Clock Pulse Width	100	55		55	30		44	18		ns	
t _{wSD(H)}	Minimum S _D Pulse Width	60	30		30	15		24	10		ns	
t _{wCD(H)}	Minimum C _D Pulse Width	60	30		30	15		24	10		ns	
t _{recSD}	Recovery Time for S _D	20	8		10	2		8	2		ns	
t _{recCD}	Recovery Time for C _D	30	15		15	7		12	6		ns	
f _{MAX}	Maximum CP Frequency (Note 2)	5	8		8	16		9	19		MHz	

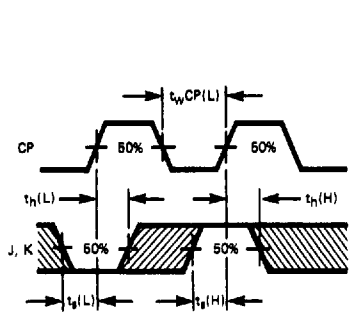
NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. For f_{MAX} Input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
3. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs at $V_{DD} = 5$ V, 4 μs at $V_{DD} = 10$ V, and 3 μs at $V_{DD} = 15$ V.

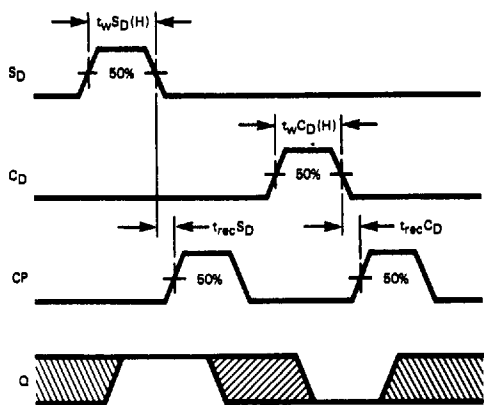
TYPICAL ELECTRICAL CHARACTERISTICS



WAVEFORMS



SET-UP TIMES, HOLD TIMES, AND MINIMUM CLOCK PULSE WIDTH



RECOVERY TIME FOR S_D , RECOVERY TIME FOR C_D , MINIMUM S_D PULSE WIDTH, AND MINIMUM C_D PULSE WIDTH

NOTE: Set-up Times and Hold Times are shown as positive values but may be specified as negative values.