P87LPC779

CMOS single-chip 8-bit 80C51 microcontroller with 128-byte data RAM, 8 kB OTP

Rev. 02 — 03 May 2004 **Product data**

1. General description

The P87LPC779 is a 20-pin single-chip microcontroller designed for low pin count applications demanding high-integration, low cost solutions over a wide range of performance requirements. A member of the Philips low pin count family, the P87LPC779 offers a four channel, 8-bit A/D converter, two DAC outputs, programmable oscillator configurations for high and low speed crystals or RC operation, wide operating voltage range, programmable port output configurations, selectable Schmitt trigger inputs, LED drive outputs, and a built-in Watchdog timer. The P87LPC779 is based on an accelerated 80C51 processor architecture that executes instructions at twice the rate of standard 80C51 devices.

2. Features

- An accelerated 80C51 CPU provides instruction cycle times of 300 ns to 600 ns for all instructions except multiply and divide when executing at 20 MHz.
- 2.7 V to 5.5 V operating range for digital functions.
- Two 8-bit Digital to Analog Converters.
- Four channel, 8-bit Analog to Digital Converter. Conversion time is 9.3 µs with a 20 MHz crystal.
- I^2C-bus communication port and Full duplex UART.
- Internal oscillator 2.5 %. The internal oscillator option allows operation with no external oscillator components.
- Two analog comparators.
- Eight keypad interrupt inputs, plus two additional external interrupt inputs.
- Watchdog timer with separate on-chip oscillator, requiring no external components. The Watchdog time-out time is selectable from eight values.
- 20-pin TSSOP package.

PHILIPS

3. Ordering information

Table 1: Ordering information

Type number	Package			
	Name	Description	Temperature range	Version
P87LPC779FDH	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	–40 °C to +85 °C	SOT360-1

4. Block diagram

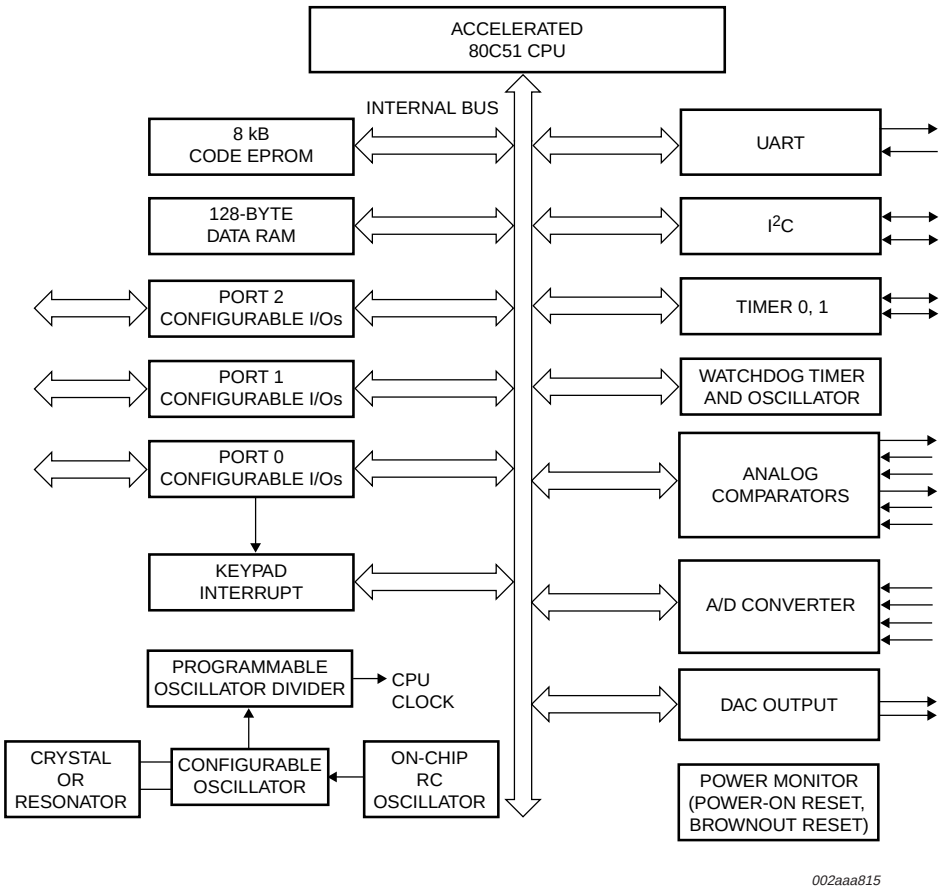
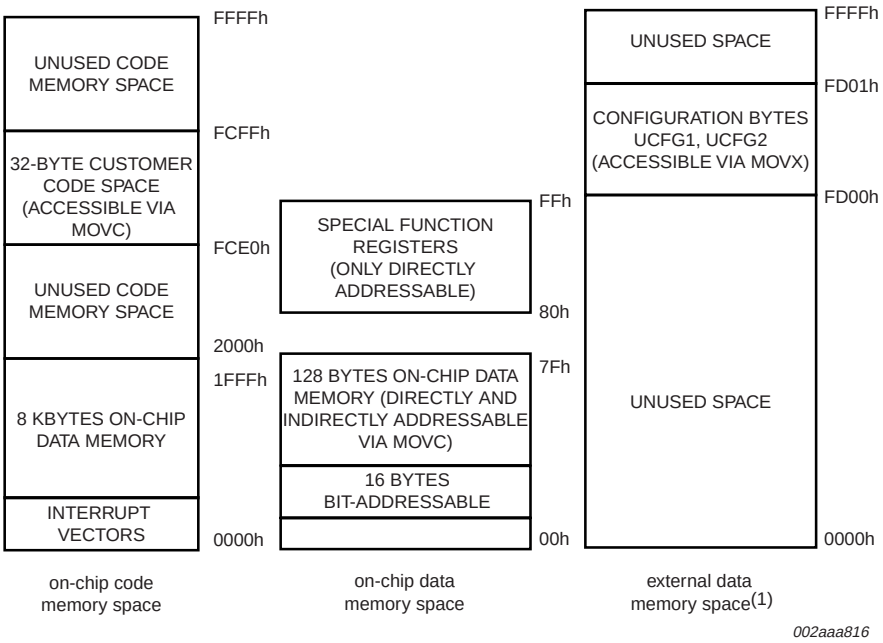


Fig 1. Block diagram.



(1) The P87LPC779 does not support access to external data memory. However, the User Configuration Bytes are accessed via the MOVX instruction as if they were in external data memory.

Fig 2. Memory map.

5. Pinning information

5.1 Pinning

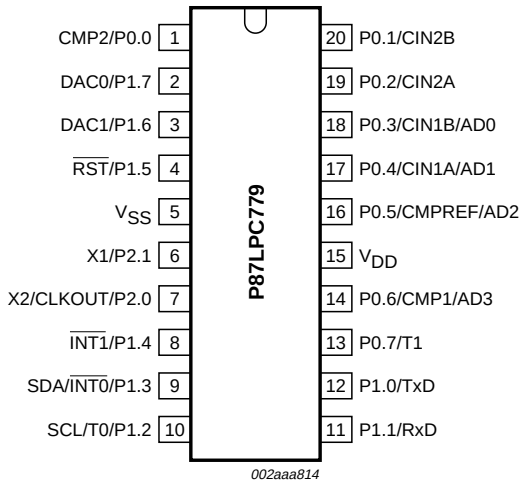


Fig 3. 20 pin DIP and SO configuration.

5.2 Pin description

Table 2: Pin description

Symbol	Pin	Type	Description
P0.0 - P0.7	1, 20-16, 14, 13	I/O	**Port 0:** Port 0 is an 8-bit I/O port with a user-configurable output type. Port 0 latches are configured in the quasi-bidirectional mode and have either ones or zeros written to them during reset, as determined by the PRHI bit in the UCFG1 configuration byte. The operation of port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.9 “I/O ports” and Table 55 “DC electrical characteristics” for details. The Keypad Interrupt feature operates with Port 0 pins. Port 0 also provides various special functions as described below:
P0.0	1	O	**CMP2 —** Comparator 2 output.
P0.1	20	I	**CIN2B —** Comparator 2 positive input B.
P0.2	19	I	**CIN2A —** Comparator 2 positive input A.
P0.3	18	I	**CIN1B —** Comparator 1 positive input B.
		I	**AD0 —** A/D channel 0 input.
P0.4	17	I	**CIN1A —** Comparator 1 positive input A.
		I	**AD1 —** A/D channel 1 input.
P0.5	16	I	**CMPREF —** Comparator reference (negative) input.
		I	**AD2 —** A/D channel 2 input.
P0.6	14	O	**CMP1 —** Comparator 1 output.
		I	**AD3 —** A/D channel 3 input.
P0.7	13	I/O	**T1 —** Timer/counter 1 external count input or overflow output.

Table 2: Pin description...*continued*

Symbol	Pin	Type	Description
P1.0 - P1.7	12-8, 4, 3, 2	I/O	**Port 1:** Port 1 is an 8-bit I/O port with a user-configurable output type, except for three pins as noted below. Port 1 latches are configured in the quasi-bidirectional mode and have either ones or zeros written to them during reset, as determined by the PRHI bit in the UCFG1 configuration byte. The operation of the configurable port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 8.9 “I/O ports” and Table 55 “DC electrical characteristics” for details. Port 1 also provides various special functions as described below:
P1.0	12	O	**TxD —** Transmitter output for the serial port.
P1.1	11	I	**RxD —** Receiver input for the serial port.
P1.2	10	I/O	**T0 —** Timer/counter 0 external count input or overflow output.
		I/O	**SCL —** I^2C-bus serial clock input/output. When configured as an output, P1.2 is open drain, in order to conform to I^2C-bus specifications.
P1.3	9	I	**$\overline{\text{INT0}}$ —** External interrupt 0 input.
		I/O	**SDA —** I^2C-bus serial data input/output. When configured as an output, P1.3 is open drain, in order to conform to I^2C-bus specifications.
P1.4	8	I	**$\overline{\text{INT1}}$ —** External interrupt 1 input.
P1.5	4	I	**$\overline{\text{RST}}$ —** External Reset input (if selected via EPROM configuration). A LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. When used as a port pin, P1.5 is a Schmitt trigger input only.
P1.6	3	O	**DAC1 —** Output from Digital to Analog Converter 1.
P1.7	2	O	**DAC0 —** Output from Digital to Analog Converter 0.
P2.0 - P2.1	7, 6	I/O	**Port 2:** Port 2 is a 2-bit I/O port with a user-configurable output type. Port 2 latches are configured in the quasi-bidirectional mode and have either ones or zeros written to them during reset, as determined by the PRHI bit in the UCFG1 configuration byte. The operation of port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.9 “I/O ports” and Table 55 “DC electrical characteristics” for details. Port 2 also provides various special functions as described below:
P2.0	7	O	**X2 —** Output from the oscillator amplifier (when a crystal oscillator option is selected via the EPROM configuration.
		O	**CLKOUT —** CPU clock divided by 6 clock output when enabled via SFR bit and in conjunction with internal RC oscillator or external clock input.
P2.1	6	I	**X1 —** Input to the oscillator circuit and internal clock generator circuits (when selected via the EPROM configuration).
V_{SS}	5	I	**Ground:** 0 V reference.
V_{DD}	15	I	**Power Supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.

6. Logic symbol

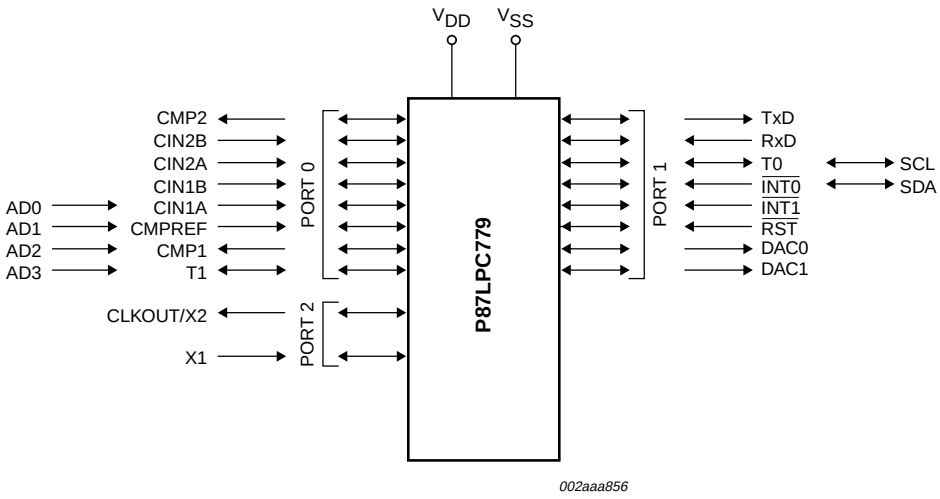


Fig 4. Logic symbol.

7. Special function registers

Remark: Special Function Registers (SFRs) accesses are restricted in the following ways:

- User must **not** attempt to access any SFR locations not defined.
- Accesses to any defined SFR locations must be strictly for the functions for the SFRs.
- SFR bits labeled '-', '0' or '1' can **only** be written and read as follows:
  - '-' Unless otherwise specified, **must** be written with '0', but can return any value when read (even if it was written with '0'). It is a reserved bit and may be used in future derivatives.
  - '0' **must** be written with '0', and will return a '0' when read.
  - '1' **must** be written with '1', and will return a '1' when read.

Table 3: Special function registers

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value
			MSB							LSB	Hex
		Bit address	E7	E6	E5	E4	E3	E2	E1	E0	
ACC*	Accumulator	E0H									00H
		Bit address	C7	C6	C5	C4	C3	C2	C1	C0	
ADCON*	A/D Control	C0h	ENADC			ADCI	ADCS	RCCLK	AADR1	AADR0	02h
AUXR1	Auxiliary Function Register	A2h	KBF	BOD	BOI	LPEP	SRST	0	-	DPS	02h
		Bit address	F7	F6	F5	F4	F3	F2	F1	F0	
B*	B register	F0h									00H
CMP1	Comparator 1 control register	ACh	-	-	CE1	CP1	CN1	OE1	CO1	CMF1	00H
CMP2	Comparator 2 control register	ADh	-	-	CE2	CP2	CN2	OE2	CO2	CMF2	00H
DAC0	A/D Result / Read DAC0 output value / Write	C5h									00H
DAC1	DAC1 output value	C6h									00H
DIVM	CPU clock divide-by-M control	95h									00H
DPTR	Data pointer (2 bytes)										
DPH	Data pointer HIGH	83h									00H
DPL	Data pointer LOW	82h									00H
		Bit address	CF	CE	CD	CC	CB	CA	C9	C8	
I2CFG*	I^2C-bus configuration register	C8h/RD	SLAVEN	MASTRQ	0	TIRUN	-	-	CT1	CT0	00H
		C8h/WR	SLAVEN	MASTRQ	CLRTI	TIRUN	-	-	CT1	CT0	
		Bit address	DF	DE	DD	DC	DB	DA	D9	D8	
I2CON*	I^2C-bus control register	D8h/RD	RDAT	ATN	DRDY	ARL	STR	STP	MASTER	-	80h
		D8h/WR	CXA	IDLE	CDR	CARL	CSTR	CSTP	XSTR	XSTP	
I2DAT	I^2C-bus data register	D9h/RD	RDAT	0	0	0	0	0	0	0	80h
		D9h/WR	XDAT	x	x	x	x	x	x	x	
		Bit address	AF	AE	AD	AC	AB	AA	A9	A8	
IEN0*	Interrupt enable 0	A8h	EA	EWD	EBO	ES	ET1	EX1	ET0	EX0	00H
		Bit address	EF	EE	ED	EC	EB	EA	E9	E8	
IEN1*	Interrupt enable 1	E8h	ETI	-	EC1	EAD	-	EC2	EKB	EI2	00H

9397 750 13213

Table 3: Special function registers...*continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value
			MSB							LSB	Hex
		Bit address	BF	BE	BD	BC	BB	BA	B9	B8	
IP0*	Interrupt priority 0	B8h	-	PWD	PBO	PS	PT1	PX1	PT0	PX0	00H
IP0H	Interrupt priority 0 HIGH	B7h	-	PWDH	PBOH	PSH	PT1H	PX1H	PT0H	PX0H	00H
		Bit address	FF	FE	FD	FC	FB	FA	F9	F8	
IP1*	Interrupt priority 1	F8h	PTI	-	PC1	PAD	-	PC2	PKB	PI2	00H
IP1H	Interrupt priority 1 HIGH	F7h	PTIH	-	PC1H	PADH	-	PC2H	PKBH	PI2H	00H
KBI	Keyboard Interrupt	86h									00H
		Bit address	87	86	85	84	83	82	81	80	
P0*	Port 0	80h	T1	CMP1	CMPREF	CIN1A	CIN1B	CIN2A	CIN2B	CMP2	[1]
		Bit address	97	96	95	94	93	92	91	90	
P1*	Port 1	90h	DAC0	DAC1	$\overline{\text{RST}}$	INT1	INT0	T0	RxD	TxD	[1]
		Bit address	A7	A6	A5	A4	A3	A2	A1	A0	
P2*	Port 2	A0h	-	-	-	-	-	-	X1	X2	[1]
P0M1	Port 0 output mode 1	84h	(P0M1.7)	(P0M1.6)	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	(P0M1.0)	00H
P0M2	Port 0 output mode 2	85h	(P0M2.7)	(P0M2.6)	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	(P0M2.0)	00H
P1M1	Port 1 output mode 1	91h	(P1M1.7)	(P1M1.6)	-	(P1M1.4)	-	-	(P1M1.1)	(P1M1.0)	00H
P1M2	Port 1 output mode 2	92h	(P1M2.7)	(P1M2.6)	-	(P1M2.4)	-	-	(P1M2.1)	(P1M2.0)	00H
P2M1	Port 2 output mode 1	A4h	P2S	P1S	P0S	ENCLK	ENT1	ENT0	(P2M1.1)	(P2M1.0)	00H
P2M2	Port 2 output mode 2	A5h	-	-	-	-	-	-	(P2M2.1)	(P2M2.0)	00H
PCON	Power control register	87h	SMOD1	SMOD0	BOF	POF	GF1	GF0	PD	IDL	[2]
		Bit address	D7	D6	D5	D4	D3	D2	D1	D0	
PSW*	Program status word	D0h	CY	AC	F0	RS1	RS0	OV	F1	P	00H
PT0AD	Port 0 digital input disable	F6h									00H
		Bit address	9F	9E	9D	9C	9B	9A	99	98	
SCON*	Serial port control	98h	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00H
SBUF	Serial port data buffer register	99h									xxh
SADDR	Serial port address register	A9h									00H
SADEN	Serial port address enable	B9h									00H

Table 3: Special function registers...*continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value
			MSB							LSB	Hex
SP	Stack pointer	81h									07h
		Bit address	8F	8E	8D	8C	8B	8A	89	88	
TCON*	Timer0 and 1 control	88h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
TH0	Timer0 HIGH	8Ch									00H
TH1	Timer1 HIGH	8Dh									00H
TL0	Timer0 LOW	8Ah									00H
TL1	Timer1 LOW	8Bh									00H
TMOD	Timer0 and 1 mode	89h	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00H
WDCON	Watchdog control register	A7h	-	-	WDOVF	WDRUN	WDCLK	WDS2	WDS1	WDS0	[3]
WDRST	Watchdog reset register	A6h									xxh

[1] I/O port values at reset are determined by the PRHI bit in the UCFG1 configuration byte.

[2] The PCON reset value is xxBOF POF - 0000b. The BOF and POF flags are not affected by reset. The POF flag is set by hardware upon power up. The BOF flag is set by the occurrence of a brownout reset/interrupt and upon power up.

[3] The WDCON reset value is xx11 0000b for a Watchdog reset, xx01 0000b for all other reset causes if the Watchdog is enabled, and xx00 0000b for all other reset causes if the Watchdog is disabled.

8. Functional description

Remark: Please refer to the *P87LPC779 User's Manual* for a more detailed functional description.

8.1 Enhanced CPU

The P87LPC779 uses an enhanced 80C51 CPU which runs at twice the speed of standard 80C51 devices. This means that the performance of the P87LPC779 running at 5 MHz is exactly the same as that of a standard 80C51 running at 10 MHz. A machine cycle consists of 6 oscillator cycles, and most instructions execute in 6 or 12 clocks. A user configurable option allows restoring standard 80C51 execution timing. In that case, a machine cycle becomes 12 oscillator cycles.

In the following sections, the term 'CPU clock' is used to refer to the clock that controls internal instruction execution. This may sometimes be different from the externally applied clock, as in the case where the part is configured for standard 80C51 timing by means of the CLKR configuration bit or in the case where the clock is divided down via the setting of the DIVM register. These features are described in the Section 8.10 "Oscillator" on page 34.

8.2 Analog functions

The P87LPC779 incorporates analog peripheral functions: an ADC, two Analog Comparators, and two DACs. In order to give the best analog function performance and to minimize power consumption, pins that are actually being used for analog functions must have the digital outputs (except for the DAC output pins) and the digital inputs must also be disabled.

Digital outputs are disabled by putting the port output into the Input Only (high impedance) mode as described in the Section 8.9 "I/O ports" on page 29.

Digital inputs on port 0 may be disabled through the use of the PT0AD register. Each bit in this register corresponds to one pin of Port 0. Setting the corresponding bit in PT0AD disables that pin's digital input. Port bits that have their digital inputs disabled will be read as '0' by any instruction that accesses the port.

8.3 Analog to digital converter

The P87LPC779 incorporates a four channel, 8-bit A/D converter. The A/D inputs are alternate functions on four port 0 pins. Because the device has a very limited number of pins, the A/D power supply and references are shared with the processor power pins, V_{DD} and V_{SS}. The A/D converter operates down to a V_{DD} supply of 3.0 V.

The A/D converter circuitry consists of a 4-input analog multiplexer and an 8-bit successive approximation ADC. The A/D employs a ratiometric potentiometer which guarantees DAC monotonicity.

The A/D converter is controlled by the special function register ADCON. Details of ADCON are shown in Tables 4 and 5. The A/D must be enabled by setting the ENADC bit at least 10 microseconds before a conversion is started, to allow time for

the A/D to stabilize. Prior to the beginning of an A/D conversion, one analog input pin must be selected for conversion via the AADR1 and AADR0 bits. These bits cannot be changed while the A/D is performing a conversion.

An A/D conversion is started by setting the ADCS bit, which remains set while the conversion is in progress. When the conversion is complete, the ADCS bit is cleared and the ADCI bit is set. When ADCI is set, it will generate an interrupt if the interrupt system is enabled, the A/D interrupt is enabled (via the EAD bit in the IE1 register), and the A/D interrupt is the highest priority pending interrupt.

When a conversion is complete, the result is contained in the register DAC0 and can be read to get the ADC result. This value will not change until another conversion is started. Before another A/D conversion may be started, the ADCI bit must be cleared by software. The A/D channel selection may be changed by the same instruction that sets ADCS to start a new conversion, but not by the same instruction that clears ADCI.

The connections of the A/D converter are shown in Figure 5.

The ideal A/D result may be calculated as follows:

$$\text{Result} = (V_{IN} - V_{SS}) \times \frac{256}{V_{DD} - V_{SS}} (\text{round result to the nearest integer}) \quad (1)$$

Table 4: ADCON - A/D control register (address C0h) bit allocation

Bit addressable; Reset value: 00H

Bit	7	6	5	4	3	2	1	0
Symbol	ENADC	DAC1	DAC0	ADCI	ADCS	RCCLK	AADR1	AADR0

Table 5: ADCON - A/D control register (address C0h) bit description

Bit	Symbol	Description
7	ENADC	When ENADC = 1, the A/D is enabled and conversions may take place. Must be set 10 microseconds before a conversion is started. ENADC cannot be cleared while ADCS or ADCI are ‘1’.
6	DAC1	When ENDAC1 = 1, DAC1 is enabled to provide an analog output voltage. Refer to Section 8.5 “Digital to Analog Converter (DAC) outputs” on page 17.
5	DAC0	When ENDAC1 = 0, DAC0 is enabled to provide an analog output voltage. Writable while ADCS and ADCI are ‘0’. Refer to Section 8.5 “Digital to Analog Converter (DAC) outputs” on page 17 for more detail. ENADC and ENDAC0 should not be set at the same time.

Table 5: ADCON - A/D control register (address C0h) bit description *...continued*

Bit	Symbol	Description
4	ADCI	A/D conversion complete/interrupt flag. This flag is set when an A/D conversion is completed. This bit will cause a hardware interrupt if enabled and of sufficient priority. Must be cleared by software.
3	ADCS	A/D start. Setting this bit by software starts the conversion of the selected A/D input. ADCS remains set while the A/D conversion is in progress and is cleared automatically upon completion. While ADCS or ADCI are one, new start commands are ignored. See Table 6.
2	RCCLK	When RCCLK = 0, the CPU clock is used as the A/D clock. When RCCLK = 1, the internal RC oscillator is used as the A/D clock. This bit is writable while ADCS and ADCI are 0.
1, 0	AADR1, 0	Along with AADR0, selects the A/D channel to be converted. These bits can only be written while ADCS and ADCI are 0. See Table 7.

Table 6: ADCON - ADCI, ADCS A/D status

ADCI, ADCS	A/D status
0 0	A/D not busy, a conversion can be started
0 1	A/D busy, the start of a new conversion is blocked.
1 0	An A/D conversion is complete. ADCI must be cleared prior to starting a new conversion.
1 1	An A/D conversion is complete. ADCI must be cleared prior to starting a new conversion. This state exists for one machine cycle as an A/D conversion is completed.

Table 7: ADCON - AADR1, AADR0 A/D input selection

AADR1, AADR0	A/D input selected
0 0	AD0 (P0.3)
0 1	AD1 (P0.4)

8.4 A/D timing

The A/D may be clocked in one of two ways. The default is to use the CPU clock as the A/D clock source. When used in this manner, the A/D completes a conversion in 31 machine cycles. The A/D may be operated up to the maximum CPU clock rate of 20 MHz, giving a conversion time of 9.3 µs. The formula for calculating A/D conversion time when the CPU clock runs the A/D is: 186 µs / CPU clock rate (in MHz). To obtain accurate A/D conversion results, the CPU clock must be at least 1 MHz.

The A/D may also be clocked by the on-chip RC oscillator, even if the RC oscillator is not used as the CPU clock. This is accomplished by setting the RCCLK bit in ADCON. This arrangement has several advantages. First, the A/D conversion time is faster at lower CPU clock rates. Also, the CPU may be run at speeds below 1 MHz without affecting A/D accuracy. Finally, the Power-down mode may be used to completely shut down the CPU and its oscillator, along with other peripheral functions, in order to obtain the best possible A/D accuracy.

When the A/D is operated from the RCCLK while the CPU is running from another clock source, 3 or 4 machine cycles are used to synchronize A/D operation. The time can range from a minimum of 3 machine cycles (at the CPU clock rate) + 108 RC clocks to a maximum of 4 machine cycles (at the CPU clock rate) + 112 RC clocks.

Example A/D conversion times at various CPU clock rates are shown in Table 8. In the table, maximum times for RCCLK = 1 use an RC clock frequency of 6 MHz. Minimum times for RCCLK = 1 use an RC clock frequency of. Nominal time assume an ideal RC clock frequency of 6 MHz and an average of 3.5 machine cycles at the CPU clock rate.

Table 8: Example A/D conversion times

CPU clock rate	RCCLK = 0	RCCLK = 1		
		minimum	nominal	maximum
32 kHz	NA	563.4 µs	659 µs	757 µs
1 MHz	186 µs	32.4 µs	39.3 µs	48.9 µs
4 MHz	46.5 µs	18.9 µs	23.6 µs	30.1 µs
11.0592 MHz	16.8 µs	16 µs	20.2 µs	27.1 µs
12 MHz	15.5 µs	15.9 µs	20.1 µs	26.9 µs
16 MHz	11.6 µs	15.5 µs	19.7 µs	26.4 µs
20 MHz	9.3 µs	15.3 µs	19.4 µs	26.1 µs

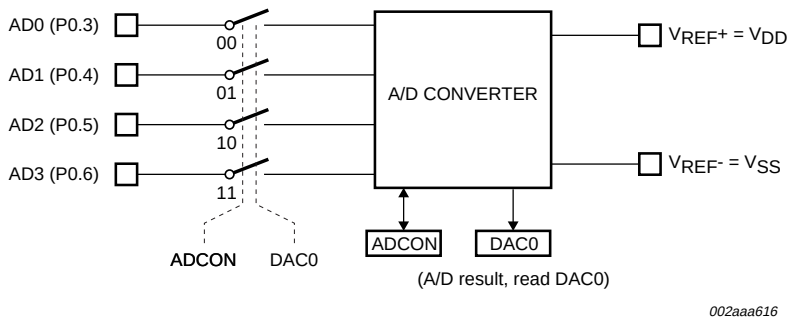


Fig 5. A/D converter connections.

8.4.1 The A/D in Power-down and Idle modes

While using the CPU clock as the A/D clock source, the Idle mode may be used to conserve power and/or to minimize system noise during the conversion. CPU operation will resume and Idle mode terminate automatically when a conversion is complete if the A/D interrupt is active. In Idle mode, noise from the CPU itself is eliminated, but noise from the oscillator and any other on-chip peripherals that are running will remain.

The CPU may be put into Power-down mode when the A/D is clocked by the on-chip RC oscillator (RCCLK = 1). This mode gives the best possible A/D accuracy by eliminating most on-chip noise sources.

If the Power-down mode is entered while the A/D is running from the CPU clock (RCCLK = 0), the A/D will abort operation and will not wake up the CPU. The contents of DAC0 will be invalid when operation does resume.

When an A/D conversion is started, Power-down or Idle mode must be activated within two machine cycles in order to have the most accurate A/D result. These two machine cycles are counted at the CPU clock rate. When using the A/D with either Power-down or Idle mode, care must be taken to insure that the CPU is not restarted by another interrupt until the A/D conversion is complete. The possible causes of wake-up are different in Power-down and Idle modes.

A/D accuracy is also affected by noise generated elsewhere in the application, power supply noise, and power supply regulation. Since the P87LPC779 power pins are also used as the A/D reference and supply, the power supply has a very direct affect on the accuracy of A/D readings. Using the A/D without Power-down mode while the clock is divided through the use of CLKR or DIVM has an adverse effect on A/D accuracy.

8.4.2 Code examples for the A/D

The first piece of sample code shows an example of port configuration for use with the A/D. This example sets up the pins so that all four A/D channels may be used. Port configuration for analog functions is described in Section 8.2 “Analog functions” on page 12.

```
; Set up port pins for A/D conversion, without affecting other pins.
   mov   PT0AD,#78h  ; Disable digital inputs on A/D input pins.
   anl   P0M2,#87h   ; Disable digital outputs on A/D input pins.
   orl   P0M1,#78h   ; Disable digital outputs on A/D input pins.
```

Following is an example of using the A/D with interrupts. The routine ADStart begins an A/D conversion using the A/D channel number supplied in the accumulator. The channel number is not checked for validity. The A/D must previously have been enabled with sufficient time to allow for stabilization.

The interrupt handler routine reads the conversion value and returns it in memory address ADResult. The interrupt should be enabled prior to starting the conversion.

```
; Start A/D conversion.
ADStart:
  orl   ADCON,A    ; Add in the new channel number.
  setb  ADCS       ; Start an A/D conversion.
; orl   PCON,#01h  ; The CPU could be put into Idle mode here.
; orl   PCON,#02h  ; The CPU could be put into Power-down mode here if
RCCLK = 1.
  ret
; A/D interrupt handler.
ADInt:
 push  ACC         ; Save accumulator.
 mov   A,DAC0      ; Get A/D result, by reading DAC0 SFR
 mov   ADResult,A  ; and save it in memory.
 clr   ADCI        ; Clear the A/D completion flag.
 anl   ADCON,#0fch ; Clear the A/D channel number.
 pop   ACC         ; Restore accumulator.
 ret
```

Following is an example of using the A/D with polling. An A/D conversion is started using the channel number supplied in the accumulator. The channel number is not checked for validity. The A/D must previously have been enabled with sufficient time to allow for stabilization. The conversion result is returned in the accumulator.

```
ADRead:
 orl  ADCON,A      ; Add in the new channel number.
 setb ADCS         ; Start A/D conversion.
ADChk:
 jnb  ADCI,ADChk   ; Wait for ADCI to be set.
 mov  A,DAC0       ; Get A/D result.
 clr  ADCI         ; Clear the A/D completion flag.
 anl  ADCON,#0fch  ; Clear the A/D channel number.
 ret
```

8.5 Digital to Analog Converter (DAC) outputs

The P87LPC779 provides a two channel, 8-bit DAC function. DAC0 is also part of the A/D Converter and is should not be enabled while the A/D is active. The DAC outputs function down to a V_{DD} of 3.0 V. Digital outputs must be disabled on the DAC output pins while the corresponding DAC is enabled, as described in Section 8.2 “Analog functions” on page 12.

The DACs use the power supply as the references: V_{DD} as the upper reference and VSS as the lower reference. The DAC output is generated by a tap from a resistor ladder and is not buffered. The maximum resistance to V_{DD} or V_{SS} from a DAC output is 10 kΩ. Care must be taken with the loading of the DAC outputs in order to avoid distortion of the output voltage. DAC accuracy is affected by noise generated on-chip and elsewhere in the application. Since the P87LPC779 power pins are used for the DAC references, the power supply also affects the accuracy of the DAC outputs.

The ideal DAC output may be calculated as follows:

$$\text{Result} = (\text{DAC value} + 0.5) \times \frac{V_{DD} - V_{SS}}{256} \quad (2)$$

where DAC Value is the contents of the relevant DAC register: DAC0 or DAC1.

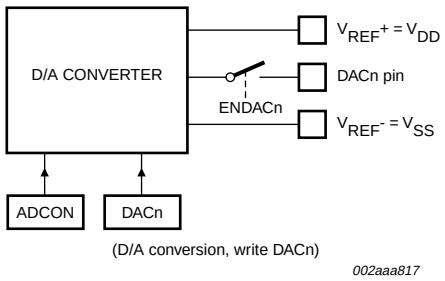


Fig 6. DAC block diagram.

8.6 Analog comparators

Two analog comparators are provided on the P87LPC779. Input and output options allow use of the comparators in a number of different configurations. Comparator operation is such that the output is a logic 1 (which may be read in a register and/or routed to a pin) when the positive input (one of two selectable pins) is greater than the

negative input (selectable from a pin or an internal reference voltage). Otherwise the output is a zero. Each comparator may be configured to cause an interrupt when the output value changes.

8.6.1 Comparator configuration

Each comparator has a control register, CMP1 for comparator 1 and CMP2 for comparator 2. The control registers are identical and are shown in Tables 9 and 10.

The overall connections to both comparators are shown in Figure 7. There are eight possible configurations for each comparator, as determined by the control bits in the corresponding CMPn register: CPn, CNn, and OEn. These configurations are shown in Figure 8. The comparators function down to a V_{DD} of 3.0 V.

When each comparator is first enabled, the comparator output and interrupt flag are not guaranteed to be stable for 10 μs. The corresponding comparator interrupt should not be enabled during that time, and the comparator interrupt flag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service.

Table 9: CMPn - Comparator control registers CMP1 and CMP2 (address ACh for CMP1, ADh for CMP2) bit allocation

Not bit addressable; Reset value: 00H

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	CEn	CPn	CNn	OEn	COn	CMFn

Table 10: CMPn - Comparator control registers CMP1 and CMP2 (address ACh for CMP1, ADh for CMP2) bit description

Bit	Symbol	Description
7, 6	-	Reserved for future use. Should not be set to ‘1’ by user programs.
5	CEn	Comparator enable. When set by software, the corresponding comparator function is enabled. Comparator output is stable 10 μs after CEn is first set.
4	CPn	Comparator positive input select. When ‘0’, CINnA is selected as the positive comparator input. When ‘1’, CINnB is selected as the positive comparator input.
3	CNn	Comparator negative input select. When ‘0’, the comparator reference pin CMPREF is selected as the negative comparator input. When ‘1’, the internal comparator reference Vref is selected as the negative comparator input.
2	OEn	Output enable. When ‘1’, the comparator output is connected to the CMPn pin if the comparator is enabled (CEn = 1). This output is asynchronous to the CPU clock.
1	COn	Comparator output, synchronized to the CPU clock to allow reading by software. Cleared when the comparator is disabled (CEn = 0).
0	CMFn	Comparator interrupt flag. This bit is set by hardware whenever the comparator output COn changes state. This bit will cause a hardware interrupt if enabled and of sufficient priority. Cleared by software and when the comparator is disabled (CEn = 0).

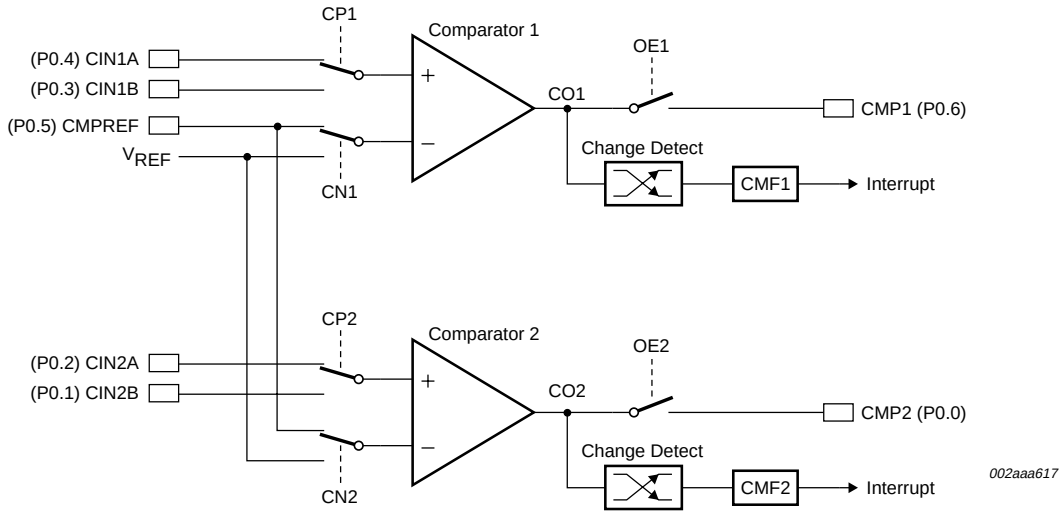


Fig 7. Comparator input and output connections.

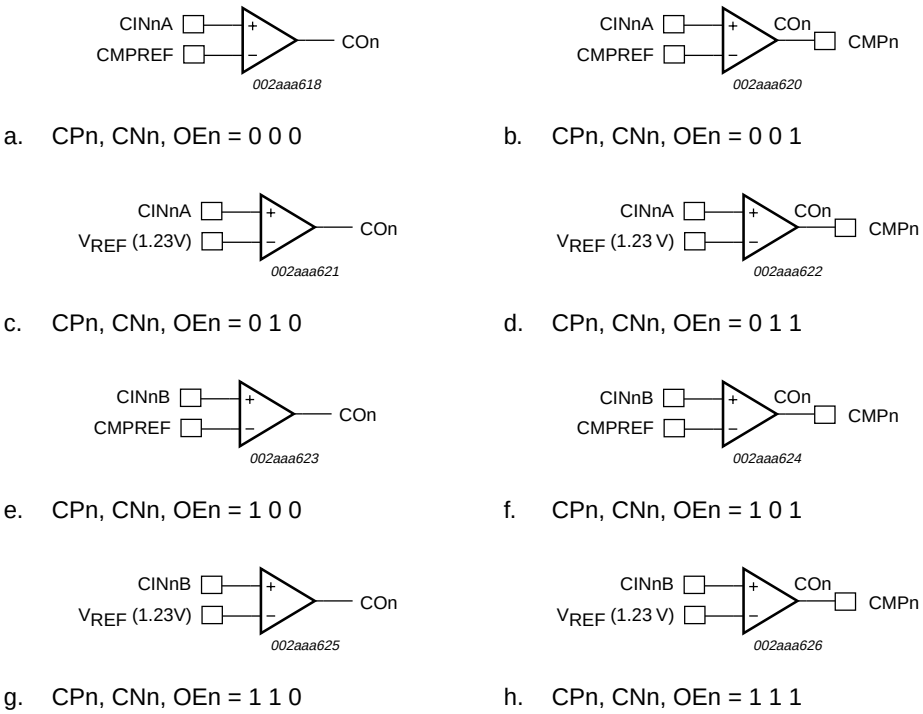


Fig 8. Comparator configurations.

8.6.2 Internal reference voltage

An internal reference voltage generator may supply a default reference when a single comparator input pin is used. The value of the internal reference voltage, referred to as Vref, is 1.28 V ±10 %.

8.6.3 Comparator interrupt

Each comparator has an interrupt flag CMFn contained in its configuration register. This flag is set whenever the comparator output changes state. The flag may be polled by software or may be used to generate an interrupt. The interrupt will be generated when the corresponding enable bit ECn in the IEN1 register is set and the interrupt system is enabled via the EA bit in the IEN0 register.

8.6.4 Comparators and power reduction modes

Either or both comparators may remain enabled when Power-down or Idle mode is activated. The comparators will continue to function in the power reduction mode. If a comparator interrupt is enabled, a change of the comparator output state will generate an interrupt and wake up the processor. If the comparator output to a pin is enabled, the pin should be configured in the push-pull mode in order to obtain fast switching times while in Power-down mode. The reason is that with the oscillator stopped, the temporary strong pull-up that normally occurs during switching on a quasi-bidirectional port pin does not take place.

Comparators consume power in Power-down and Idle modes, as well as in the normal operating mode. This fact should be taken into account when system power consumption is an issue.

8.6.5 Comparator configuration example

The code shown below is an example of initializing one comparator. Comparator 1 is configured to use the CIN1A and CMPREF inputs, outputs the comparator result to the CMP1 pin, and generates an interrupt when the comparator output changes.

```
CmpInit: b
  mov   PT0AD,#30h    ; Disable digital inputs on pins that are used
                      ;   for analog functions: CIN1A, CMPREF.
  anl   P0M2,#0cfh    ; Disable digital outputs on pins that are used
  orl   P0M1,#30h     ;   for analog functions: CIN1A, CMPREF.
  mov   CMP1,#24h     ; Turn on comparator 1 and set up for:
                      ;   - Positive input on CIN1A.
                      ;   - Negative input from CMPREF pin.
                      ;   - Output to CMP1 pin enabled.
  call  delay10us     ; The comparator has to start up for at
                      ;   least 10 microseconds before use.
  anl   CMP1,#0feh    ; Clear comparator 1 interrupt flag.
  setb  EC1           ; Enable the comparator 1 interrupt. The
                      ;   priority is left at the current value.
  setb  EA            ; Enable the interrupt system (if needed).
  ret                 ; Return to caller.
```

The interrupt routine used for the comparator must clear the interrupt flag (CMF1 in this case) before returning.

8.7 I²C-bus serial interface

The I²C-bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus are:

- Bidirectional data transfer between masters and slaves.
- Serial addressing of slaves (no added wiring).

- Acknowledgment after each transferred byte.
- Multimaster bus.
- Arbitration between simultaneously transmitting masters without corruption of serial data on bus.

The I^2C-bus subsystem includes hardware to simplify the software required to drive the I^2C-bus. The hardware is a single bit interface which in addition to including the necessary arbitration and framing error checks, includes clock stretching and a bus timeout timer. The interface is synchronized to software either through polled loops or interrupts. Refer to the application note AN422, in Section 4, entitled *'Using the 8XC751 Microcontroller as an I^2C-bus Master'* for additional discussion of the 87C77x I^2C-bus interface and sample driver routines.

Six time spans are important in I^2C-bus operation and are insured by timer I:

- The MINIMUM HIGH time for SCL when this device is the master.
- The MINIMUM LOW time for SCL when this device is a master. This is not very important for a single-bit hardware interface like this one, because the SCL low time is stretched until the software responds to the I^2C-bus flags. The software response time normally meets or exceeds the MIN LO time. In cases where the software responds within MIN HI + MIN LO) time, timer I will ensure that the minimum time is met.
- The MINIMUM SCL HIGH TO SDA HIGH time in a stop condition.
- The MINIMUM SDA HIGH TO SDA LOW time between I^2C-bus stop and start conditions (4.7 ms, see I^2C-bus specification).
- The MINIMUM SDA LOW TO SCL LOW time in a start condition.

The MAXIMUM SCL CHANGE time while an I^2C-bus frame is in progress. A frame is in progress between a start condition and the following stop condition. This time span serves to detect a lack of software response on this device as well as external I^2C-bus problems. SCL 'stuck low' indicates a faulty master or slave. SCL 'stuck high' may mean a faulty device, or that noise induced onto the I^2C-bus caused all masters to withdraw from I^2C-bus arbitration.

The first five of these times are 4.7 ms (see I^2C-bus specification) and are covered by the low order three bits of timer I. Timer I is clocked by the 87LPC77987 CPU clock. Timer I can be pre-loaded with one of four values to optimize timing for different oscillator frequencies. At lower frequencies, software response time is increased and will degrade maximum performance of the I^2C-bus. See special function register I2CFG description for prescale values (CT0, CT1).

The MAXIMUM SCL CHANGE time is important, but its exact span is not critical. The complete 10 bits of timer I are used to count out the maximum time. When I^2C-bus operation is enabled, this counter is cleared by transitions on the SCL pin. The timer does not run between I^2C-bus frames (i.e., whenever reset or stop occurred more recently than the last start). When this counter is running, it will carry out after 1020 to 1023 machine cycles have elapsed since a change on SCL. A carry out causes a hardware reset of the I^2C-bus interface. In cases where the bus hang-up is due to a lack of software response by this device, the reset releases SCL and allows I^2C-bus operation among other devices to continue.

8.7.1 I²C-bus interrupts

If I²C-bus interrupts are enabled (EA and EI2 are both set to 1), an I²C-bus interrupt will occur whenever the ATN flag is set by a start, stop, arbitration loss, or data ready condition (refer to the description of ATN following). In practice, it is not efficient to operate the I²C-bus interface in this fashion because the I²C-bus interrupt service routine would somehow have to distinguish between hundreds of possible conditions. Also, since I²C-bus can operate at a fairly high rate, the software may execute faster if the code simply waits for the I²C-bus interface.

Typically, the I²C-bus interrupt should only be used to indicate a start condition at an idle slave device, or a stop condition at an idle master device (if it is waiting to use the I²C-bus). This is accomplished by enabling the I²C-bus interrupt only during the aforementioned conditions.

Table 11: I2CON - I²C-bus control register (address D8H) bit allocation

Bit addressable[1]*; Reset value: 81H*

Bit	7	6	5	4	3	2	1	0
Symbol (R)	RDAT	ATN	DRDY	ARL	STR	STP	MASTER	-
Symbol (W)	CXA	IDLE	CDR	CARL	CSTR	CSTP	XSTR	XSTP

[1] Due to the manner in which bit addressing is implemented in the 80C51 family, the I2CON register should never be altered by use of the SETB, CLR, CPL, MOV (bit), or JBC instructions. This is due to the fact that read and write functions of this register are different. Testing of I2CON bits via the JB and JNB instructions is supported.

Table 12: I2CON - I²C-bus control register (address D8H) bit description

Bit	Symbol	Access	Description
7	RDAT	R	The most recently received data bit
	CXA	W	Clears the transmit active flag
6	ATN	R	ATN = 1 if any of the flags DRDY, ARL, STP, or STP = 1
	IDLE	W	In the I²C-bus slave mode, writing a '1' to this bit causes the I²C-bus hardware to ignore the bus until it is needed again
5	DRDY	R	Data Ready flag, set when there is a rising edge on SCL
	CDR	W	Writing a '1' to this bit clears the DRDY flag
4	ARL	R	Arbitration Loss flag, set when arbitration is lost while in the transmit mode
	CARL	W	Writing a '1' to this bit clears the CARL flag
3	STR	R	Start flag, set when a start condition is detected at a master or non-idle slave
	CSTR	W	Writing a '1' to this bit clears the STR flag
2	STP	R	Stop flag, set when a stop condition is detected at a master or non-idle slave
	CSTP	W	Writing a '1' to this bit clears the STP flag
1	MASTER	R	Indicates whether this device is currently as bus master
	XSTR	W	Writing a '1' to this bit causes a repeated start condition to be generated
0	-	R	Undefined
	XSTP	W	Writing a '1' to this bit causes a stop condition to be generated

8.7.2 Reading I2CON

RDAT — The data from SDA is captured into 'Receive DATa' whenever a rising edge occurs on SCL. RDAT is also available (with seven low-order zeros) in the I2DAT register. The difference between reading it here and there is that reading I2DAT clears DRDY, allowing the I^2C-bus to proceed on to another bit. Typically, the first seven bits of a received byte are read from I2DAT, while the 8th is read here. Then I2DAT can be written to send the Acknowledge bit and clear DRDY.

ATN — 'ATteNtion' is '1' when one or more of DRDY, ARL, STR, or STP is '1'. Thus, ATN comprises a single bit that can be tested to release the I^2C-bus service routine from a 'wait loop.'

DRDY — 'Data ReaDY' (and thus ATN) is set when a rising edge occurs on SCL, except at idle slave. DRDY is cleared by writing CDR = 1, or by writing or reading the I2DAT register. The following low period on SCL is stretched until the program responds by clearing DRDY.

8.7.3 Checking ATN and DRDY

When a program detects ATN = '1', it should next check DRDY. If DRDY = '1', then if it receives the last bit, it should capture the data from RDAT (in I2DAT or I2CON). Next, if the next bit is to be sent, it should be written to I2DAT. One way or another, it should clear DRDY and then return to monitoring ATN. Note that if any of ARL, STR, or STP is set, clearing DRDY will not release SCL to HIGH, so that the I^2C-bus will not go on to the next bit. If a program detects ATN = '1', and DRDY = '0', it should go on to examine ARL, STR, and STP.

ARL — 'Arbitration Loss' is '1' when transmit Active was set, but this device lost arbitration to another transmitter. Transmit Active is cleared when ARL is '1'. There are four separate cases in which ARL is set:

1. If the program sent a '1' or repeated start, but another device sent a '0', or a stop, so that SDA is '0' at the rising edge of SCL. (If the other device sent a stop, the setting of ARL will be followed shortly by STP being set.)
2. If the program sent a '1', but another device sent a repeated start, and it drove SDA LOW before SCL could be driven LOW. (This type of ARL is always accompanied by STR = '1'.)
3. In master mode, if the program sent a repeated start, but another device sent a '1', and it drove SCL LOW before this device could drive SDA LOW.
4. In master mode, if the program sent stop, but it could not be sent because another device sent a '0'.

STR — 'STaRt' is set to a '1' when an I^2C-bus start condition is detected at a non-idle slave or at a master. (STR is not set when an idle slave becomes active due to a start bit; the slave has nothing useful to do until the rising edge of SCL sets DRDY.)

STP — 'SToP' is set to '1' when an I^2C-bus stop condition is detected at a non-idle slave or at a master. (STP is not set for a stop condition at an idle slave.)

MASTER — 'MASTER' is '1' if this device is currently a master on the I^2C-bus. MASTER is set when MASTRQ is '1' and the bus is not busy (i.e., if a start bit hasn't been received since reset or a 'Timer I' time-out, or if a stop has been received since the last start). MASTER is cleared when ARL is set, or after the software writes MASTRQ = '0' and then XSTP = '1'.

8.7.4 Writing I2CON

Typically, for each bit in an I²C-bus message, a service routine waits for ATN = 1. Based on DRDY, ARL, STR, and STP, and on the current bit position in the message, it may then write I2CON with one or more of the following bits, or it may read or write the I2DAT register.

CXA — Writing a '1' to 'Clear Xmit Active' clears the Transmit Active state. (Reading the I2DAT register also does this.)

8.7.5 Regarding Transmit Active

Transmit Active is set by writing the I2DAT register, or by writing I2CON with XSTR = 1 or XSTP = 1. The I²C-bus interface will only drive the SDA line low when Transmit Active is set, and the ARL bit will only be set to '1' when Transmit Active is set. Transmit Active is cleared by reading the I2DAT register, or by writing I2CON with CXA = 1. Transmit Active is automatically cleared when ARL is '1'.

IDLE — Writing '1' to 'IDLE' causes a slave's I²C-bus hardware to ignore the I²C-bus until the next start condition (but if MASTRQ is '1', then a stop condition will cause this device to become a master).

CDR — Writing a '1' to 'Clear Data Ready' clears DRDY. (Reading or writing the I2DAT register also does this.)

CARL — Writing a '1' to 'Clear Arbitration Loss' clears the ARL bit.

CSTR — Writing a '1' to 'Clear STaRt' clears the STR bit.

CSTP — Writing a '1' to 'Clear SToP' clears the STP bit. Note that if one or more of DRDY, ARL, STR, or STP is '1', the low time of SCL is stretched until the service routine responds by clearing them.

XSTR — Writing '1's to 'Xmit repeated STaRt' and CDR tells the I²C-bus hardware to send a repeated start condition. This should only be at a master. Note that XSTR need not and should not be used to send an 'initial' (non-repeated) start; it is sent automatically by the I²C-bus hardware. Writing XSTR = '1' includes the effect of writing I2DAT with XDAT = '1'; it sets Transmit Active and releases SDA to HIGH during the SCL low time. After SCL goes HIGH, the I²C-bus hardware waits for the suitable minimum time and then drives SDA low to make the start condition.

XSTP — Writing 1s to 'Xmit SToP' and CDR tells the I²C-bus hardware to send a stop condition. This should only be done at a master. If there are no more messages to initiate, the service routine should clear the MASTRQ bit in I2CFG to '0' before writing XSTP with '1'. Writing XSTP = '1' includes the effect of writing I2DAT with XDAT = '0'; it sets Transmit Active and drives SDA low during the SCL low time. After SCL goes HIGH, the I²C-bus hardware waits for the suitable minimum time and then releases SDA to HIGH to make the stop condition.

Table 13: I2DAT - I²C-bus data register (address D9H) bit allocation

Not bit addressable; Reset value: xxH

Bit	7	6	5	4	3	2	1	0
Symbol (R)	RDAT	-	-	-	-	-	-	-
Symbol (W)	XDAT	-	-	-	-	-	-	-

Table 14: I2DAT - I²C-bus data register (address D9H) bit description

Bit	Symbol	Access	Description
7	RDAT	R	The most recently received data bit, captured from SDA at every rising edge of SCL. Reading I2DAT also clears DRDY and the Transmit Active state.
	XDAT	W	Sets the data for the next transmitted bit. Writing I2DAT also clears DRDY and sets the Transmit Active state.
6 to 0	-	-	Reserved for future use. Should not be set to '1' by user programs.

8.7.6 Regarding software response time

Because the P87LPC779 can run at 20 MHz, and because the I²C-bus interface is optimized for high-speed operation, it is quite likely that an I²C-bus service routine will sometimes respond to DRDY (which is set at a rising edge of SCL) and write I2DAT before SCL has gone low again. If XDAT were applied directly to SDA, this situation would produce an I²C-bus protocol violation. The programmer need not worry about this possibility because XDAT is applied to SDA only when SCL is low.

Conversely, a program that includes an I²C-bus service routine may take a long time to respond to DRDY. Typically, an I²C-bus routine operates on a flag-polling basis during a message, with interrupts from other peripheral functions enabled. If an interrupt occurs, it will delay the response of the I²C-bus service routine. The programmer need not worry about this very much either, because the I²C-bus hardware stretches the SCL low time until the service routine responds. The only constraint on the response is that it must not exceed the Timer I time-out.

Table 15: I2CFG - I²C-bus configuration register (address C8h) bit allocation

Not bit addressable; Reset value: 00H

Bit	7	6	5	4	3	2	1	0
Symbol	SLAVEN	MASTRQ	CLRTI	TIRUN	-	-	CT1	CT0

Table 16: I2CFG - I²C-bus configuration register (address C8h) bit description

Bit	Symbol	Description
7	SLAVEN	Slave Enable. Writing a '1' this bit enables the slave functions of the I²C-bus subsystem. If SLAVEN and MASTRQ are '0', the I²C-bus hardware is disabled. This bit is cleared to '0' by reset and by an I²C-bus time-out.
6	MASTRQ	Master Request. Writing a '1' to this bit requests mastership of the I²C-bus. If a transmission is in progress when this bit is changed from '0' to '1', action is delayed until a stop condition is detected. A start condition is sent and DRDY is set (thus making ATN = '1' and generating an I²C-bus interrupt). When a master wishes to release mastership status of the I²C-bus, it writes a '1' to XSTP in I2CON. MASTRQ is cleared by an I²C-bus time-out.
5	CLRTI	Writing a '1' to this bit clears the Timer I overflow flag. This bit position always reads as a '0'.

Table 16: I2CFG - I²C-bus configuration register (address C8h) bit description

Bit	Symbol	Description
4	TIRUN	Writing a '1' to this bit lets Timer I run; a '0' stops and clears it. Together with SLAVEN, MASTRQ, and MASTER, this bit determines operational modes as shown in Table 17.
3, 2	-	Reserved for future use. Should not be set to '1' by user programs.
1, 0	CT1, CT0	These two bits are programmed as a function of the CPU clock rate, to optimize the MIN HI and LO time of SCL when this device is a master on the I²C-bus. The time value determined by these bits controls both of these parameters, and also the timing for stop and start conditions.

Values to be used in the CT1 and CT0 bits are shown in Table 18. To allow the I²C-bus to run at the maximum rate for a particular oscillator frequency, compare the actual oscillator rate to the f_{osc} max column in the table. The value for CT1 and CT0 is found in the first line of the table where CPU clock max is greater than or equal to the actual frequency. Table 18 also shows the machine cycle count for various settings of CT1/CT0. This allows calculation of the actual minimum high and low times for SCL as follows:

$$\text{SCL min high/low time (in microseconds)} = \frac{6 * \text{min time count}}{\text{CPUclock (in MHz)}} \quad (3)$$

For instance, at an 8 MHz frequency, with CT1/CT0 set to 1 0, the minimum SCL high and low times will be 5.25 µs. Table 18 also shows the Timer I timeout period (given in machine cycles) for each CT1/CT0 combination. The timeout period varies because of the way in which minimum SCL high and low times are measured. When the I²C-bus interface is operating, Timer I is pre-loaded at every SCL transition with a value dependent upon CT1/CT0. The pre-load value is chosen such that a minimum SCL high or low time has elapsed when Timer I reaches a count of 008 (the actual value pre-loaded into Timer I is 8 minus the machine cycle count).

Table 17: Interaction of TIRUN with SLAVEN, MASTRQ, and MASTER

SLAVEN, MASTRQ, MASTER	TIRUN	OPERATING MODE
All 0	0	The I²C-bus interface is disabled. Timer I is cleared and does not run. This is the state assumed after a reset. If an I²C-bus application wants to ignore the I²C-bus at certain times, it should write SLAVEN, MASTRQ, and TIRUN all to zero.
All 0	1	The I²C-bus interface is disabled.
Any or all 1	0	The I²C-bus interface is enabled. The 3 low-order bits of Timer I run for min-time generation, but the hi-order bits do not, so that there is no checking for I²C-bus being 'hung.' This configuration can be used for very slow I²C-bus operation.
Any or all 1	1	The I²C-bus interface is enabled. Timer I runs during frames on the I²C-bus, and is cleared by transitions on SCL, and by Start and Stop conditions. This is the normal state for I²C-bus operation.

Table 18: CT1, CT0 values

CT1, CT0	Min Time Count (Machine Cycles)	CPU Clock Max (for 100 kHz I²C-bus)	Timeout Period (Machine Cycles)
1 0	7	8.4 MHz	1023
0 1	6	7.2 MHz	1022
0 0	5	6.0 MHz	1021
1 1	4	4.8 MHz	1020

8.8 Interrupts

The P87LPC779 uses a four priority level interrupt structure. This allows great flexibility in controlling the handling of the P87LPC779's many interrupt sources. The P87LPC779 supports up to 13 interrupt sources.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in registers IEN0 or IEN1. The IEN0 register also contains a global disable bit, EA, which disables all interrupts at once.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the IP0, IP0H, IP1, and IP1H registers. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. So, if two requests of different priority levels are received simultaneously, the request of higher priority level is serviced.

If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve simultaneous requests of the same priority level.

Table 19 summarizes the interrupt sources, flag bits, vector addresses, enable bits, priority bits, arbitration ranking, and whether each interrupt may wake up the CPU from Power-down mode.

Table 19: Summary of interrupts

Description	Interrupt Flag Bit(s)	Vector Address	Interrupt Enable Bit(s)	Interrupt Priority	Arbitration Ranking	Power-down Wake-up
External Interrupt 0	IE0	0003h	EX0 (IEN0.0)	IP0H.0, IP0.0	1 (highest)	Yes
Timer0 Interrupt	TF0	000Bh	ET0 (IEN0.1)	IP0H.1, IP0.1	4	No
External Interrupt 1	IE1	0013h	EX1 (IEN0.2)	IP0H.2, IP0.2	7	Yes
Timer1 Interrupt	TF1	001Bh	ET1 (IEN0.3)	IP0H.3, IP0.3	10	No
Serial Port Tx and Rx	TI & RI	0023h	ES (IEN0.4)	IP0H.4, IP0.4	12	No
Brownout Detect	BOD	002Bh	EBO (IEN0.5)	IP0H.5, IP0.5	2	Yes
I²C-bus Interrupt	ATN	0033h	EI2 (IEN1.0)	IP1H.0, IP1.0	5	No
KBI Interrupt	KBF	003Bh	EKB (IEN1.1)	IP1H.1, IP1.1	8	Yes
Comparator 2 interrupt	CMF2	0043h	EC2 (IEN1.2)	IP1H.2, IP1.2	11	Yes
Watchdog Timer	WDOVF	0053h	EWD (IEN0.6)	IP0H.6, IP0.6	3	Yes

Table 19: Summary of interrupts...*continued*

Description	Interrupt Flag Bit(s)	Vector Address	Interrupt Enable Bit(s)	Interrupt Priority	Arbitration Ranking	Power-down Wake-up
A/D Converter	ADCI	005Bh	EAD (IEN1.4)	IP1H.4, IP1.4	6	Yes
Comparator 1 interrupt	CMF1	0063h	EC1 (IEN1.5)	IP1H.5, IP1.5	9	Yes
Timer I interrupt	-	0073h	ETI (IEN1.7)	IP1H.7, IP1.7	13 (lowest)	No

8.8.1 External interrupt inputs

The P87LPC779 has two individual interrupt inputs as well as the Keyboard Interrupt function. The latter is described separately elsewhere in this section. The two interrupt inputs are identical to those present on the standard 80C51 microcontroller.

The external sources can be programmed to be level-activated or transition-activated by setting or clearing bit IT1 or IT0 in Register TCON. If ITn = 0, external interrupt n is triggered by a detected low at the $\overline{\text{INTn}}$ pin. If ITn = 1, external interrupt n is edge triggered. In this mode if successive samples of the $\overline{\text{INTn}}$ pin show a high in one cycle and a low in the next cycle, interrupt request flag IEn in TCON is set, causing an interrupt request.

Since the external interrupt pins are sampled once each machine cycle, an input high or low should hold for at least 6 CPU Clocks to ensure proper sampling. If the external interrupt is transition-activated, the external source has to hold the request pin high for at least one machine cycle, and then hold it low for at least one machine cycle. This is to ensure that the transition is seen and that interrupt request flag IEn is set. IEn is automatically cleared by the CPU when the service routine is called.

If the external interrupt is level-activated, the external source must hold the request active until the requested interrupt is actually generated. If the external interrupt is still asserted when the interrupt service routine is completed another interrupt will be generated. It is not necessary to clear the interrupt flag IEn when the interrupt is level sensitive, it simply tracks the input pin level.

If an external interrupt is enabled when the P87LPC779 is put into Power-down or Idle mode, the interrupt will cause the processor to wake up and resume operation. Refer to Section 8.12 “Power reduction modes” on page 38 for details.

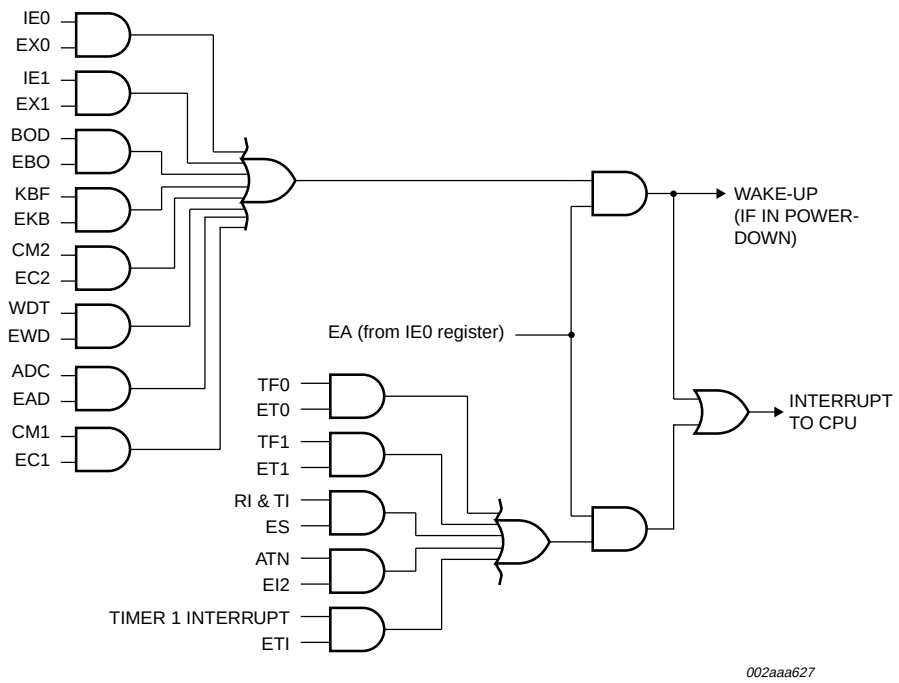


Fig 9. Interrupt sources, interrupt enables, and Power-down wake-up sources.

8.9 I/O ports

The P87LPC779 has 3 I/O ports, port 0, port 1, and port 2. The exact number of I/O pins available depends upon the oscillator and reset options chosen. At least 15 pins of the P87LPC779 may be used as I/Os when a two-pin external oscillator and an external reset circuit are used. Up to 18 pins may be available if fully on-chip oscillator and reset configurations are chosen.

All but three I/O port pins on the P87LPC779 may be software configured to one of four types on a bit-by-bit basis, as shown in Table 20. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open drain, and input only. Two configuration registers for each port choose the output type for each port pin.

Table 20: Port output configuration settings

PxM1.y	PxM2.y	Port output mode
0	0	Quasi-bidirectional
0	1	Push-Pull
1	0	Input Only (High Impedance)
1	1	Open Drain

8.9.1 Quasi-bidirectional output configuration

The default port output configuration for standard P87LPC779 I/O ports is the quasi-bidirectional output that is common on the 80C51 and most of its derivatives. This output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is

pulled LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

One of these pull-ups, called the ‘very weak’ pull-up, is turned on whenever the port latch for the pin contains a logic 1. The very weak pull-up sources a very small current that will pull the pin HIGH if it is left floating.

A second pull-up, called the ‘weak’ pull-up, is turned on when the port latch for the pin contains a logic 1 and the pin itself is also at a logic 1 level. This pull-up provides the primary source current for a quasi-bidirectional pin that is outputting a ‘1’. If a pin that has a logic 1 on it is pulled LOW by an external device, the weak pull-up turns off, and only the very weak pull-up remains on. In order to pull the pin LOW under these conditions, the external device has to sink enough current to overpower the weak pull-up and take the voltage on the port pin below its input threshold.

The third pull-up is referred to as the ‘strong’ pull-up. This pull-up is used to speed up low-to-high transitions on a quasi-bidirectional port pin when the port latch changes from a logic 0 to a logic 1. When this occurs, the strong pull-up turns on for a brief time, two CPU clocks, in order to pull the port pin HIGH quickly. Then it turns off again.

The quasi-bidirectional port configuration is shown in Figure 10.

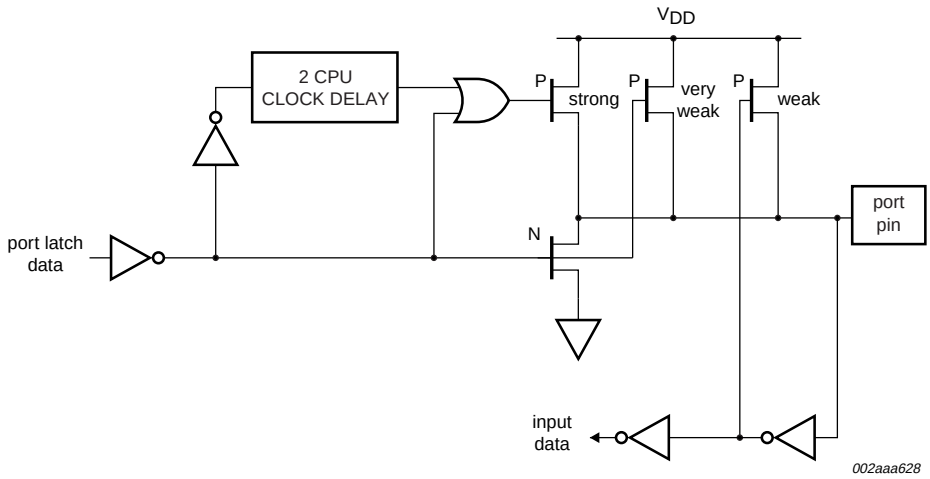


Fig 10. Quasi-bidirectional output.

8.9.2 Open drain output configuration

The open drain output configuration turns off all pull-ups and only drives the pulldown transistor of the port driver when the port latch contains a logic 0. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{DD}. The pulldown for this mode is the same as for the quasi-bidirectional mode.

The open drain port configuration is shown in Figure 11.

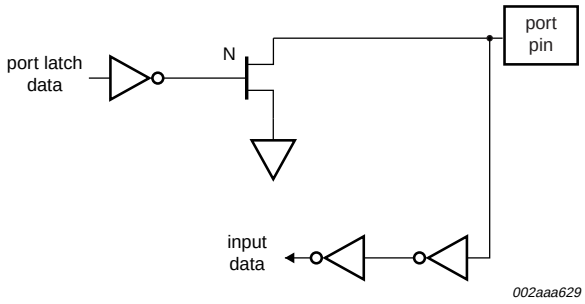


Fig 11. Open drain output.

8.9.3 Push-pull output configuration

The push-pull output configuration has the same pulldown structure as both the open drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The push-pull mode may be used when more source current is needed from a port output.

The push-pull port configuration is shown in Figure 12.

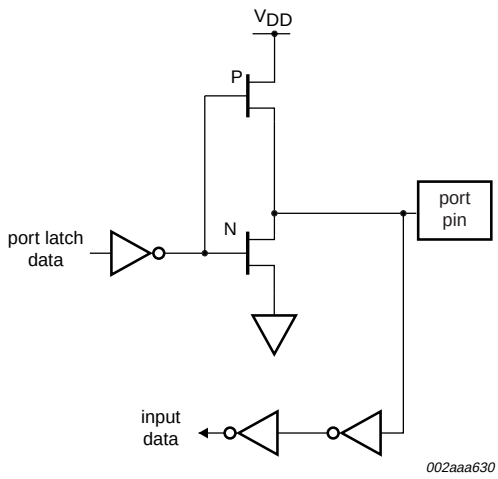


Fig 12. Push-pull output.

The three port pins that cannot be configured are P1.2, P1.3, and P1.5. The port pins P1.2 and P1.3 are permanently configured as open drain outputs. They may be used as inputs by writing ones to their respective port latches. P1.5 may be used as a Schmitt trigger input if the P87LPC779 has been configured for an internal reset and is not using the external reset input function $\overline{\text{RST}}$.

Additionally, port pins P2.0 and P2.1 are disabled for both input and output if one of the crystal oscillator options is chosen. Those options are described in Section 8.10 “Oscillator” on page 34.

The value of port pins at reset is determined by the PRHI bit in the UCFG1 register. Ports may be configured to reset high or low as needed for the application. When port pins are driven high at reset, they are in quasi-bidirectional mode and therefore do not source large amounts of current.

Every output on the P87LPC779 may potentially be used as a 20 mA sink LED drive output. However, there is a maximum total output current for all ports which must not be exceeded.

All ports pins of the P87LPC779 have slew rate controlled outputs. This is to limit noise generated by quickly switching output signals. The slew rate is factory set to approximately 10 ns rise and fall times.

The bits in the P2M1 register that are not used to control configuration of P2.1 and P2.0 are used for other purposes. These bits can enable Schmitt trigger inputs on each I/O port, enable toggle outputs from Timer 0 and Timer 1, and enable a clock output if either the internal RC oscillator or external clock input is being used. The last two functions are described in Section 8.14 “Timer/counters” on page 41 and Section 8.10 “Oscillator” on page 34 respectively. The enable bits for all of these functions are shown in Tables 21 and 22.

Each I/O port of the P87LPC779 may be selected to use TTL level inputs or Schmitt inputs with hysteresis. A single configuration bit determines this selection for the entire port. Port pins P1.2, P1.3, and P1.5 always have a Schmitt trigger input.

Table 21: P2M1 - Port 2 mode register 1 (address A4h) bit allocation

Not bit addressable; Reset value: 00H

Bit	7	6	5	4	3	2	1	0
Symbol	P2S	P1S	P0S	ENCLK	ENT1	ENT0	(P2M1.1)	(P2M1.0)

Table 22: P2M1 - Port 2 mode register 1 (address A4h) bit description

Bit	Symbol	Description
7	P2S	When P2S = 1, this bit enables Schmitt trigger inputs on Port 2.
6	P1S	When P1S = 1, this bit enables Schmitt trigger inputs on Port 1.
5	P0S	When P0S = 1, this bit enables Schmitt trigger inputs on Port 0.
4	ENCLK	When ENCLK is set and the P87LPC779 is configured to use the on-chip RC oscillator, a clock output is enabled on the X2 pin (P2.0). Refer to Section 8.10 “Oscillator” on page 34 for details.
3	ENT1	When set, the P.7 pin is toggled whenever Timer1 overflows. The output frequency is therefore one half of the Timer1 overflow rate. Refer to Section 8.14 “Timer/counters” on page 41 for details.
2	ENT0	When set, the P1.2 pin is toggled whenever Timer0 overflows. The output frequency is therefore one half of the Timer0 overflow rate. Refer to Section 8.14 “Timer/counters” on page 41 for details.
1, 0	-	These bits, along with the matching bits in the P2M2 register, control the output configuration of P2.1 and P2.0 respectively, as shown in Table 20.

8.9.4 Keyboard interrupt (KBI)

The Keyboard Interrupt function is intended primarily to allow a single interrupt to be generated when any key is pressed on a keyboard or keypad connected to specific pins of the P87LPC779, as shown in Figure 13. This interrupt may be used to wake up the CPU from Idle or Power-down modes. This feature is particularly useful in handheld, battery powered systems that need to carefully manage power consumption yet also need to be convenient to use.

The P87LPC779 allows any or all pins of port 0 to be enabled to cause this interrupt. Port pins are enabled by the setting of bits in the KBI register, as shown in Tables 23 and 24. The Keyboard Interrupt Flag (KBF) in the AUXR1 register is set when any enabled pin is pulled LOW while the KBI interrupt function is active. An interrupt will be generated if it has been enabled. Note that the KBF bit must be cleared by software.

Due to human time scales and the mechanical delay associated with keyswitch closures, the KBI feature will typically allow the interrupt service routine to poll port 0 in order to determine which key was pressed, even if the processor has to wake up from Power-down mode. Refer to Section 8.12 “Power reduction modes” on page 38 for details.

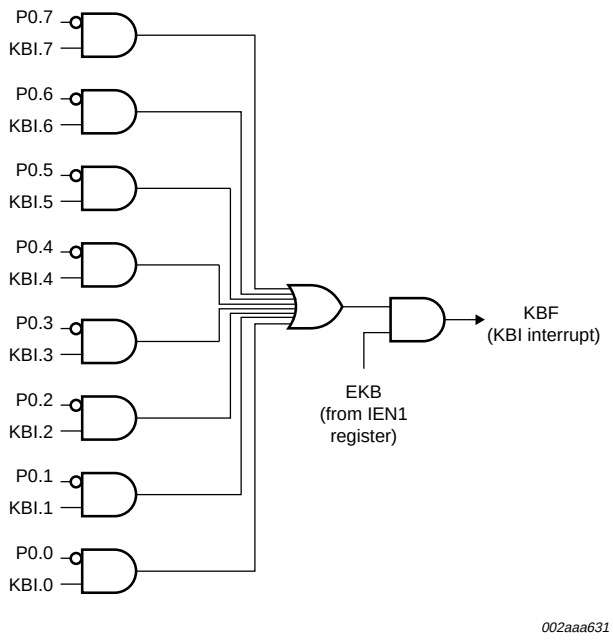


Fig 13. Keyboard interrupt.

Table 23: KBI - Keyboard interrupt register (address 86H) bit allocation

Not bit addressable; Reset value: 00H

Bit	7	6	5	4	3	2	1	0
Symbol	KBI.7	KBI.6	KBI.5	KBI.4	KBI.3	KBI.2	KBI.1	KBI.0

Table 24: KBI - Keyboard interrupt register (address 86H) bit description

Bit	Symbol	Description
7	-	When set, enables P0.7 as a cause of a Keyboard Interrupt.
6	-	When set, enables P0.6 as a cause of a Keyboard Interrupt.
5	-	When set, enables P0.5 as a cause of a Keyboard Interrupt.
4	-	When set, enables P0.4 as a cause of a Keyboard Interrupt.
3	-	When set, enables P0.3 as a cause of a Keyboard Interrupt.
2	-	When set, enables P0.2 as a cause of a Keyboard Interrupt.
1	-	When set, enables P0.1 as a cause of a Keyboard Interrupt.
0	-	When set, enables P0.0 as a cause of a Keyboard Interrupt.

8.10 Oscillator

The P87LPC779 provides several user selectable oscillator options, allowing optimization for a range of needs from high precision to lowest possible cost. These are configured when the EPROM is programmed. Basic oscillator types that are supported include: low, medium, and high speed crystals, covering a range from 20 kHz to 20 MHz; ceramic resonators; and on-chip RC oscillator.

8.10.1 Low speed oscillator option

This option supports an external crystal in the range of 20 kHz to 100 kHz.

Table 25: Recommended oscillator capacitors for use with the low frequency oscillator option

Oscillator Frequency	V_{DD} = 2.7 V to 4.5 V			V_{DD} = 4.5 V to 6.0 V		
	Lower Limit	Optimal Value	Upper Limit	Lower Limit	Optimal Value	Upper Limit
20 kHz	15 pF	15 pF	33 pF	33 pF	33 pF	47 pF
32 kHz	15 pF	15 pF	33 pF	33 pF	33 pF	47 pF
100 kHz	15 pF	15 pF	33 pF	15 pF	15 pF	33 pF

8.10.2 Medium speed oscillator option

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

Table 26: Recommended oscillator capacitors for use with the medium frequency oscillator option

Oscillator Frequency	V_{DD} = 2.7 V to 4.5 V			V_{DD} = 4.5 V to 6.0 V		
	Lower Limit	Optimal Value	Upper Limit	Lower Limit	Optimal Value	Upper Limit
100 kHz	33 pF	33 pF	47 pF	33 pF	33 pF	47 pF
1 MHz	15 pF	15 pF	33 pF	15 pF	22 pF	47 pF
4 MHz	15 pF	15 pF	33 pF	15 pF	15 pF	33 pF

8.10.3 High speed oscillator option

This option supports an external crystal in the range of 4 MHz to 20 MHz. Ceramic resonators are also supported in this configuration.

Table 27: Recommended oscillator capacitors for use with the high frequency oscillator option

Oscillator Frequency	V_{DD} = 2.7 V to 4.5 V			V_{DD} = 4.5 V to 6.0 V		
	Lower Limit	Optimal Value	Upper Limit	Lower Limit	Optimal Value	Upper Limit
4 MHz	15 pF	33 pF	47 pF	15 pF	33 pF	68 pF
8 MHz	15 pF	15 pF	33 pF	15 pF	33 pF	47 pF
16 MHz	-	-	-	15 pF	15 pF	33 pF
20 MHz	-	-	-	15 pF	15 pF	33 pF

8.10.4 On-chip RC oscillator option

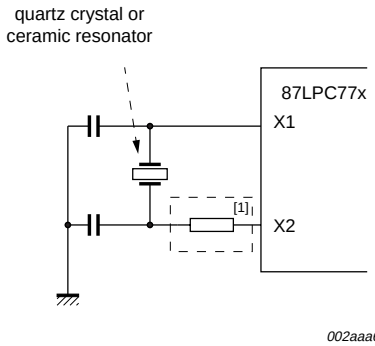
The on-chip RC oscillator option has a typical frequency of 6 MHz and can be divided down for slower operation through the use of the DIVM register. A clock output on the X2 / P2.0 pin may be enabled when the on-chip RC oscillator is used.

8.10.5 External clock input option

In this configuration, the processor clock is input from an external source driving the X1 / P2.1 pin. The rate may be from 0 Hz up to 20 MHz when V_{DD} is above 4.5 V and up to 10 MHz when V_{DD} is below 4.5 V. When the external clock input mode is used, the X2 / P2.0 pin may be used as a standard port pin. A clock output on the X2 / P2.0 pin may be enabled when the external clock input is used.

8.10.6 Clock output

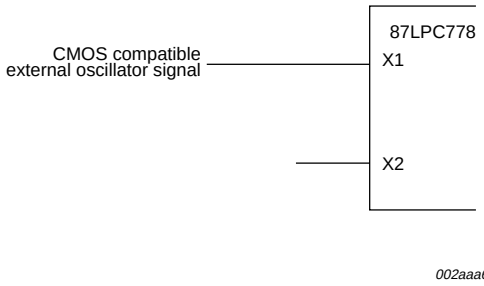
The P87LPC779 supports a clock output function when either the on-chip RC oscillator or external clock input options are selected. This allows external devices to synchronize to the P87LPC779. When enabled, via the ENCLK bit in the P2M1 register, the clock output appears on the X2 / CLKOUT pin whenever the on-chip oscillator is running, including in Idle mode. The frequency of the clock output is $\frac{1}{6}$ of the CPU clock rate. If the clock output is not needed in Idle mode, it may be turned off prior to entering Idle, saving additional power. The clock output may also be enabled when the external clock input option is selected.



The oscillator must be configured in one of the following modes: Low frequency crystal, medium frequency crystal, or high frequency crystal.

(1) A series resistor may be required to limit crystal drive levels. This is especially important for low frequency crystals (see text).

Fig 14. Using the crystal oscillator.



The oscillator must be configured in the External Clock input mode. A clock output may be obtained on the X2 pin by setting the ENCLK bit in the P2M1 register.

Fig 15. Using an external clock input.

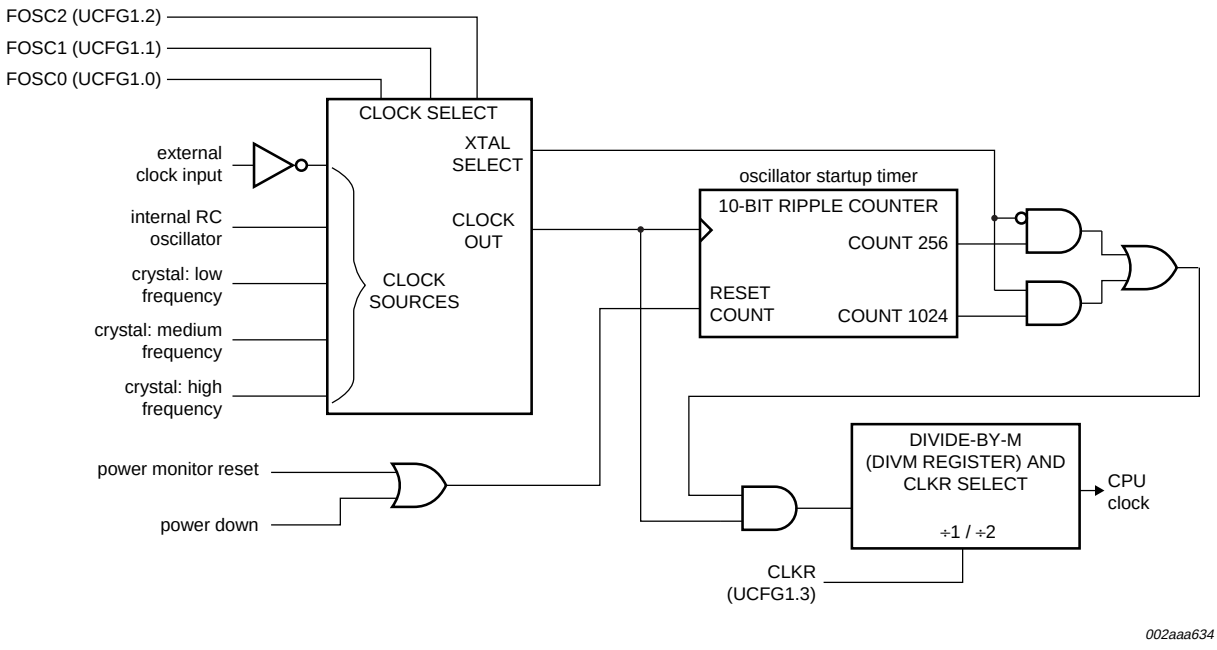


Fig 16. Block diagram of oscillator control.

8.10.7 CPU clock modification: CLKR and DIVM

For backward compatibility, the CLKR configuration bit allows setting the P87LPC779 instruction and peripheral timing to match standard 80C51 timing by dividing the CPU clock by two. Default timing for the P87LPC779 is 6 CPU clocks per machine cycle while standard 80C51 timing is 12 clocks per machine cycle. This division also applies to peripheral timing, allowing 80C51 code that is oscillator frequency and/or timer rate dependent. The CLKR bit is located in the EPROM configuration register UCFG1, described under Section 8.18 “EPROM characteristics” on page 61.

In addition to this, the CPU clock may be divided down from the oscillator rate by a programmable divider, under program control. This function is controlled by the DIVM register. If the DIVM register is set to zero (the default value), the CPU will be clocked by either the unmodified oscillator rate, or that rate divided by two, as determined by the previously described CLKR function.

When the DIVM register is set to some value N (between 1 and 255), the CPU clock is divided by $2 \times (N + 1)$. Clock division values from 4 through 512 are thus possible. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption, in a manner similar to Idle mode. By dividing the clock, the CPU can retain the ability to respond to events other than those that can cause interrupts (i.e., events that allow exiting the Idle mode) by executing its normal program at a lower rate. This can allow bypassing the oscillator startup time in cases where Power-down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

8.11 Power monitoring functions

The P87LPC779 incorporates power monitoring functions designed to prevent incorrect operation during initial power up and power loss or reduction during operation. This is accomplished with two hardware functions: Power-On Detect and Brownout Detect.

8.11.1 Brownout detection

The Brownout Detect function helps prevent the processor from failing in an unpredictable manner if the power supply voltage drops below a certain level. The default operation is for a brownout detection to cause a processor reset, however it may alternatively be configured to generate an interrupt by setting the BOI bit in the AUXR1 register (AUXR1.5).

The P87LPC779 allows selection of two Brownout levels: 2.5 V or 3.8 V. When V_{DD} drops below the selected voltage, the brownout detector triggers and remains active until V_{DD} is returns to a level above the Brownout Detect voltage. When Brownout Detect causes a processor reset, that reset remains active as long as V_{DD} remains below the Brownout Detect voltage. When Brownout Detect generates an interrupt, that interrupt occurs once as V_{DD} crosses from above to below the Brownout Detect voltage. For the interrupt to be processed, the interrupt system and the BOI interrupt must both be enabled (via the EA and EBO bits in IEN0).

When Brownout Detect is activated, the BOF flag in the PCON register is set so that the cause of processor reset may be determined by software. This flag will remain set until cleared by software.

For correct activation of Brownout Detect, the V_{DD} fall time must be no faster than 50 mV/µs. When V_{DD} is restored, is should not rise faster than 2 mV/µs in order to insure a proper reset.

The brownout voltage (2.5 V or 3.8 V) is selected via the BOV bit in the EPROM configuration register UCFG1. When unprogrammed (BOV = 1), the brownout detect voltage is 2.5 V. When programmed (BOV = 0), the brownout detect voltage is 3.8 V.

If the Brownout Detect function is not required in an application, it may be disabled, thus saving power. Brownout Detect is disabled by setting the control bit BOD in the AUXR1 register (AUXR1.6).

8.11.2 Power-on detection

The Power-on Detect has a function similar to the Brownout Detect, but is designed to work as power comes up initially, before the power supply voltage reaches a level where Brownout Detect can work. When this feature is activated, the POF flag in the PCON register is set to indicate an initial power up condition. The POF flag will remain set until cleared by software.

8.12 Power reduction modes

The P87LPC779 supports Idle and Power-down modes of power reduction.

8.12.1 Idle mode

The Idle mode leaves peripherals running in order to allow them to activate the processor when an interrupt is generated. Any enabled interrupt source or Reset may terminate Idle mode. Idle mode is entered by setting the IDL bit in the PCON register (see Tables 29 and 30).

8.12.2 Power-down mode

The Power-down mode stops the oscillator in order to absolutely minimize power consumption. Power-down mode is entered by setting the PD bit in the PCON register (see Tables 29 and 30).

The processor can be made to exit Power-down mode via Reset or one of the interrupt sources shown in Table 28. This will occur if the interrupt is enabled and its priority is higher than any interrupt currently in progress.

In Power-down mode, the power supply voltage may be reduced to the RAM keep-alive voltage V_{RAM}. This retains the RAM contents at the point where Power-down mode was entered. SFR contents are not guaranteed after V_{DD} has been lowered to V_{RAM}, therefore it is recommended to wake up the processor via Reset in this case. V_{DD} must be raised to within the operating range before the Power-down mode is exited. Since the Watchdog timer has a separate oscillator, it may reset the processor upon overflow if it is running during Power-down.

Note that if the Brownout Detect reset is enabled, the processor will be put into reset as soon as V_{DD} drops below the brownout voltage. If Brownout Detect is configured as an interrupt and is enabled, it will wake up the processor from Power-down mode when V_{DD} drops below the brownout voltage.

When the processor wakes up from Power-down mode, it will start the oscillator immediately and begin execution when the oscillator is stable. Oscillator stability is determined by counting 1024 CPU clocks after start-up when one of the crystal oscillator configurations is used, or 256 clocks after start-up for the internal RC or external clock input configurations.

Table 28: Interrupt sources

Wake-up Source	Conditions
External Interrupt 0 or 1	The corresponding interrupt must be enabled.
Keyboard Interrupt	The keyboard interrupt feature must be enabled and properly set up. The corresponding interrupt must be enabled.
Comparator 1 or 2	The comparator(s) must be enabled and properly set up. The corresponding interrupt must be enabled.
Watchdog Timer Reset	The Watchdog timer must be enabled via the WDTE bit in the UCFG1 EPROM configuration byte.
Watchdog Timer Interrupt	The WDTE bit in the UCFG1 EPROM configuration byte must not be set. The corresponding interrupt must be enabled.
Brownout Detect Reset	The BOD bit in AUXR1 must not be set (brownout detect not disabled). The BOI bit in AUXR1 must not be set (brownout interrupt disabled).
Brownout Detect Interrupt	The BOD bit in AUXR1 must not be set (brownout detect not disabled). The BOI bit in AUXR1 must be set (brownout interrupt enabled). The corresponding interrupt must be enabled.
Reset Input	The external reset input must be enabled.
A/D Converter	Must use internal RC clock (RCCLK = 1) for A/D converter to work in Power-down mode. The A/D must be enabled and properly set up. The corresponding interrupt must be enabled.

Some chip functions continue to operate and draw power during Power-down mode, increasing the total power used during Power-down. These include the Brownout Detect, Watchdog Timer, and Comparators.

8.12.3 Low voltage EPROM operation

The EPROM array contains some analog circuits that are not required when V_{DD} is less than 4 V, but are required for a V_{DD} greater than 4 V. The LPEP bit (AUXR.4), when set by software, will Power-down these analog circuits resulting in a reduced supply current. LPEP is cleared only by power-on reset, so it may be set ONLY for applications that always operate with V_{DD} less than 4 V.

Table 29: PCON - Power control register (address 87H) bit allocation

Not bit addressable; Reset value: 30H for a Power-on reset; 20H for a Brownout reset; 00H for other reset sources.

Bit	7	6	5	4	3	2	1	0
Symbol	SMOD1	SMOD0	BOF	POF	GF1	GF0	PD	IDL

Table 30: PCON - Power control register (address 87H) bit description

Bit	Symbol	Description
7	SMOD1	When set, this bit doubles the UART baud rate for modes 1, 2, and 3.
6	SMOD0	This bit selects the function of bit 7 of the SCON SFR. When 0, SCON.7 is the SM0 bit. When 1, SCON.7 is the FE (Framing Error) flag. See Tables 36 and 37 for additional information.
5	BOF	Brown Out Flag. Set automatically when a brownout reset or interrupt has occurred. Also set at Power-on. Cleared by software. Refer to Section 8.11 “Power monitoring functions” on page 37 for additional information.

Table 30: PCON - Power control register (address 87H) bit description*...continued*

Bit	Symbol	Description
4	POF	Power-on Flag. Set automatically when a power-on reset has occurred. Cleared by software. Refer to the Section 8.11 “Power monitoring functions” on page 37 for additional information.
3	GF1	General purpose flag 1. May be read or written by user software, but has no effect on operation.
2	GF0	General purpose flag 0. May be read or written by user software, but has no effect on operation.
1	PD	Power-down control bit. Setting this bit activates Power-down mode operation. Cleared when the Power-down mode is terminated (see text).
0	IDL	Idle mode control bit. Setting this bit activates Idle mode operation. Cleared when the Idle mode is terminated (see text).

8.13 Reset

The P87LPC779 has an active LOW reset input when configured for an external reset. A fully internal reset may also be configured which provides a reset when power is initially applied to the device. The Watchdog timer can act as an oscillator fail detect because it uses an independent, fully on-chip oscillator.

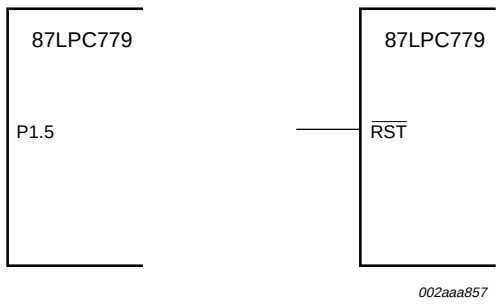


Fig 17. Typical external reset circuits.

The external reset input is disabled, and fully internal reset generation enabled, by programming the RPD bit in the EPROM configuration register UCFG1 to 0. EPROM configuration is described in Section 8.18 “EPROM characteristics” on page 61.

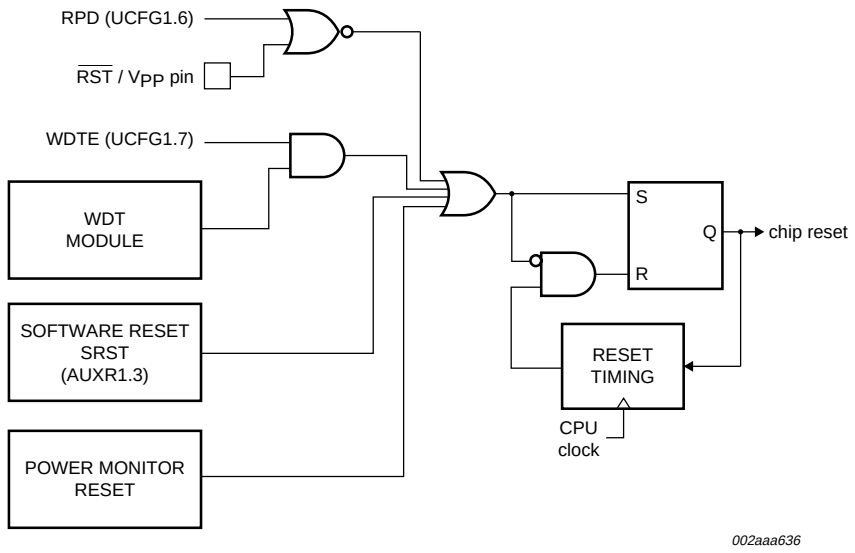


Fig 18. Block diagram showing reset sources.

8.14 Timer/counters

The P87LPC779 has two general purpose counter/timers which are upward compatible with the standard 80C51 Timer0 and Timer1. Both can be configured to operate either as timers or event counters (see Tables 31 and 32). An option to automatically toggle the T0 and/or T1 pins upon timer overflow has been added.

In the 'Timer' function, the register is incremented every machine cycle. Thus, one can think of it as counting machine cycles. Since a machine cycle consists of 6 CPU clock periods, the count rate is $\frac{1}{6}$ of the CPU clock frequency. Refer to Section 8.1 "Enhanced CPU" on page 12 for a description of the CPU clock.

In the 'Counter' function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled once during every machine cycle. When the samples of the pin state show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (12 CPU clocks) to recognize a 1-to-0 transition, the maximum count rate is $\frac{1}{6}$ of the CPU clock frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

The 'Timer' or 'Counter' function is selected by control bits C/T in the Special Function Register TMOD. In addition to the 'Timer' or 'Counter' selection, Timer0 and Timer1 have four operating modes, which are selected by bit-pairs (M1, M0) in TMOD. Modes 0, 1, and 2 are the same for both Timers/Counters. Mode 3 is different. The four operating modes are described in the following text.

Table 31: TMOD - Timer/counter mode control register (address 89H) bit allocation

Not bit addressable; Reset value: 00H

Bit	7	6	5	4	3	2	1	0
Symbol	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0

Table 32: TMOD - Timer/counter mode control register (address 89H) bit description

Bit	Symbol	Description
7	GATE	Gating control for Timer1. When set, Timer/Counter is enabled only while the INT1 pin is high and the TR1 control pin is set. When cleared, Timer1 is enabled when the TR1 control bit is set.
6	C/$\overline{T}$	Timer or Counter Selector for Timer1. Cleared for Timer operation (input from internal system clock.) Set for Counter operation (input from T1 input pin).
5, 4	M1, M0	Mode select for Timer1 (see table below).
3	GATE	Gating control for Timer0. When set, Timer/Counter is enabled only while the $\overline{INT0}$ pin is high and the TR0 control pin is set. When cleared, Timer0 is enabled when the TR0 control bit is set.
2	C/$\overline{T}$	Timer or Counter Selector for Timer0. Cleared for Timer operation (input from internal system clock.) Set for Counter operation (input from T0 input pin).
1, 0	M1, M0	Mode Select for Timer0 (see Table 33 below).

Table 33: M1, M0 timer mode

M1, M0	Timer mode
0 0	8048 Timer 'TLn' serves as 5-bit prescaler.
0 1	16-bit Timer/Counter 'THn' and 'TLn' are cascaded; there is no prescaler.
1 0	8-bit auto-reload Timer/Counter. THn holds a value which is loaded into TLn when it overflows.
1 1	Timer0 is a dual 8-bit Timer/Counter in this mode. TL0 is an 8-bit Timer/Counter controlled by the standard Timer0 control bits. TH0 is an 8-bit timer only, controlled by the Timer1 control bits (see text). Timer1 in this mode is stopped.

8.14.1 Mode 0

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. Figure 19 shows Mode 0 operation.

In this mode, the Timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the Timer interrupt flag TFn. The count input is enabled to the Timer when TRn = 1 and either GATE = 0 or $\overline{INTn}$ = 1. (Setting GATE = 1 allows the Timer to be controlled by external input $\overline{INTn}$, to facilitate pulse width measurements). TRn is a control bit in the Special Function Register TCON (Tables 34 and 35). The GATE bit is in the TMOD register.

The 13-bit register consists of all 8 bits of THn and the lower 5 bits of TLn. The upper 3 bits of TLn are indeterminate and should be ignored. Setting the run flag (TRn) does not clear the registers.

Mode 0 operation is the same for Timer0 and Timer1. See Figure 19. There are two different GATE bits, one for Timer1 (TMOD.7) and one for Timer0 (TMOD.3).

8.14.2 Mode 1

Mode 1 is the same as Mode 0, except that all 16 bits of the timer register (THn and TLn) are used. See Figure 20.

8.14.3 Mode 2

Mode 2 configures the Timer register as an 8-bit Counter (TL1) with automatic reload, as shown in Figure 21. Overflow from TLn not only sets TFn, but also reloads TLn with the contents of THn, which must be preset by software. The reload leaves THn unchanged. Mode 2 operation is the same for Timer0 and Timer1.

8.14.4 Mode 3

When Timer1 is in Mode 3 it is stopped. The effect is the same as setting TR1 = 0.

Timer0 in Mode 3 establishes TL0 and TH0 as two separate 8-bit counters. The logic for Mode 3 on Timer0 is shown in Figure 22. TL0 uses the Timer0 control bits: C/T, GATE, TR0, $\overline{\text{INT0}}$, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer1. Thus, TH0 now controls the 'Timer1' interrupt.

Mode 3 is provided for applications that require an extra 8-bit timer. With Timer0 in Mode 3, an P87LPC779 can look like it has three Timer/Counters. When Timer0 is in Mode 3, Timer1 can be turned on and off by switching it into and out of its own Mode 3. It can still be used by the serial port as a baud rate generator, or in any application not requiring an interrupt.

Table 34: TCON - Timer/counter control register (address 88H) bit allocation

Bit addressable; Reset value: 00H

Bit	7	6	5	4	3	2	1	0
Symbol	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Table 35: TCON - Timer/counter control register (address 88H) bit description

Bit	Symbol	Description
7	TF1	Timer1 overflow flag. Set by hardware on Timer/Counter overflow. Cleared by hardware when the interrupt is processed, or by software.
6	TR1	Timer1 Run control bit. Set/cleared by software to turn Timer/Counter 1 on/off.
5	TF0	Timer0 overflow flag. Set by hardware on Timer/Counter overflow. Cleared by hardware when the processor vectors to the interrupt routine, or by software.
4	TR0	Timer0 Run control bit. Set/cleared by software to turn Timer/Counter 0 on/off.
3	IE1	Interrupt 1 Edge flag. Set by hardware when external interrupt 1 edge is detected. Cleared by hardware when the interrupt is processed, or by software.

Table 35: TCON - Timer/counter control register (address 88H) bit description

Bit	Symbol	Description
2	IT1	Interrupt 1 Type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupts.
1	IE0	Interrupt 0 Edge flag. Set by hardware when external interrupt 0 edge is detected. Cleared by hardware when the interrupt is processed, or by software.
0	IT0	Interrupt 0 Type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupts.

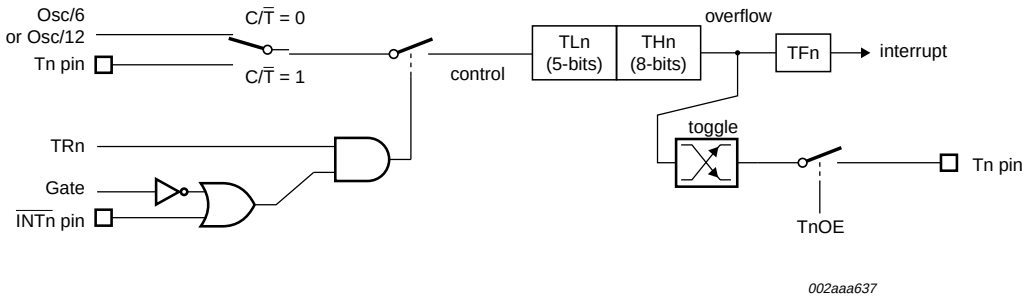


Fig 19. Timer/counter 0 or 1 in Mode 0 (13-bit counter).

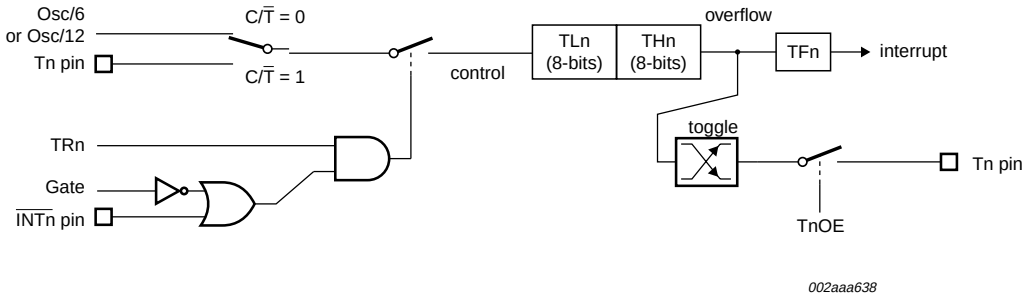


Fig 20. Timer/counter 0 or 1 in Mode 1 (16-bit counter).

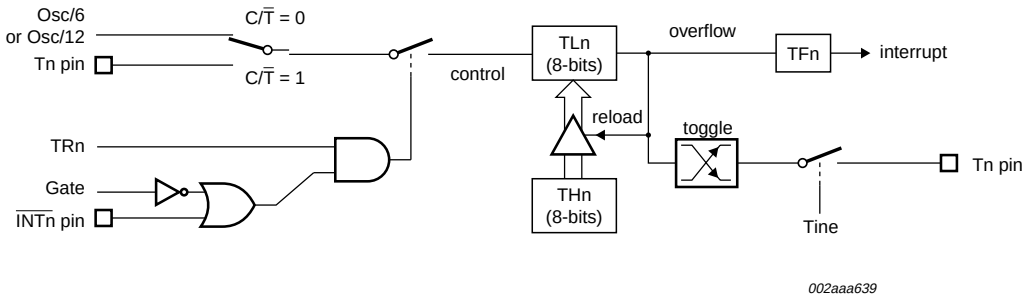


Fig 21. Timer/counter 0 or 1 in Mode 2 (8-bit auto-reload).

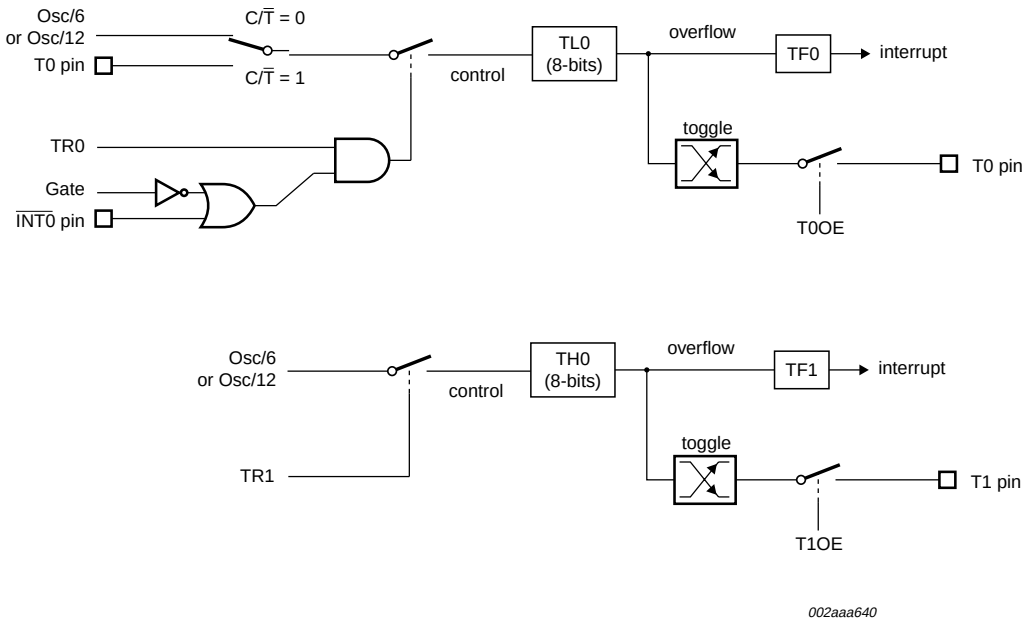


Fig 22. Timer/counter 0 Mode 3 (two 8-bit counters).

8.14.5 Timer overflow toggle output

Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. This function is enabled by control bits ENT0 and ENT1 in the P2M1 register, and apply to Timer0 and Timer1 respectively. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

8.15 UART

The P87LPC779 includes an enhanced 80C51 UART. The baud rate source for the UART is Timer1 for modes 1 and 3, while the rate is fixed in modes 0 and 2. Because CPU clocking is different on the P87LPC779 than on the standard 80C51, baud rate calculation is somewhat different. Enhancements over the standard 80C51 UART include Framing Error detection and automatic address recognition.

The serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the SBUF register. However, if the first byte still hasn't been read by the time reception of the second byte is complete, the first byte will be lost. The serial port receive and transmit registers are both accessed through Special Function Register SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

The serial port can be operated in 4 modes.

8.15.1 Mode 0

Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at $\frac{1}{6}$ of the CPU clock frequency.

8.15.2 Mode 1

10 bits are transmitted (through TxD) or received (through RxD): a start bit (logic 0), 8 data bits (LSB first), and a stop bit (logic 1). When data is received, the stop bit is stored in RB8 in Special Function Register SCON. The baud rate is variable and is determined by the Timer1 overflow rate.

8.15.3 Mode 2

11 bits are transmitted (through TxD) or received (through RxD): start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of '0' or '1'. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. When data is received, the 9th data bit goes into RB8 in Special Function Register SCON, while the stop bit is ignored. The baud rate is programmable to either $\frac{1}{16}$ or $\frac{1}{32}$ of the CPU clock frequency, as determined by the SMOD1 bit in PCON.

8.15.4 Mode 3

11 bits are transmitted (through TxD) or received (through RxD): a start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable and is determined by the Timer1 overflow rate.

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

8.15.5 Serial port control register (SCON)

The serial port control and status register is the Special Function Register SCON, shown in Tables 36 and 37. This register contains not only the mode selection bits, but also the 9th data bit for transmit and receive (TB8 and RB8), and the serial port interrupt bits (TI and RI).

The Framing Error bit (FE) allows detection of missing stop bits in the received data stream. The FE bit shares the bit position SCON.7 with the SM0 bit. Which bit appears in SCON at any particular time is determined by the SMOD0 bit in the PCON register. If SMOD0 = 0, SCON.7 is the SM0 bit. If SMOD0 = 1, SCON.7 is the FE bit. Once set, the FE bit remains set until it is cleared by software. This allows detection of framing errors for a group of characters without the need for monitoring it for every character individually.

Table 36: SCON - Serial port control register (address 98H) bit allocation

Bit addressable; Reset value: 00H

Bit	7	6	5	4	3	2	1	0
Symbol	FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Table 37: SCON - Serial port control register (address 98H) bit description

Bit	Symbol	Description
7	FE	Framing Error. This bit is set by the UART receiver when an invalid stop bit is detected. Must be cleared by software. The SMOD0 bit in the PCON register must be '1' for this bit to be accessible. See SM0 bit below.
	SM0	With SM1, defines the serial port mode. The SMOD0 bit in the PCON register must be '0' for this bit to be accessible. See FE bit above.
6	SM1	With SM0, defines the serial port mode (see Table 38 below).
5	SM2	Enables the multiprocessor communication feature in Modes 2 and 3. In Mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In Mode 1, if SM2 = 1 then RI will not be activated if a valid stop bit was not received. In Mode 0, SM2 should be 0.
4	REN	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.
3	TB8	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.
2	RB8	In Modes 2 and 3, is the 9th data bit that was received. In Mode 1, it SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
1	TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
0	RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

Table 38: SM0, SM1 serial port mode

SM0, SM1	UART mode	Baud rate
0 0	0: shift register	CPU clock/6
0 1	1: 8-bit UART	variable (see text)
1 0	2: 9-bit UART	CPU clock/32 or CPU clock/16
1 1	3: 9-bit UART	variable (see text)

8.15.6 Baud rates

The baud rate in Mode 0 is fixed: Mode 0 Baud Rate = CPU clock/6. The baud rate in Mode 2 depends on the value of bit SMOD1 in Special Function Register PCON. If SMOD1 = 0 (which is the value on reset), the baud rate is $1/32$ of the CPU clock frequency. If SMOD1 = 1, the baud rate is $1/16$ of the CPU clock frequency.

$$\text{Mode 2 baud rate} = \frac{1 + SMOD1}{32} \times \text{CPU clock frequency} \quad (4)$$

8.15.7 Using Timer1 to generate baud rates

When Timer1 is used as the baud rate generator, the baud rates in Modes 1 and 3 are determined by the Timer1 overflow rate and the value of SMOD1. The Timer1 interrupt should be disabled in this application. The Timer itself can be configured for either 'timer' or 'counter' operation, and in any of its 3 running modes. In the most typical applications, it is configured for 'timer' operation, in the auto-reload mode (high nibble of TMOD = 0010b). In that case the baud rate is given by the formula:

$$\text{Mode 1, 3 baud rate} = \frac{\text{CPU clock frequency / 192 (or 96 if SMOD 1 = 1)}}{256 - (TH1)} \quad (5)$$

Tables 39 and 40 list various commonly used baud rates and how they can be obtained using Timer1 as the baud rate generator.

Table 39: Baud rates, timer values, and CPU clock frequencies for SMOD1 = 0

Timer Count	Baud Rate					
	2400	4800	9600	19.2 k	38.4 k	57.6 k
–1	0.4608	0.9216	* 1.8432	* 3.6864	* 7.3728	* 11.0592
–2	0.9216	1.8432	* 3.6864	* 7.3728	* 14.7456	
–3	1.3824	2.7648	5.5296	* 11.0592	-	-
–4	* 1.8432	* 3.6864	* 7.3728	* 14.7456	-	-
–5	2.3040	4.6080	9.2160	* 18.4320	-	-
–6	2.7648	5.5296	* 11.0592	-	-	-
–7	3.2256	6.4512	12.9024	-	-	-
–8	* 3.6864	* 7.3728	* 14.7456	-	-	-
–9	4.1472	8.2944	16.5888	-	-	-
–10	4.6080	9.2160	* 18.4320	-	-	-

Table 40: Baud rates, timer values, and CPU clock frequencies for SMOD1 = 1

Timer Value	Baud Rate						
	2400	4800	9600	19.2 k	38.4 k	57.6 k	115.2 k
–1	0.2304	0.4608	0.9216	* 1.8432	* 3.6864	5.5296	* 11.0592
–2	0.4608	0.9216	* 1.8432	* 3.6864	* 7.3728	* 11.0592	-
–3	0.6912	1.3824	2.7648	5.5296	* 11.0592	16.5888	-
–4	0.9216	* 1.8432	* 3.6864	* 7.3728	* 14.7456	-	-
–5	1.1520	2.3040	4.6080	9.2160	* 18.4320	-	-
–6	1.3824	2.7648	5.5296	* 11.0592	-	-	-
–7	1.6128	3.2256	6.4512	12.9024	-	-	-
–8	* 1.8432	* 3.6864	* 7.3728	* 14.7456	-	-	-
–9	2.0736	4.1472	8.2944	16.5888	-	-	-
–10	2.3040	4.6080	9.2160	* 18.4320	-	-	-
–11	2.5344	5.0688	10.1376	-	-	-	-
–12	2.7648	5.5296	* 11.0592	-	-	-	-
–13	2.9952	5.9904	11.9808	-	-	-	-
–14	3.2256	6.4512	12.9024	-	-	-	-

Table 40: Baud rates, timer values, and CPU clock frequencies for SMOD1 = 1*...continued*

Timer Value	Baud Rate						
	2400	4800	9600	19.2 k	38.4 k	57.6 k	115.2 k
–15	3.4560	6.9120	13.8240	-	-	-	-
–16	* 3.6864	* 7.3728	* 14.7456	-	-	-	-
–17	3.9168	7.8336	15.6672	-	-	-	-
–18	4.1472	8.2944	16.5888	-	-	-	-
–19	4.3776	8.7552	17.5104	-	-	-	-
–20	4.6080	9.2160	* 18.4320	-	-	-	-
–21	4.8384	9.6768	19.3536	-	-	-	-

[1] Tables 39 and 40 apply to UART modes 1 and 3 (variable rate modes), and show CPU clock rates in MHz for standard baud rates from 2400 to 115.2 kbaud.

[2] Table 39 shows timer settings and CPU clock rates with the SMOD1 bit in the PCON register = 0 (the default after reset), while Table 40 reflects the SMOD1 bit = 1.

[3] The tables show all potential CPU clock frequencies up to 20 MHz that may be used for baud rates from 9600 baud to 115.2 kbaud. Other CPU clock frequencies that would give only lower baud rates are not shown.

[4] Table entries marked with an asterisk (*) indicate standard crystal and ceramic resonator frequencies that may be obtained from many sources without special ordering.

8.15.8 More about UART Mode 0

Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received: 8 data bits (LSB first). The baud rate is fixed at $\frac{1}{6}$ the CPU clock frequency. Figure 23 shows a simplified functional diagram of the serial port in Mode 0, and associated timing.

Transmission is initiated by any instruction that uses SBUF as a destination register. The ‘write to SBUF’ signal at S6P2 also loads a ‘1’ into the 9th position of the transmit shift register and tells the TX Control block to commence a transmission. The internal timing is such that one full machine cycle will elapse between ‘write to SBUF’ and activation of SEND.

SEND enables the output of the shift register to the alternate output function line of P3.0 and also enable SHIFT CLOCK to the alternate output function line of P3.1. SHIFT CLOCK is low during S3, S4, and S5 of every machine cycle, and high during S6, S1, and S2. At S6P2 of every machine cycle in which SEND is active, the contents of the transmit shift are shifted to the right one position.

As data bits shift out to the right, zeros come in from the left. When the MSB of the data byte is at the output position of the shift register, then the ‘1’ that was initially loaded into the 9th position, is just to the left of the MSB, and all positions to the left of that contain zeros. This condition flags the TX Control block to do one last shift and then deactivate SEND and set T1. Both of these actions occur at S1P1 of the 10th machine cycle after ‘write to SBUF.’ Reception is initiated by the condition REN = 1 and R1 = 0. At S6P2 of the next machine cycle, the RX Control unit writes the bits 11111110 t o the receive shift register, and in the next clock phase activates RECEIVE.

RECEIVE enable SHIFT CLOCK to the alternate output function line of P3.1. SHIFT CLOCK makes transitions at S3P1 and S6P1 of every machine cycle. At S6P2 of every machine cycle in which RECEIVE is active, the contents of the receive shift register are shifted to the left one position. The value that comes in from the right is the value that was sampled at the P3.0 pin at S5P2 of the same machine cycle.

As data bits come in from the right, 1s shift out to the left. When the '0' that was initially loaded into the rightmost position arrives at the leftmost position in the shift register, it flags the RX Control block to do one last shift and load SBUF. At S1P1 of the 10th machine cycle after the write to SCON that cleared RI, RECEIVE is cleared as RI is set.

8.15.9 More about UART Mode 1

Ten bits are transmitted (through TxD), or received (through RxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in SCON. In the P87LPC779 the baud rate is determined by the Timer1 overflow rate. Figure 24 shows a simplified functional diagram of the serial port in Mode 1, and associated timings for transmit receive.

Transmission is initiated by any instruction that uses SBUF as a destination register. The 'write to SBUF' signal also loads a '1' into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission actually commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. (Thus, the bit times are synchronized to the divide-by-16 counter, not to the 'write to SBUF' signal.)

The transmission begins with activation of SEND which puts the start bit at TxD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TxD. The first shift pulse occurs one bit time after that.

As data bits shift out to the right, zeros are clocked in from the left. When the MSB of the data byte is at the output position of the shift register, then the '1' that was initially loaded into the 9th position is just to the left of the MSB, and all positions to the left of that contain zeros. This condition flags the TX Control unit to do one last shift and then deactivate SEND and set TI. This occurs at the 10th divide-by-16 rollover after 'write to SBUF.'

Reception is initiated by a detected 1-to-0 transition at RxD. For this purpose RxD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written into the input shift register. Resetting the divide-by-16 counter aligns its rollovers with the boundaries of the incoming bit times.

The 16 states of the counter divide each bit time into 16ths. At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of RxD. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. This is to provide rejection of false start bits. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

As data bits come in from the right, 1s shift out to the left. When the start bit arrives at the leftmost position in the shift register (which in mode 1 is a 9-bit register), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI. The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated:

1. R1 = 0, and
2. Either SM2 = 0, or the received stop bit = 1.

If either of these two conditions is not met, the received frame is irretrievably lost. If both conditions are met, the stop bit goes into RB8, the 8 data bits go into SBUF, and RI is activated. At this time, whether the above conditions are met or not, the unit goes back to looking for a 1-to-0 transition in RxD.

8.15.10 More about UART Modes 2 and 3

Eleven bits are transmitted (through TxD), or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On transmit, the 9th data bit (TB8) can be assigned the value of '0' or '1'. On receive, the 9th data bit goes into RB8 in SCON. The baud rate is programmable to either $^1/_{16}$ or $^1/_{32}$ of the CPU clock frequency in Mode 2. Mode 3 may have a variable baud rate generated from Timer1.

Figures 25 and 26 show a functional diagram of the serial port in Modes 2 and 3. The receive portion is exactly the same as in Mode 1. The transmit portion differs from Mode 1 only in the 9th bit of the transmit shift register.

Transmission is initiated by any instruction that uses SBUF as a destination register. The 'write to SBUF' signal also loads TB8 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. (Thus, the bit times are synchronized to the divide-by-16 counter, not to the 'write to SBUF' signal.)

The transmission begins with activation of SEND, which puts the start bit at TxD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TxD. The first shift pulse occurs one bit time after that. The first shift clocks a '1' (the stop bit) into the 9th bit position of the shift register. Thereafter, only zeros are clocked in. Thus, as data bits shift out to the right, zeros are clocked in from the left. When TB8 is at the output position of the shift register, then the stop bit is just to the left of TB8, and all positions to the left of that contain zeros. This condition flags the TX Control unit to do one last shift and then deactivate SEND and set TI. This occurs at the 11th divide-by-16 rollover after 'write to SBUF.'

Reception is initiated by a detected 1-to-0 transition at RxD. For this purpose RxD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written to the input shift register.

At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of R-D. The value accepted is the value that was seen in at least 2 of the 3 samples. If the value accepted during the first bit time is not 0, the receive circuits are

reset and the unit goes back to looking for another 1-to-0 transition. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

As data bits come in from the right, 1s shift out to the left. When the start bit arrives at the leftmost position in the shift register (which in Modes 2 and 3 is a 9-bit register), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI.

The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated. 1. RI = 0, and 2. Either SM2 = 0, or the received 9th data bit = 1.

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set. If both conditions are met, the received 9th data bit goes into RB8, and the first 8 data bits go into SBUF. One bit time later, whether the above conditions were met or not, the unit goes back to looking for a 1-to-0 transition at the RxD input.

8.15.11 Multiprocessor communications

UART modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received or transmitted. When data is received, the 9th bit is stored in RB8. The UART can be programmed such that when the stop bit is received, the serial port interrupt will be activated only if RB8 = 1. This feature is enabled by setting bit SM2 in SCON. One way to use this feature in multiprocessor systems is as follows:

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is ‘1’ in an address byte and ‘0’ in a data byte. With SM2 = 1, no slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that follow. The slaves that weren’t being addressed leave their SM2 bits set and go on about their business, ignoring the subsequent data bytes.

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the stop bit, although this is better done with the Framing Error flag. In a Mode 1 reception, if SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

8.15.12 Automatic address recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON. In the 9 bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the ‘Given’ address or the ‘Broadcast’ address. The 9 bit mode requires that the 9th information bit is a ‘1’ to indicate that the received information is an address and not data.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave's address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are 'don't care'. The SADEN mask can be logically ANDed with the SADDR to create the 'Given' address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme:

Table 41: Slave 0/1 examples

Example 1			Example 2		
Slave 0	SADDR =	1100 0000	Slave 1	SADDR =	1100 0000
	SADEN =	1111 1101		SADEN =	1111 1110
	Given =	1100 00X0		Given =	1100 000X

In the above example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a '0' in bit 0 and it ignores bit 1. Slave 1 requires a '0' in bit 1 and bit 0 is ignored. A unique address for Slave 0 would be 1100 0010 since slave 1 requires a '0' in bit 1. A unique address for slave 1 would be 1100 0001 since a '1' in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Table 42: Slave 0/1/2 examples

Example 1			Example 2			Example 3		
Slave 0	SADDR =	1100 0000	Slave 1	SADDR =	1110 0000	Slave 2	SADDR =	1110 0000
	SADEN =	1111 1001		SADEN =	1111 1010		SADEN =	1111 1100
	Given =	1100 0XX0		Given =	1110 0X0X		Given =	1110 00XX

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2 use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2. The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are treated as don't-cares. In most cases, interpreting the don't-cares as ones, the broadcast address will be FF hexadecimal. Upon reset SADDR and SADEN are loaded with 0s. This produces a given address of all 'don't cares' as well as a Broadcast address of all 'don't cares'. This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard UART drivers which do not make use of this feature.

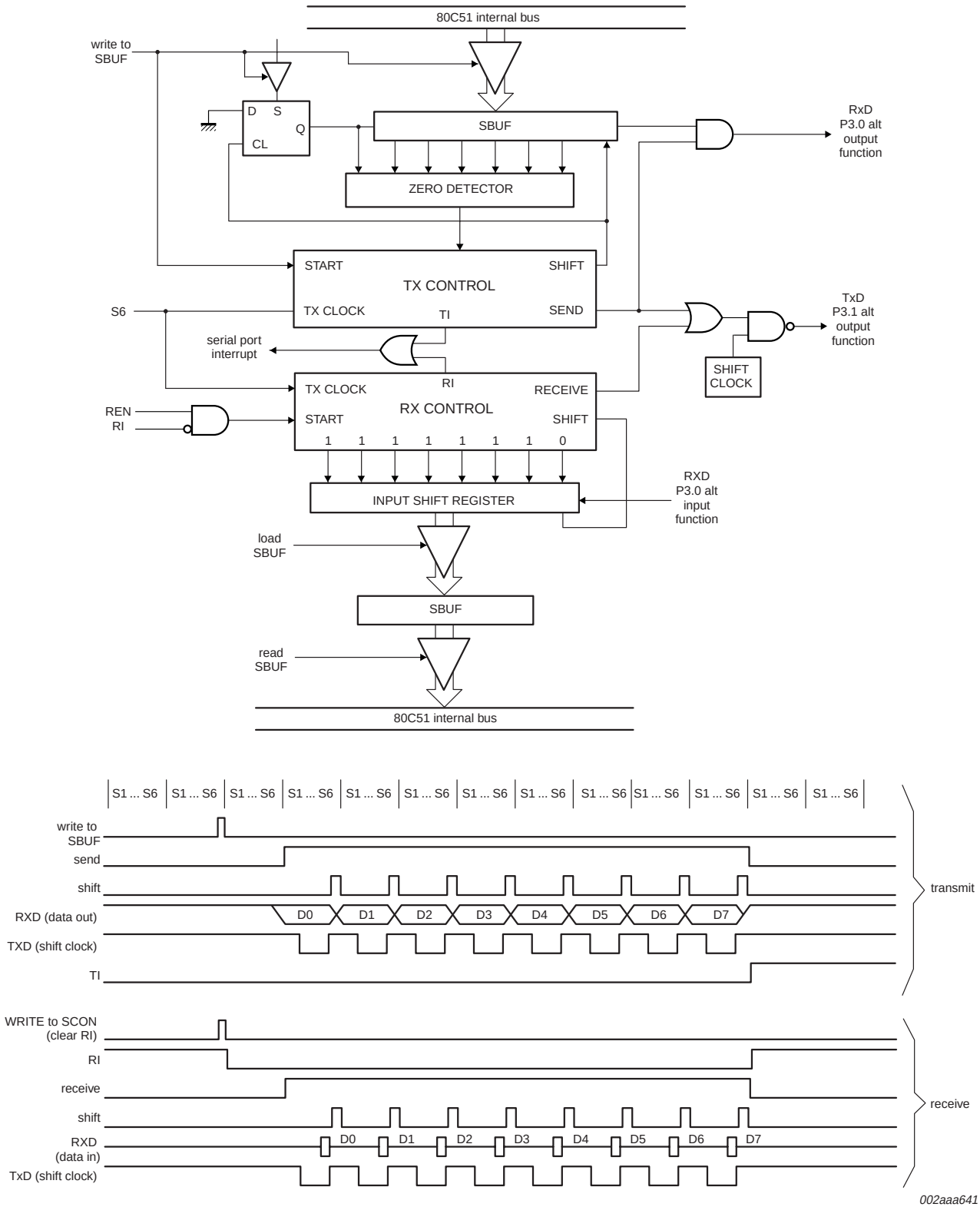


Fig 23. Serial port mode 0.

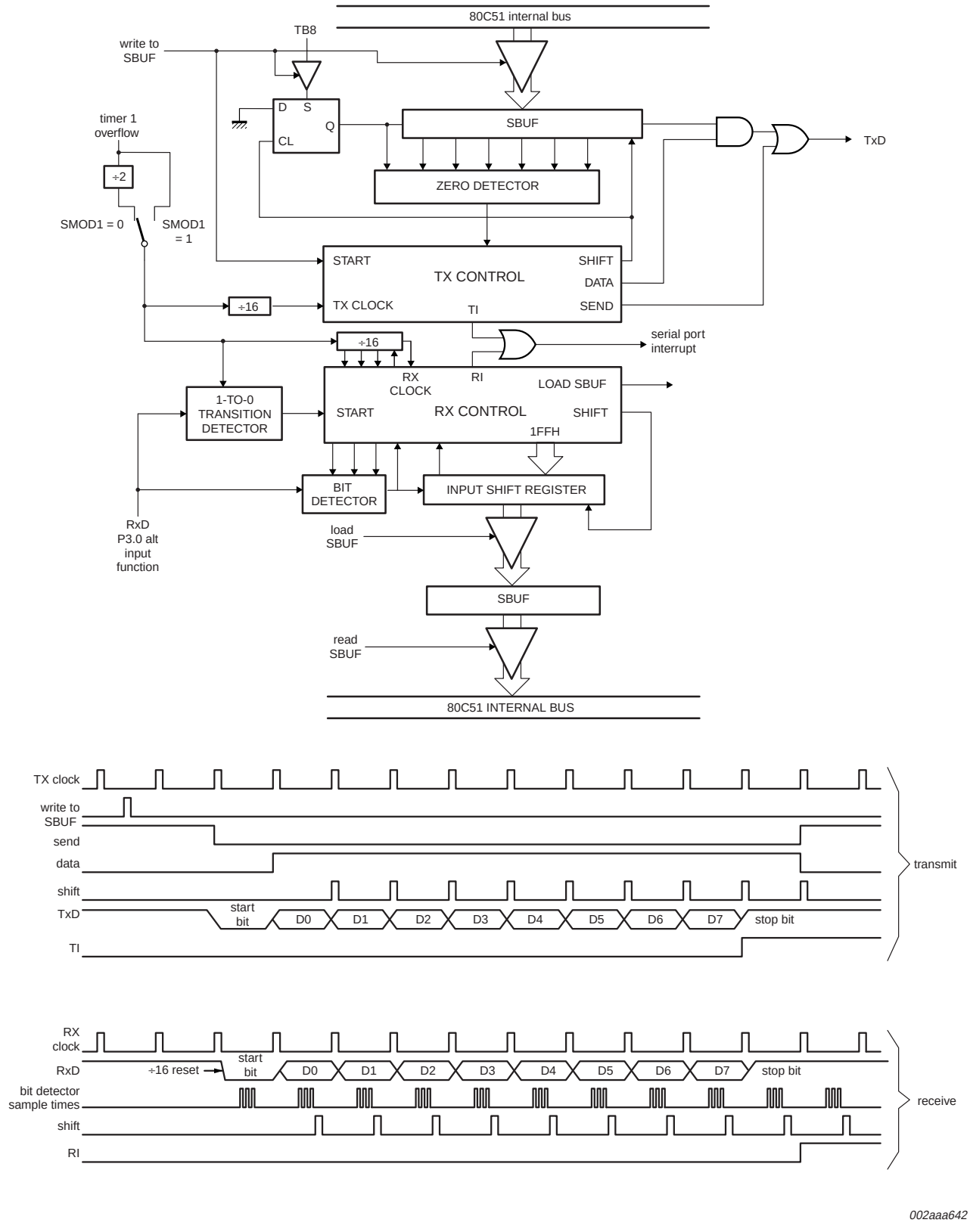


Fig 24. Serial port mode 1.

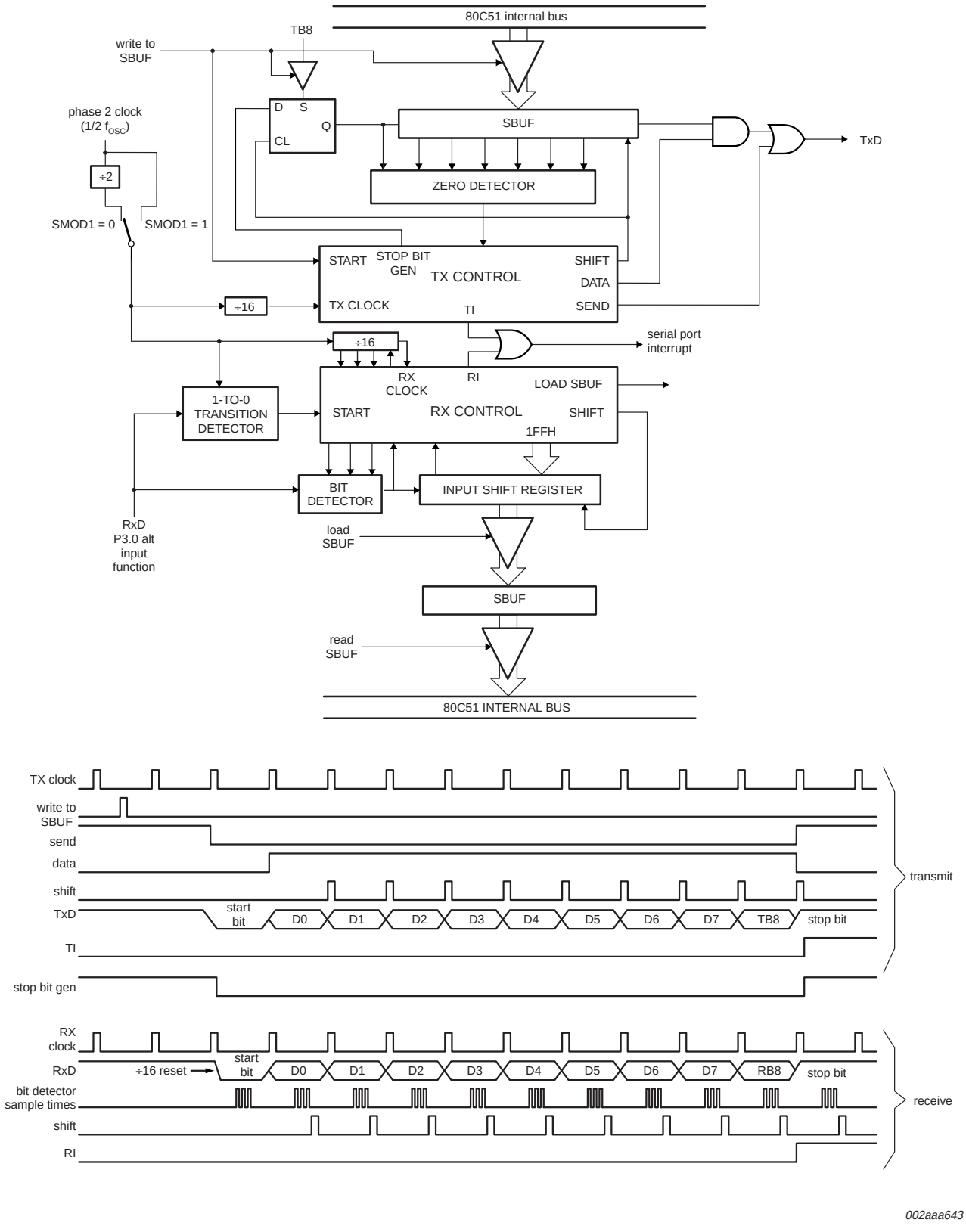


Fig 25. Serial port mode 2.

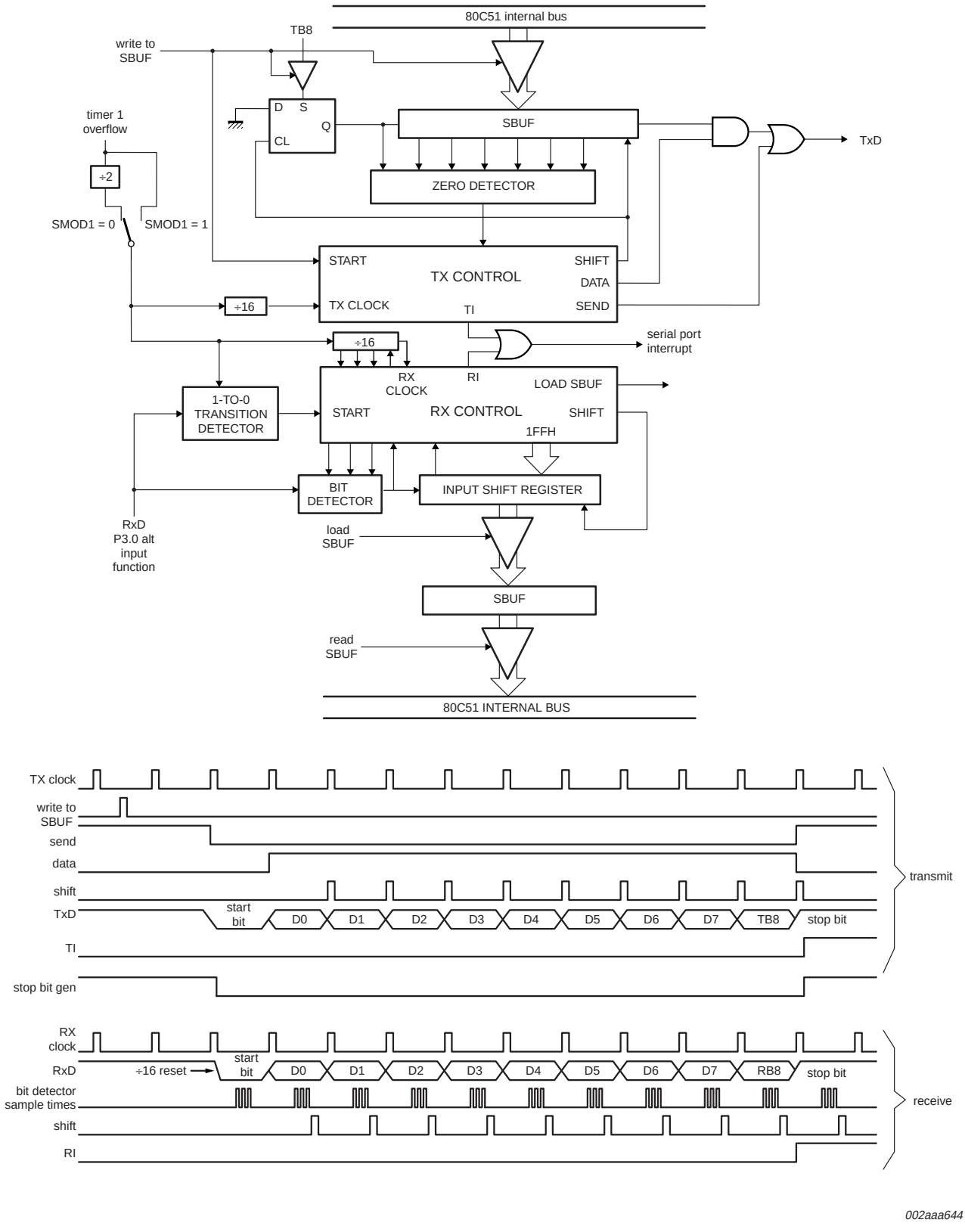


Fig 26. Serial port mode 3.

8.16 Watchdog timer

When enabled via the WDTE configuration bit, the Watchdog timer is operated from an independent, fully on-chip oscillator in order to provide the greatest possible dependability. When the Watchdog feature is enabled, the timer must be fed regularly by software in order to prevent it from resetting the CPU, and it **cannot** be turned off. When disabled as a Watchdog timer (via the WDTE bit in the UCFG1 configuration register), it may be used as an interval timer and may generate an interrupt. The Watchdog timer is shown in Figure 27.

The Watchdog timeout time is selectable from one of eight values, nominal times range from 16 milliseconds to 2.1 seconds. The frequency tolerance of the independent Watchdog RC oscillator is ±37 %. The timeout selections and other control bits are shown in Tables 43 and 44. When the Watchdog function is enabled, the WDCON register may be written **once** during chip initialization in order to set the Watchdog timeout time. The recommended method of initializing the WDCON register is to first feed the Watchdog, then write to WDCON to configure the WDS2-0 bits. Using this method, the Watchdog initialization may be done any time within 10 milliseconds after start-up without a Watchdog overflow occurring before the initialization can be completed.

Since the Watchdog timer oscillator is fully on-chip and independent of any external oscillator circuit used by the CPU, it intrinsically serves as an oscillator fail detection function. If the Watchdog feature is enabled and the CPU oscillator fails for any reason, the Watchdog timer will time out and reset the CPU.

When the Watchdog function is enabled, the timer is deactivated temporarily when a chip reset occurs from another source, such as a Power-on reset, brownout reset, or external reset.

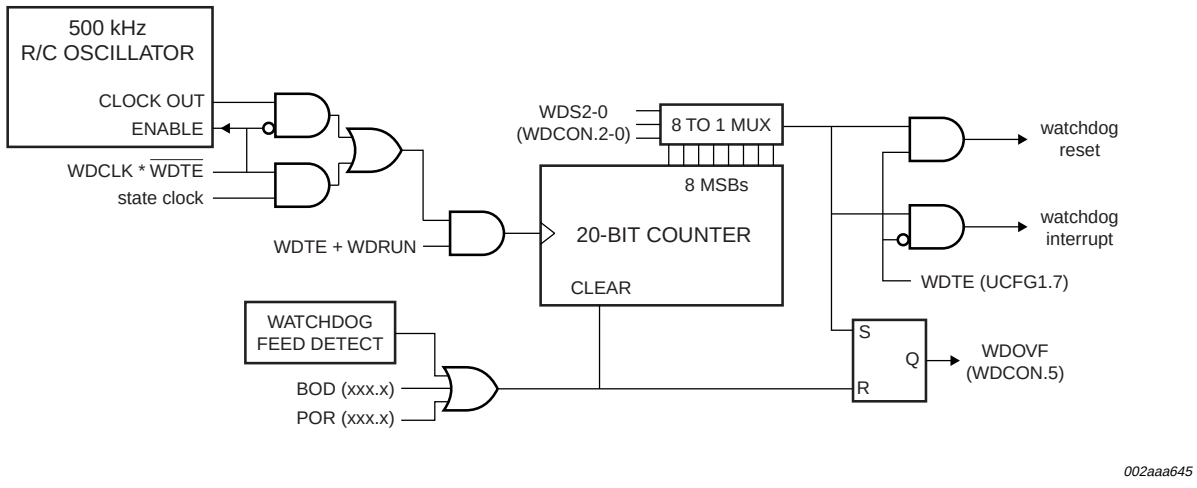


Fig 27. Block diagram of the Watchdog timer.

8.16.1 Watchdog feed sequence

If the Watchdog timer is running, it must be fed before it times out in order to prevent a chip reset from occurring. The Watchdog feed sequence consists of first writing the value 1Eh, then the value E1h to the WDRST register. An example of a Watchdog feed sequence is shown below.

```
WDFeed:
   mov   WDRST,#1eh    ; First part of Watchdog feed sequence.
   mov   WDRST,#0e1h   ; Second part of Watchdog feed sequence.
```

The two writes to WDRST do not have to occur in consecutive instructions. An incorrect Watchdog feed sequence does not cause any immediate response from the Watchdog timer, which will still time out at the originally scheduled time if a correct feed sequence does not occur prior to that time.

After a chip reset, the user program has a limited time in which to either feed the Watchdog timer or change the timeout period. When a low CPU clock frequency is used in the application, the number of instructions that can be executed before the Watchdog overflows may be quite small.

8.16.2 Watchdog reset

If a Watchdog reset occurs, the internal reset is active for approximately one microsecond. If the CPU clock was still running, code execution will begin immediately after that. If the processor was in Power-down mode, the Watchdog reset will start the oscillator and code execution will resume after the oscillator is stable.

Table 43: WDCON - Watchdog timer control register (address A7H) bit allocation

Not bit addressable; Reset value: 30H for a Watchdog reset; 10H for other reset sources if the Watchdog is enabled via the WDTE configuration bit; 00H for other reset sources if the Watchdog is disabled via the WDTE configuration bit.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	WDOVF	WDRUN	WDCLK	WDS2	WDS1	WDS0

Table 44: WDCON - Watchdog timer control register (address A7H) bit description

Bit	Symbol	Description
7, 6	-	Reserved for future use. Should not be set to ‘1’ by user programs.
5	WDOVF	Watchdog timer overflow flag. Set when a Watchdog reset or timer overflow occurs. Cleared when the Watchdog is fed.
4	WDRUN	Watchdog run control. The Watchdog timer is started when WDRUN = 1 and stopped when WDRUN = 0. This bit is forced to ‘1’ (Watchdog running) if the WDTE configuration bit = 1.
3	WDCLK	Watchdog clock select. The Watchdog timer is clocked by CPU clock / 6 when WDCLK = 1 and by the Watchdog RC oscillator when WDCLK = 0. This bit is forced to ‘0’ (using the Watchdog RC oscillator) if the WDTE configuration bit = 1.
2-0	WDS2-0	Watchdog rate select.

Table 45: Watchdog rate select clock time

WDS2-0	Timeout clocks	Minimum time	Nominal time	Maximum time
0 0 0	8,192	10 ms	16 ms	23 ms
0 0 1	16,384	20 ms	32 ms	45 ms
0 1 0	32,768	41 ms	65 ms	90 ms
0 1 1	65,536	82 ms	131 ms	180 ms
1 0 0	131,072	165 ms	262 ms	360 ms
1 0 1	262,144	330 ms	524 ms	719 ms
1 1 0	524,288	660 ms	1.05 sec	1.44 sec
1 1 1	1,048,576	1.3 sec	2.1 sec	2.9 sec

8.17 Additional features

The AUXR1 register contains several special purpose control bits that relate to several chip features. AUXR1 is described in Tables 46 and 47.

Table 46: AUXR1 - AUXR1 register (address A2H) bit allocation

Not bit addressable; Reset value: 00H

Bit	7	6	5	4	3	2	1	0
Symbol	KBF	BOD	BOI	LPEP	SRST	0	-	DPS

Table 47: AUXR1 - AUXR1 register (address A2H) bit description

Bit	Symbol	Description
7	KBF	Keyboard Interrupt Flag. Set when any pin of port 0 that is enabled for the Keyboard Interrupt function goes LOW. Must be cleared by software.
6	BOD	Brown Out Disable. When set, turns off brownout detection and saves power. See Section 8.11 “Power monitoring functions” on page 37 for details.
5	BOI	Brown Out Interrupt. When set, prevents brownout detection from causing a chip reset and allows the brownout detect function to be used as an interrupt. See Section 8.11 “Power monitoring functions” on page 37 for details.
4	LPEP	Low Power EPROM control bit. Allows power savings in low voltage systems. Set by software. Can only be cleared by Power-on or brownout reset. See Section 8.12 “Power reduction modes” on page 38 for details.
3	SRST	Software Reset. When set by software, resets the P87LPC779 as if a hardware reset occurred.
2	0	This bit contains a hard-wired 0. Allows toggling of the DPS bit by incrementing AUXR1, without interfering with other bits in the register.
1	-	Reserved for future use. Should not be set to ‘1’ by user programs.
0	DPS	Data Pointer Select. Chooses one of two Data Pointers for use by the program. See text for details.

8.17.1 Software reset

The SRST bit in AUXR1 allows software the opportunity to reset the processor completely, as if an external reset or Watchdog reset had occurred. If a value is written to AUXR1 that contains a '1' at bit position 3, all SFRs will be initialized and execution will resume at program address 0000. Care should be taken when writing to AUXR1 to avoid accidental software resets.

8.17.2 Dual data pointers

The dual Data Pointer (DPTR) adds to the ways in which the processor can specify the address used with certain instructions. The DPS bit in the AUXR1 register selects one of the two Data Pointers. The DPTR that is not currently selected is not accessible to software unless the DPS bit is toggled.

Specific instructions affected by the Data Pointer selection are:

- INC DPTR: Increments the Data Pointer by 1.
- JMP @A+DPTR: Jump indirect relative to DPTR value.
- MOV DPTR, #data16: Load the Data Pointer with a 16-bit constant.
- MOVCA, @A+DPTR: Move code byte relative to DPTR to the accumulator.
- MOVXA, @DPTR: Move data byte the accumulator to data memory relative to DPTR.
- MOVX @DPTR, A: Move data byte from data memory relative to DPTR to the accumulator.

Also, any instruction that reads or manipulates the DPH and DPL registers (the upper and lower bytes of the current DPTR) will be affected by the setting of DPS. The MOVX instructions have limited application for the P87LPC779 since the part does not have an external data bus. However, they may be used to access EPROM configuration information (see Section 8.18 "EPROM characteristics").

Bit 2 of AUXR1 is permanently wired as a logic 0. This is so that the DPS bit may be toggled (thereby switching Data Pointers) simply by incrementing the AUXR1 register, without the possibility of inadvertently altering other bits in the register.

8.18 EPROM characteristics

Programming of the EPROM on the P87LPC779 is accomplished with a serial programming method. Commands, addresses, and data are transmitted to and from the device on two pins after programming mode is entered. Serial programming allows easy implementation of in-circuit programming of the P87LPC779 in an application board.

The P87LPC779 contains three signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes designate the device as an P87LPC779 manufactured by Philips. The signature bytes may be read by the user program at addresses FC30h, FC31h and FC60h with the MOVC instruction, using the DPTR register for addressing.

A special user data area is also available for access via the MOVC instruction at addresses FCE0h through FCFFh. This 'customer code' space is programmed in the same manner as the main code EPROM and may be used to store a serial number, manufacturing date, or other application information.

8.18.1 System configuration bytes

A number of user configurable features of the P87LPC779 must be defined at power up and therefore cannot be set by the program after start of execution. Those features are configured through the use of two EPROM bytes that are programmed in the same manner as the EPROM program space. The contents of the two configuration bytes, UCFG1 and UCFG2, are shown in Tables 48, 49, 51 and 52. The values of these bytes may be read by the program through the use of the MOVX instruction at the addresses shown in the tables.

Table 48: UCFG1 - EPROM system configuration byte 1 register (address FD00H) bit allocation

Unprogrammed value: FFH

Bit	7	6	5	4	3	2	1	0
Symbol	WDTE	RPD	PRHI	BOV	CLKR	FOSC2	FOSC1	FOSC0

Table 49: UCFG1 - EPROM system configuration byte 1 register (address FD00H) bit description

Bit	Symbol	Description
7	WDTE	Watchdog timer enable. When programmed (0), disables the Watchdog timer. The timer may still be used to generate an interrupt.
6	RPD	Reset pin disable. When programmed (0), disables the reset function of pin P1.5, allowing it to be used as an input only port pin.
5	PRHI	Port reset high. When '1', ports reset to a high state. When '0', ports reset to a low state.
4	BOV	Brownout voltage select. When '1', the brownout detect voltage is 2.5 V. When '0', the brownout detect voltage is 3.8 V. This is described in Section 8.11 "Power monitoring functions" on page 37.
3	CLKR	Clock rate select. When '0', the CPU clock rate is divided by 2. This results in machine cycles taking 12 CPU clocks to complete as in the standard 80C51. For full backward compatibility, this division applies to peripheral timing as well.
2 to 0	FOSC[2:0]	CPU oscillator type select. See Section 8.10 "Oscillator" on page 34 for additional information. Combinations other than those shown below should not be used. They are reserved for future use.

Table 50: FOSC2-FOSC0 oscillator configuration

FOSC2-FOSC0	Oscillator configuration
1 1 1	External clock input on X1 (default setting for an unprogrammed part).
0 1 1	Internal RC oscillator, 6 MHz.

Table 50: FOSC2-FOSC0 oscillator configuration...*continued*

FOSC2-FOSC0	Oscillator configuration
0 1 0	Low frequency crystal, 20 kHz to 100 kHz.
0 0 1	Medium frequency crystal or resonator, 100 kHz to 4 MHz.
0 0 0	High frequency crystal or resonator, 4 MHz to 20 MHz.

Table 51: UCFG2 - EPROM system configuration byte 2 register (address FD01H) bit allocation

Unprogrammed value: FFH

Bit	7	6	5	4	3	2	1	0
Symbol	SB2	SB1	-	-	-	-	-	-

Table 52: UCFG2 - EPROM system configuration byte 2 register (address FD01H) bit description

Bit	Symbol	Description
7, 6	SB2, SB1	EPROM security bits. See Table 53 for details.
5-0	-	Reserved for future use.

8.18.2 Security bits

When neither of the security bits are programmed, the code in the EPROM can be verified. When only security bit 1 is programmed, all further programming of the EPROM is disabled. At that point, only security bit 2 may still be programmed. When both security bits are programmed, EPROM verify is also disabled.

Table 53: EPROM security bits

SB2	SB1	Protection description
1	1	Both security bits unprogrammed. No program security features enabled. EPROM is programmable and verifiable.
1	0	Only security bit 1 programmed. Further EPROM programming is disabled. Security bit 2 may still be programmed.
0	1	Only security bit 2 programmed. This combination is not supported.
0	0	Both security bits programmed. All EPROM verification and programming are disabled.

9. Limiting values

Table 54: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{amb(bias)}$	operating bias ambient temperature		–55	+85	°C
T_{stg}	storage temperature range		–65	+150	°C
V_{RST}	voltage on $\overline{RST}/V_{PP}$ pin to V_{SS}		-	+11.0	V
V_n	voltage on any other pin to V_{SS}		–0.5	V_{DD} + 0.5	V
$I_{OL(I/O)}$	LOW-level output current per I/O pin		-	50	mA
$I_{OH(I/O)}$	HIGH-level output current per I/O pin		-	–50	mA
$I_{OL(tot)(max)}$	maximum total I_{OL} for all outputs		-	200	mA
$I_{OH(tot)(max)}$	maximum total I_{OH} for all outputs		-	–200	mA
$P_{tot(pack)}$	total power dissipation per package	based on package heat transfer, not device power consumption	-	1.5	W

[1] Stresses above those listed under Table 54 “Limiting values” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in Table 55 “DC electrical characteristics” and Table 57 “AC electrical characteristics” of this specification are not implied.

[2] This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

[3] Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

10. Static characteristics

Table 55: DC electrical characteristics

V_{DD} = 2.7 V to 5.5 V unless otherwise specified.
T_{amb} = –40 °C to +85 °C for extended industrial, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{DD}	power supply current, operating	5.0 V; 20 MHz	[10]	-	15	25	mA
		3.0 V; 10 MHz	[10]	-	4	7	mA
I_{ID}	power supply current, Idle mode	5.0 V; 20 MHz	[10]	-	6	10	mA
		3.0 V; 10 MHz	[10]	-	2	4	mA
I_{PD}	Power supply current, Power-down mode	5.0 V	[10]	-	1	10	µA
		3.0 V	[10]	-	1	5	µA
V_{RAM}	RAM keep-alive voltage			1.5	-	-	V
V_{IL}	Low-level input voltage (TTL input)	4.5 V < V_{DD} < 6.0 V		–0.5	-	$0.2V_{DD}$ – 0.1	V
V_{IL1}	negative-going threshold (Schmitt input)			–0.5	-	$0.3V_{DD}$	V
V_{IH}	High-level input voltage (TTL input)			$0.2V_{DD}$ + 0.9	-	V_{DD} + 0.5	V
V_{IH1}	positive-going threshold (Schmitt input)			$0.7V_{DD}$	-	V_{DD} + 0.5	V
V_{hys}	hysteresis voltage			-	$0.2V_{DD}$	-	V
V_{OL}	LOW-level output voltage; all ports[4][8]	I_{OL} = 3.2 mA; V_{DD} = 4.5 V		-	-	0.4	V
V_{OL1}	LOW-level output voltage; all ports[4][8]	I_{OL} = 20 mA; V_{DD} = 4.5 V		-	-	1.0	V
V_{OH}	HIGH-level output voltage, all ports[2]	I_{OH} = –30 µA; V_{DD} = 4.5 V		V_{DD} – 0.7	-	-	V
V_{OH1}	HIGH-level output voltage, all ports[3]	I_{OH} = –1.0 mA; V_{DD} = 4.5 V		V_{DD} – 0.7	-	-	V
C_{io}	input/output pin capacitance[9]			-	-	15	pF
I_{IL}	logic 0 input current, all ports[7]	V_{IN} = 0.4 V		-	-	–50	µA
I_{LI}	input leakage current, all ports[6]	V_{IN} = V_{IL} or V_{IH}		-	-	±2	µA
I_{TL}	logic 1-to-0 transition current, all ports[2][5]	V_{IN} = 2.0 V at V_{DD} = 5.5 V		–150	-	–650	µA
R_{RST}	internal reset pull-up resistor			40	-	225	kΩ

Table 55: DC electrical characteristics *...continued*

V_{DD} = 2.7 V to 5.5 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for extended industrial, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{BOLOW}	brownout trip voltage with BOV = 1[11]		2.35	-	2.69	V
V_{BOHI}	brownout trip voltage with BOV = 0[12]		3.45	3.8	3.99	V
V_{REF}	bandgap reference voltage		1.11	1.26	1.41	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature, 5 V.

[2] Ports in quasi-bidirectional mode with weak pull-up (applies to all port pins with pull-ups). Does not apply to open-drain pins.

[3] Ports in PUSH-PULL mode. Does not apply to open drain pins.

[4] In all output modes except high impedance mode.

[5] Port pins source a transition current when used in quasi-bidirectional mode and externally driven from '1' to '0'. This current is highest when V_{IN} is approximately 2 V.

[6] Measured with port in high-impedance mode. Parameter is guaranteed, but not tested at cold temperature.

[7] Measured with port in quasi-bidirectional mode.

[8] Under steady state (non-transient conditions, I_{OL} must be externally limited as follows.

a) Maximum I_{OL} per port pin: 20 mA

b) Maximum I_{OL} for all outputs: 80 mA

c) Maximum I_{OL} for all outputs: 5 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

[9] Pin capacitance is characterized but not tested.

[10] The I_{DD}, I_{ID}, and I_{PD} specifications are measured using an external clock with the following functions disabled: comparators, brownout detect, and Watchdog timer. For V_{DD} = 3 V, LPEP = 1. Refer to the appropriate figure on the following pages for additional current drawn by each of these functions.

[11] Devices initially operating at V_{DD} = 2.7 V or above and f_{osc} = 10 MHz or less are guaranteed to continue to execute instructions correctly at the brownout trip point. Initial power-on operation below V_{DD} = 2.7 V is not guaranteed.

[12] Devices initially operating at V_{DD} = 4.0 V or above and f_{osc} = 20 MHz or less are guaranteed to continue to execute instructions correctly at the brownout trip point. Initial power-on operation below V_{DD} = 4.0 V and f_{osc} > 10 MHz is not guaranteed

Table 56: A/D converter DC electrical characteristics

V_{DD} = 2.7 V to 5.5 V unless otherwise specified.

T_{amb} = −40 °C to +85 °C for extended industrial, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
AV_{IN}	Analog input voltage		V_{SS} − 0.2	V_{DD} + 0.2	V
C_{IA}	Analog input capacitance		-	15	pF
DL_e	Differential non-linearity[1][2][3]		-	±1	LSB
IL_e	Integral non-linearity[1][4]		-	±1	LSB
OS_e	Offset error[1][5]		-	±1	LSB
G_e	Gain error[1][6]		-	±0.4	%
A_e	Absolute voltage error[1][7]		-	±1	LSB
M_{CTC}	Channel-to-channel matching		-	±1	LSB
C_t	Crosstalk between inputs of port[8]	0 to 100 kHz	-	−60	dB
-	Input slew rate		-	100	V/ms
-	Input source impedance		-	10	kΩ

[1] Conditions: V_{SS} = 0 V; V_{DD} = 5.12 V.

[2] The A/D is monotonic, there are no missing codes.

[3] The differential non-linearity (DL_e) is the difference between the actual step width and the ideal step width. See Figure 28.

[4] The integral non-linearity (IL_e) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 28.

[5] The offset error (OS_e) is the absolute difference between the straight line which fits the actual transfer curve (after removing gain error), and the straight line which fits the ideal transfer curve. See Figure 28.

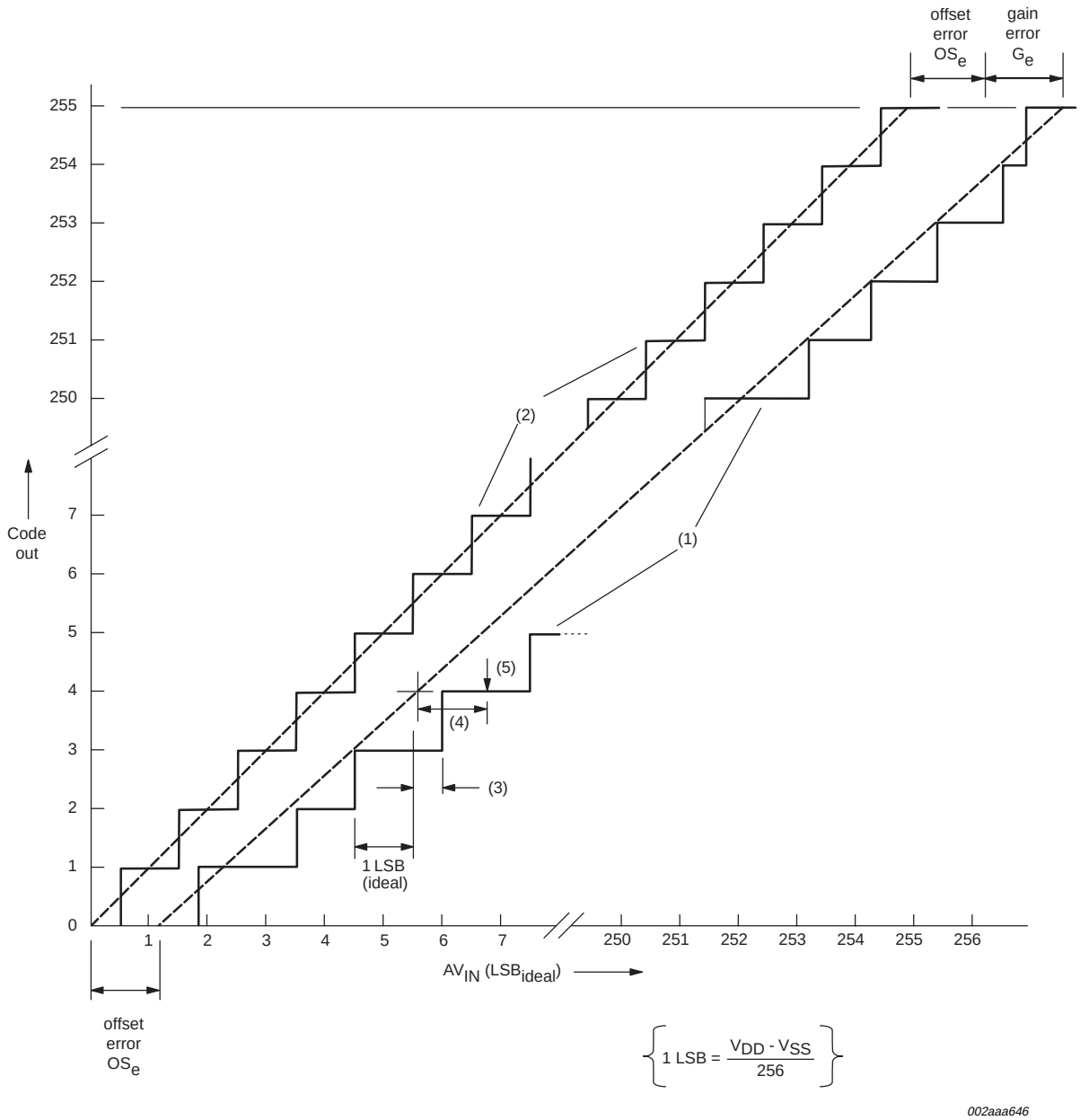
[6] The gain error (G_e) is the relative difference in percent between the straight line fitting the actual transfer curve (after removing offset error), and the straight line which fits the ideal transfer curve. Gain error is constant at every point on the transfer curve. See Figure 28.

[7] The absolute voltage error (A_e) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve.

[8] This should be considered when both analog and digital signals are input simultaneously to A/D pins.

[9] Changing the input voltage faster than this may cause erroneous readings.

[10] A source impedance higher than this driving an A/D input may result in loss of precision and erroneous readings.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential non-linearity (DL_e).

(4) Integral non-linearity (IL_e).

(5) Center of a step of the actual transfer curve.

Fig 28. A/D conversion characteristics.

11. Dynamic characteristics

Table 57: AC electrical characteristics

V_{DD} = 2.7 V to 5.5 V unless otherwise specified; V_{SS} = 0 V.[1][2][3]
T_{amb} = −40 °C to +85 °C for extended industrial, unless otherwise specified.

Symbol	Figure	Parameter		Min	Max	Unit
External Clock						
f_C	30	Oscillator frequency (V_{DD} = 4.0 V to 6.0 V)		0	20	MHz
f_C	30	Oscillator frequency (V_{DD} = 2.7 V to 6.0 V)		0	10	MHz
t_C	30	Clock period and CPU timing cycle		$1/f_C$	-	ns
t_{CLCX}	30	Clock low-time[1]	f_{osc} = 20 MHz	20	-	ns
t_{CLCX}	30		f_{osc} = 10 MHz	40	-	ns
t_{CHCX}	30	Clock high time[1]	f_{osc} = 20 MHz	20	-	ns
t_{CHCX}	30		f_{osc} = 10 MHz	40	-	ns
Internal RC Oscillator						
f_{CCAL}		On-chip oscillator calibration[2]	f_{RCOSC} = 6 MHz	−1	+1	%
f_{CTOL}		On-chip oscillator tolerance[3][4]	f_{RCOSC} = 6 MHz	−2.5	+2.5	%
f_{CTOL1}		On-chip oscillator tolerance[3]	f_{RCOSC} = 6 MHz	−25	+25	%
Shift Register						
t_{XLXL}	29	Serial port clock cycle time		$6t_C$	-	ns
t_{QVXH}	29	Output data setup to clock rising edge		$5t_C - 133$	-	ns
t_{XHQX}	29	Output data hold after clock rising edge		$1t_C - 80$	-	ns
t_{XHDV}	29	Input data setup to clock rising edge		-	$5t_C - 133$	ns
t_{XHDX}	29	Input data hold after clock rising edge		0	-	ns

[1] Applies only to an external clock source, not when a crystal is connected to the X1 and X2 pins.
[2] Tested at V_{DD} = 5.0 V and room temperature.
[3] These parameters are characterized but not tested.
[4] These parameters are for 0 °C to +70 °C

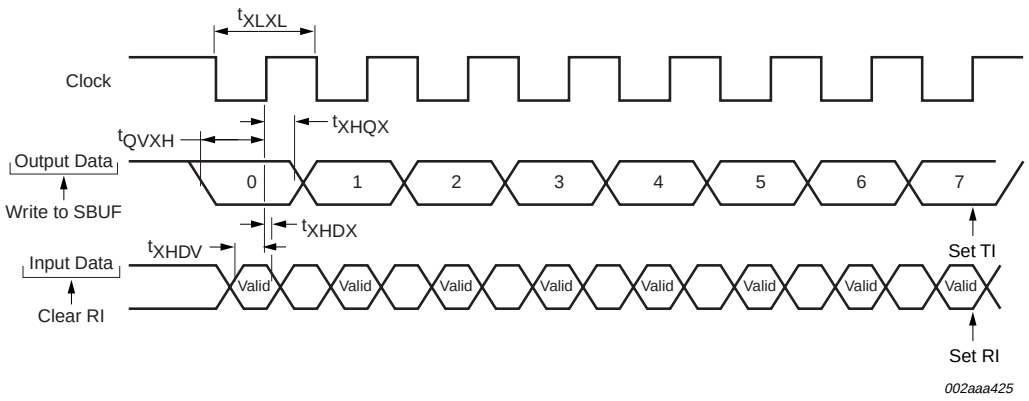


Fig 29. Shift register mode timing.

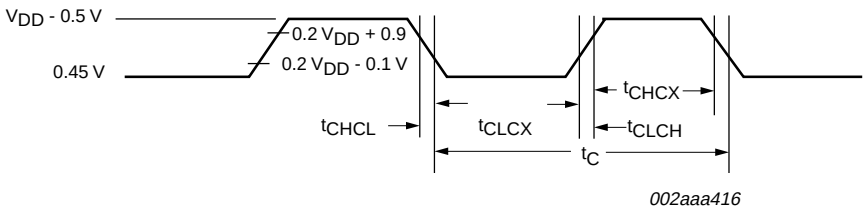


Fig 30. External clock timing.

12. Comparator electrical characteristics

Table 58: Comparator electrical characteristics

V_{DD} = 2.7 V to 5.5 V unless otherwise specified.
T_{amb} = –40 °C to +85 °C for extended industrial, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{IO}	Offset voltage comparator inputs[1]		-	-	±10	mV
V_{CR}	Common mode range comparator inputs		0	-	V_{DD} – 0.3	V
CMRR	Common mode rejection ratio[1]		-	-	–50	dB
	Response time		-	250	500	ns
	Comparator enable to output valid		-	-	10	µs
I_{IL}	Input leakage current, comparator	$0 < V_{IN} < V_{DD}$	-	-	±10	µA

[1] This parameter is characterized, but not tested in production.

13. D/A electrical characteristics

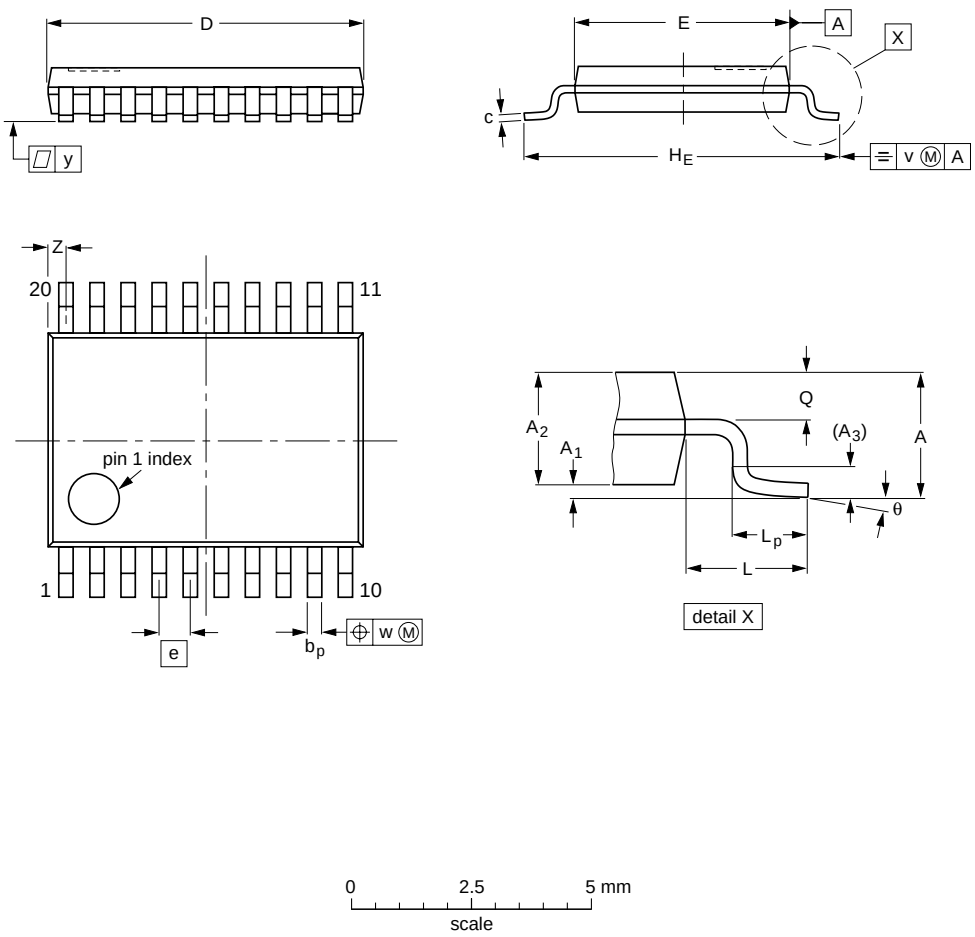
Table 59: D/A electrical characteristics

V_{DD} = 2.7 V to 5.5 V unless otherwise specified.
T_{amb} = –40 °C to +85 °C for extended industrial, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Analog output						
V_{OA}	output voltage	no resistive load	V_{SS}	-	V_{DD}	V
		R_L = 100 k	$0.975 \times V_{DD}$	-	V_{DD}	V
		R_L = 10 k	$0.9 \times V_{DD}$	-	V_{DD}	V
$t_{DACrise}$	rise time 10 % to 90 % V_{DD}	no load	-	100	-	ns
		C_L = 100 pF	-	500	-	ns
$t_{DACfall}$	fall time 90 % to 10 % V_{DD}	no load	-	80	-	ns
		C_L = 100 pF	-	500	-	ns

14. Package outline

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 31. SOT360-1.

15. Revision history

Table 60: Revision history

Rev	Date	CPCN	Description
02	20040503	-	**Product data (9397 750 13213)** Modifications: • Section 2 “Features” on page 1; adjusted text “28-bit Digital to Analog Converter” to “Two 8-bit Digital to Analog Converters”.
01	20040405	-	**Product data (9397 750 12976)**

16. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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