



STAC9766 and STAC9750 Crystal Elimination Circuit Use and Implementation for Motherboards

SigmaTel Application Note

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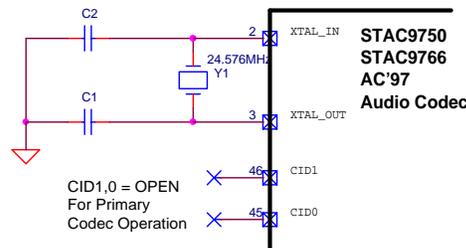


The STAC9766 and STAC9750 incorporate an internal crystal elimination circuit that allows the standard 24.576 MHz AC'97 external crystal to be eliminated from motherboard applications. This document describes the normal "crystal installed" mode of operation, as well as the "crystal eliminated" mode.

NORMAL CRYSTAL CONFIGURATION

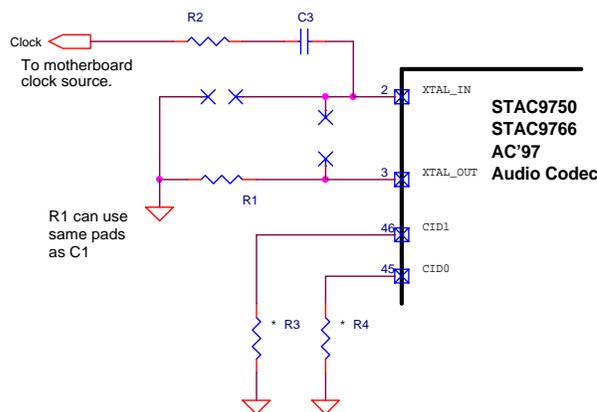
The 24.576 MHz frequency is not typically available on motherboards, and is usually generated by an external crystal connected directly to the audio codec. The frequency was originally selected because of the simple relationship between 44.1 kHz audio and 48 kHz audio data streams. In the normal mode with the crystal installed, the crystal is connected to the XTALin and XTALout pins of the codec. Capacitors C1 and C2 are connected at either side of the crystal for stability and lower EMI emissions.

The CID1 and CID0 pins (pins 45 and 46) of the codec are used to select the codec ID, which is 0 for primary codecs, and 1, 2, or 3 for secondary codecs. For motherboard codecs, the CID pins are normally left open and the codec is assigned the primary 0 ID automatically.



CRYSTAL ELIMINATION MODE

The crystal elimination mode is automatically entered when the XTALout pin is grounded. In this mode the codec will accept an external clock source from the motherboard. The expected frequencies are: 48 MHz that is related to the USB clocks, 27 MHz that is related to digital video systems, or 14.31818 MHz that is a former graphics card clock but still used on most motherboards today. A 24.576 MHz clock may also be used in both normal mode, and crystal elimination mode.





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The CID pull-down resistors (R3 and R4) should be installed according to the table below to indicate which frequency is used. The C1 surface mount pads can be used for the shorting resistor on XTALout, or another component can be added to the schematic as an assembly option. The clock ac-coupling capacitor can range from 0.1 uF to 0.01 uF and a series resistor can be added to reduce any EMI issues. If the resistor is added, it should generally be located closer to the clock source for best results.

Clock Source at XTALin	R3 for CID1	R4 for CID0	Codec Status
48 MHz	1K	Open	Primary, ID = 0
27 MHz	Open	1K	Primary, ID = 0
14.31818 MHz	Open	Open	Primary, ID = 0
24.576 MHz	1K	1K	Primary, ID = 0

Note: XTALout must be shorted to ground in this mode

Note: Clock source configurations are different for CA1 and CA2 revisions.

The STAC9766/67 and STAC9750/51 datasheets, product briefs and additional information is available at www.sigmatel.com