Read / Write amplifier for FDD

BH6626FS

The BH6626FS is a read / write IC designed for floppy disk drives and has an internal active filter for memory systems in which saddle margins are important. Any of multiple write current settings can be selected, and both density switching and inner track / outer track switching are done internally.

●Applications

Floppy disc drives (1MB and 2MB)

●Features

1) Active filter switched internally.
2) Time domain filter with internal switch set according to transfer rate.
3) Density switching and inner track / outer track switching are done internally.

●Absolute maximum ratings (unless otherwise noted, Ta = 25°C)

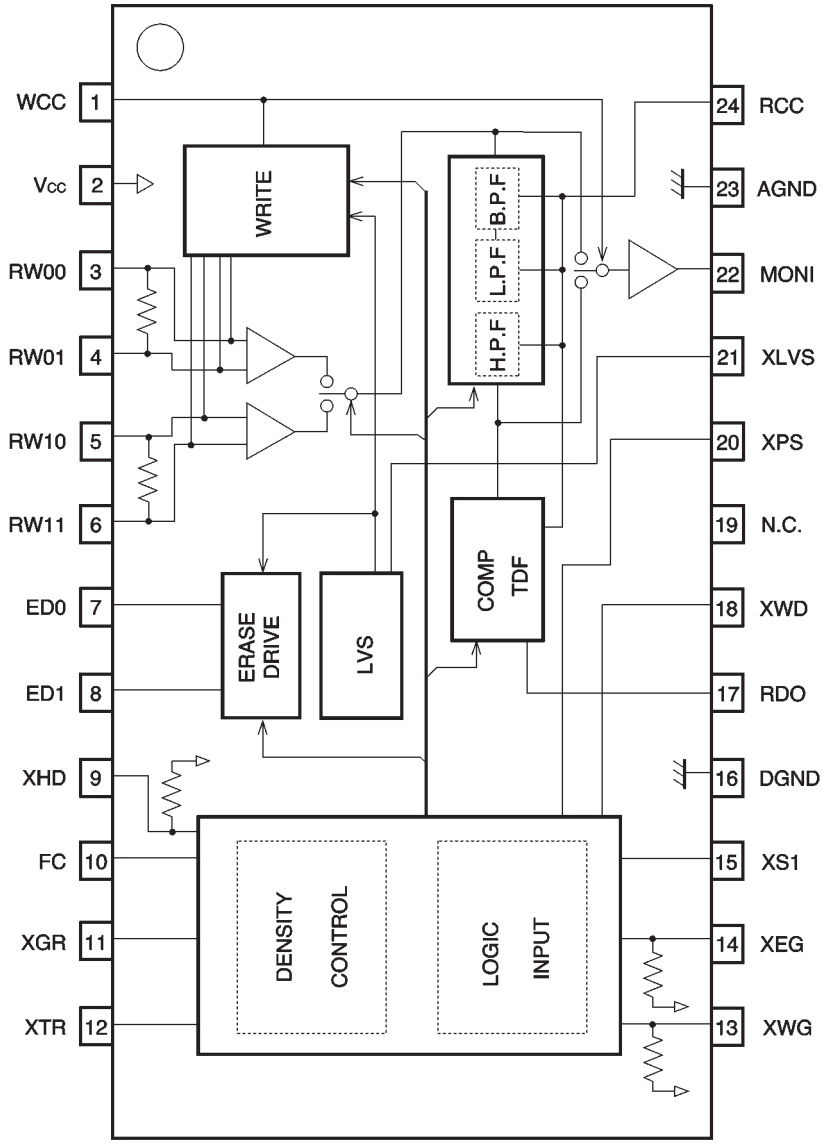
Parameter	Symbol	Limits	Unit
Power supply voltage	Vcc	+7	V
Operating temperature	Topr	0～+70	℃
Storage temperature	Tstg	−55～+125	℃
Digital input voltage	VI	−0.5～Vcc+0.3	V
RW pin voltage	VRW	+15	V
LVS output voltage	VLVS	Vcc+0.3	V
ED pin voltage	VER	Vcc+0.3	V
Power dissipation	Pd	650*	mW

* Reduced by 6.5mW for each increase in Ta of 1℃ over 25℃.

●Recommended operating conditions

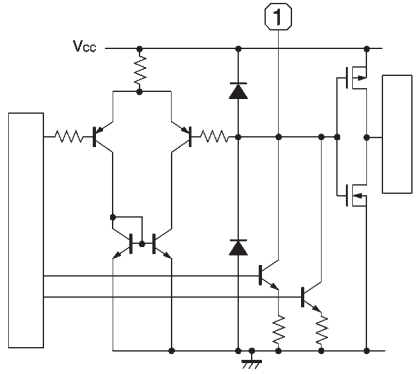
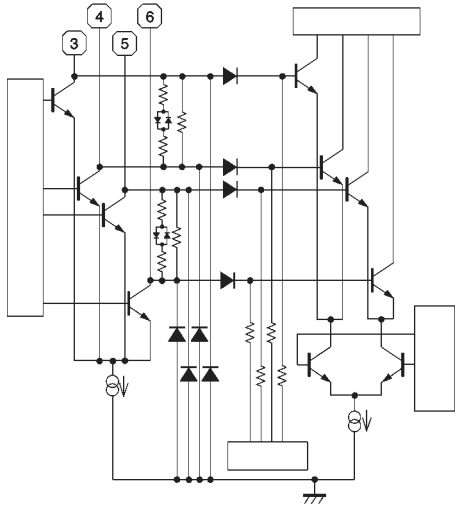
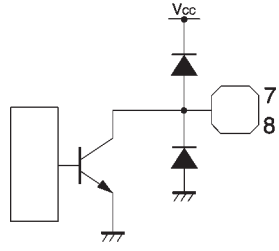
Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	Vcc	4.5	5.0	5.5	V

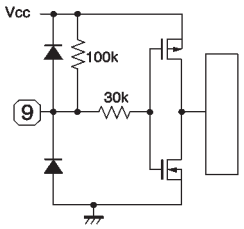
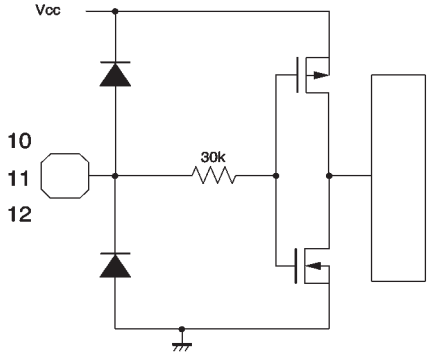
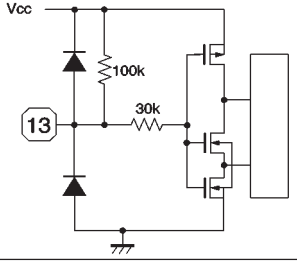
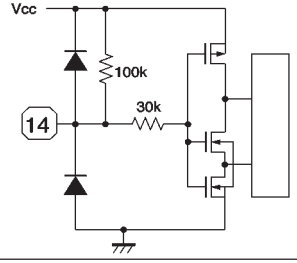
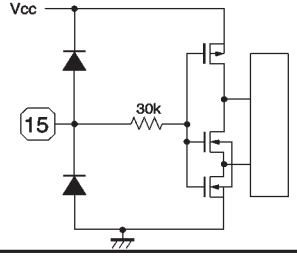
●Block diagram

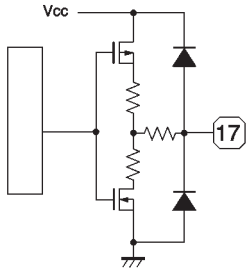
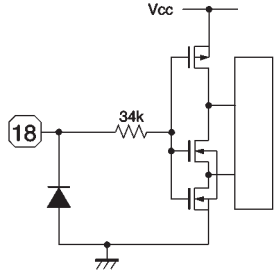
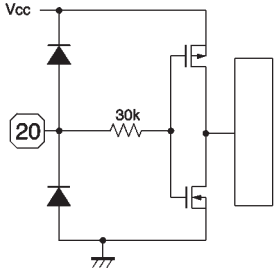


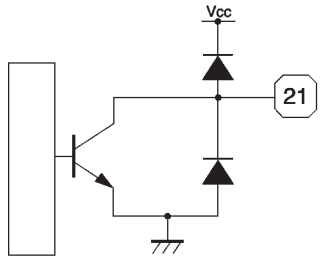
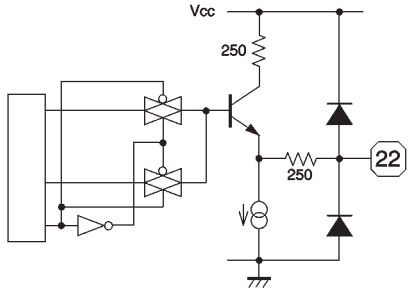
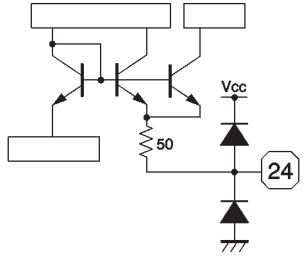
(Note) Use a short pattern for Vcc, and keep the impedance between Vcc and GND low by inserting a bypass capacitor.

●Pin descriptions and Input / output circuits

Pin No.	Pin name	Equivalent circuit	Function
1	WCC		For connecting the write current adjustment resistor Connect the write current adjustment resistor between this pin and Vcc Setting this pin to the low level during reading switches MONI to differentiator output
2	Vcc		Power supply pin
3	RW00		Active when SIDE0 and the read/write head connecting pin (pin 15, XS1) is at the high level (side 0) Starts at RW00 during the start of writing (from reading to writing)
4	RW01		
5	RW10		Active when the read / write head connecting pin (pin 15, XS1) is at the low level (side 1) Starts at RW10 during the start of writing (from reading to writing)
6	RW11		
7	ED0		Side 0 erase current sink
8	ED1		Side 1 erase current sink

Pin No.	Pin name	Equivalent circuit	Function
9	XHD		1 MB / 2 MB selector High = 1 MB Low = 2 MB
10	FC		Option 2 selector Selector signal high level = active
11	XGR		Option mode selector Controls the write current
12	XTR		Inner edge / outer track position setting Controls the filter and write current
13	XWG		Write enable gate (Schmidt input) Low = active
14	XEG		Erase enable gate (Schmidt input) Low = active
15	XS1		Head / side switching signal Low = active (Schmidt input) High = side 0, low = side 1

Pin No.	Pin name	Equivalent circuit	Function
16	DGND		Digital ground
17	RDO		Read data output TTL high level = active
18	XWD		Write data input Operates at falling edge (Schmidt input)
19	N.C.		
20	XPS		Power save selector Low level = active

Pin No.	Pin name	Equivalent circuit	Function
21	XLVS		External low level voltage detection pin Open collector output when low level voltage is detected Switches to low level when Vcc drops below the specified voltage
22	MONI		Preamplifier output and differentiator output monitoring Monitor is switched with pin 1 (WCC)
23	AGND		Analog ground
24	RCC		Filter (LPF,BPF) cutoff frequency and TDF 1st M/M pulse width setting resistor connection

●Electrical characteristics (unless otherwise noted, Ta = 25°C, V_{CC} = 5V)

Supply current

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Current dissipation,Standby	ICCST	—	190	400	μA	∗1
Current dissipation,Read	ICCR	—	28	40	mA	∗1
Current dissipation,Write	ICCW	—	8.5	15	mA	∗2

∗1 RRCC=2.0 [kΩ] (XHD=H)
∗2 RWCC=2.4 [kΩ] (When 2MB inner edge, XGR=high level, excluding IWR and IER)

Low level voltage detection circuit

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Threshold voltage 1	VTH1+	—	4.05	4.3	V	When supply volt. rises, int. LVS = write protect
	VTH1−	3.6	3.85	4.1	V	When supply volt. falls, int. LVS = write protect
Threshold voltage 2	VTH2+	—	3.92	4.17	V	When supply volt. rises, ext. LVS
	VTH2−	3.47	3.72	3.97	V	When supply volt. falls, ext. LVS
Hysteresis voltage	VH	50	—	—	mV	
Output low level voltage	VOL	—	—	0.40	V	V_{CC}=2.5 [V] IOL=0.2 [mA]
Output leakage current	IOH	—	—	10	μA	

Recovery time

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
POWER·SAVE→READ	TR2	—	—	500	μs	by XPS
READ→ERASE	TR3	—	—	6	μs	by XEG
READ→WRITE	TR4	—	—	4	μs	by XWG
WRITE→READ	TR5E	—	—	20	μs	by XEG
	TR5W	—	—	160	μs	by XWG
SIDE0↔SIDE1	TR6	—	—	40	μs	by XS1
1MB↔2MB	TR7	—	—	40	μs	by XHD

Preamplifier

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Voltage gain(1)	GVD1	43	46	49	dB	f=125[kHz], VIN=2.5[mV_{P-P}] (differential) (OPTION outer edge)
Voltage gain(2)	GVD2	46	49	52	dB	f=125[kHz], VIN=2.5[mV_{P-P}] (differential) (1 MB/2 MB outer edge, OPTION inner edge
Voltage gain(3)	GVD3	49	52	56	dB	f=125[kHz], VIN=1.5[mV_{P-P}] (differential) (1 MB/2 MB inner edge)
SIDE0↔SIDE1 crosstalk	GCTLK	50	—	—	dB	f=125[kHz], VIN=100[mV_{P-P}] (differential)*3
Differential input resistance	RID	—	4	—	kΩ	Input resistance = 8.0 kΩ parallel, damping resistance = 8.0 kΩ
Input conversion noise voltage	VN	—	2.5	3.7	μV_{rms}	f=500[Hz]~1[MHz]
Input sink current	ISINK	—	180	—	μA	
Differential input voltage amplitude(1)	VIN1	—	—	5.0	mV_{P-P}	5% distortion (sine wave input) (OPTION outer edge)
Differential input voltage amplitude(2)	VIN2	—	—	3.5	mV_{P-P}	5% distortion (sine wave input) (1 MB/2 MB outer edge, OPTION inner edge)
Differential input voltage amplitude(3)	VIN3	—	—	2.0	mV_{P-P}	5% distortion (sine wave input) (1 MB/2 MB = inner edge)
Common mode rejection ratio	CMRR	50	—	—	dB	f=125[kHz], VIN=100[mV_{P-P}] *3
Power supply rejection ratio	PSRR	40	—	—	dB	f=250[kHz], VIN=100[mV_{P-P}] *3

Preamplifier / L.P.F / differentiator (B.P.F)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Filter time constant accuracy	EFIL	−10	−	+10	%	∗3
Total gain (preamplifier/ LPF/differentiator) (1)	GVDD1	41.0	45.0	49.0	dB	f=250[kHz], VIN=2.5[mVP-P] (differential) (2MB outer edge)
Total gain (preamplifier/ LPF/differentiator) (2)	GVDD2	44.0	48.0	52.0	dB	f=250[kHz], VIN=2.5[mVP-P] (differential) (inner edge)
Total gain (preamplifier/ LPF/differentiator) (3)	GVDD3	40.5	44.5	48.5	dB	f=250[kHz], VIN=2.5[mVP-P] (differential) (OPTION 2 outer edge)
Differentiator output peaking frequency setting range	f0	0.1	−	0.5	MHz	Defined according to typical value in the settings

∗3 RRCC=2.0 [kΩ] (XHD=L, XTR=H, FC=L)

Comparator and waveform shaping

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
TDF M/M pulse width accuracy (1)	TDF1	−10	−	+10	%	1MB (TYP : 2545[ns]) f=62.5[kHz]～125[kHz] ∗4
TDF M/M pulse width accuracy (2)	TDF2	−10	−	+10	%	2MB, OPTION (TYP : 1280[ns]) f=62.5[kHz]～125[kHz] ∗4
RD pulse width	TRD	270	400	530	ns	Determination level: 1.5[V]
Rise time	TTLH	−	−	70	ns	Rise time between 0.4[V]and 2.0[V]
Fall time	TTHL	−	−	70	ns	Fall time between 2.0 [V]and 0.4[V]
Peak shift	P. S.	−	−	1.0	%	f=250[kHz], VIN=1[mVP-P](differential)
Output low level voltage	VOL	−	−	0.5	V	
Output high level voltage	VOH	2.7	−	−	V	Level after 70[ns]rise from 0.4[V]

∗4 RRCC=2.0 [kΩ]

Write circuit

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Write current adjustment range	IWR	2.0	−	20	mA0-P	
Write current accuracy	ACIW	−7.0	−	+7.0	%	∗5
Write current pairability	△IWR	−1.0	−	+1.0	%	RWCC=2.4[kΩ]
Write current supply voltage dependency	PSIW	−4.0	−0.8	+3.0	% / V	RWCC=2.4[kΩ]
Output saturation voltage	VSATRW	−	0.4	1.0	V	IWR=12[mA]
Off-state leakage current	ILKRW1	−	−	20	μA	Unselected side
	ILKRW2	−	−	50	μA	Selected side
Minimum write data pulse width	TWD	70	−	−	ns	
Write current switching ratio accuracy	ACIWTR	±10× (1− setting ratio)			%	∗6

∗5 RWCC=2.4 [kΩ] , adapted for desired setting.
∗6 Error in setting ratio (reference: 1MB outer track)

Erase output

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Erase current adjustment	IER	—	—	40	mA	
Output saturation voltage	VSATER	—	0.2	0.6	V	IER=40[mA]
Output leak current	IOH	—	—	10	μA	Off, ED0 = ED1 = Vcc

Logic input

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input high level voltage	VIH	2.0	—	—	V	
Input low level voltage	VIL	—	—	0.8	V	
Input voltage hysteresis	VH	0.15	—	—	V	Applies to XWD, XWG, XEG, XS1
Input low level current	IIL1	—	50	100	μA	Vcc=5[V] VIL=GND Applies to XWG, XEG ,XHD

●Mode table

Mode			1MB		2MB		OPTION1		OPTION2	
Transfer rate			250[kbps]		500[kbps]		500[kbps]		500[kbps]	
Input	Mode	XHD	HIGH		LOW		HIGH		NO CARE	
		FC	LOW		LOW		LOW		HIGH	
		XGR	HIGH		NO CARE		LOW			
	Track	XTR (XSWF)	Outer track LOW	Inner track HIGH	Outer track LOW	Inner track HIGH	Outer track LOW	Inner track HIGH	Outer track LOW	Inner track HIGH
Output	Preamplifier gain [dB]		49	52	49	52	46	49	46	49
	Filter	f_0 [kHz]	197	210	378	415	350	400	350	
		Characteristic.(Q)*1	A	A	A	B	C	A	C	
	TDF	[nSEC]	2545		1280		1280			
	Write current switching ratio		WCC	WCC ×0.733	WCC ×0.433	WCC ×0.318	WCC	WCC ×0.733	WCC ×0.733	

(However, RRCC=2.0 [kΩ])

*1 (A) Butterworth characteristics
(B) Chebyshev characteristics
(C) Refer to Option characteristics, filter characteristics

Total filter peak frequency setting

$f_0 = a / (RRCC\ [k\Omega] + 0.09)\ [kHz]$

a = 412 1M outer track
439 1M inner track
790 2M outer track
867 2M inner track
732 outer track(with OPTION 1), OPTION 2
836 inner track (with OPTION 1)

TDF time constant setting

250 [kbps] : $T = 939 \times RRCC\ [k\Omega] + 667\ [ns]$
500 [kbps] : $T = 403 \times RRCC\ [k\Omega] + 474\ [ns]$

Write current setting

$$Iwr = \frac{24.0}{RWCC\ [k\Omega]}\ [mA]$$

●Filter characteristic

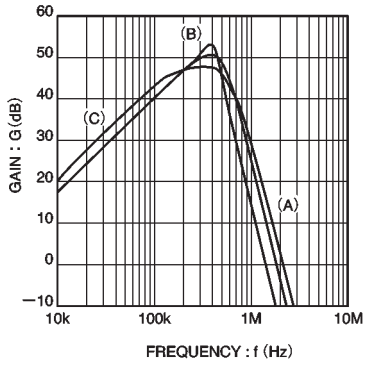
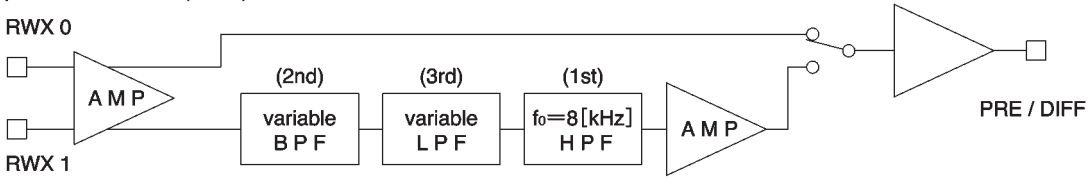
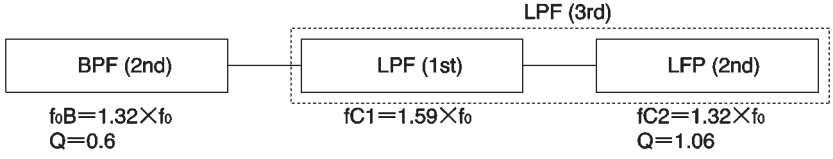


Fig. 1 Pre in / diff out characteristic

Preamplifier-differentiator (B.P.F)-L.P.F

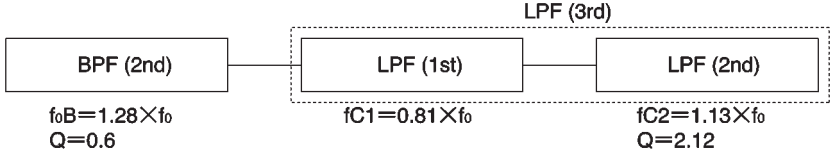


(A) Total characteristic peak frequency (f_0): 1 MB, 2 MB outer track OPTION inner edge



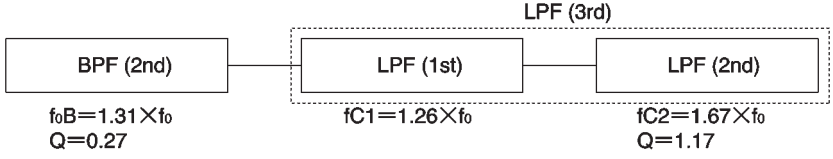
: Butterworth setting

(B) Total characteristic peak frequency (f_0): 2 MB inner track



: Chebyshev setting

(C) Total characteristic peak frequency (f_0): OPTION outer track, OPTION2



: OPTION setting

●Measurement circuit

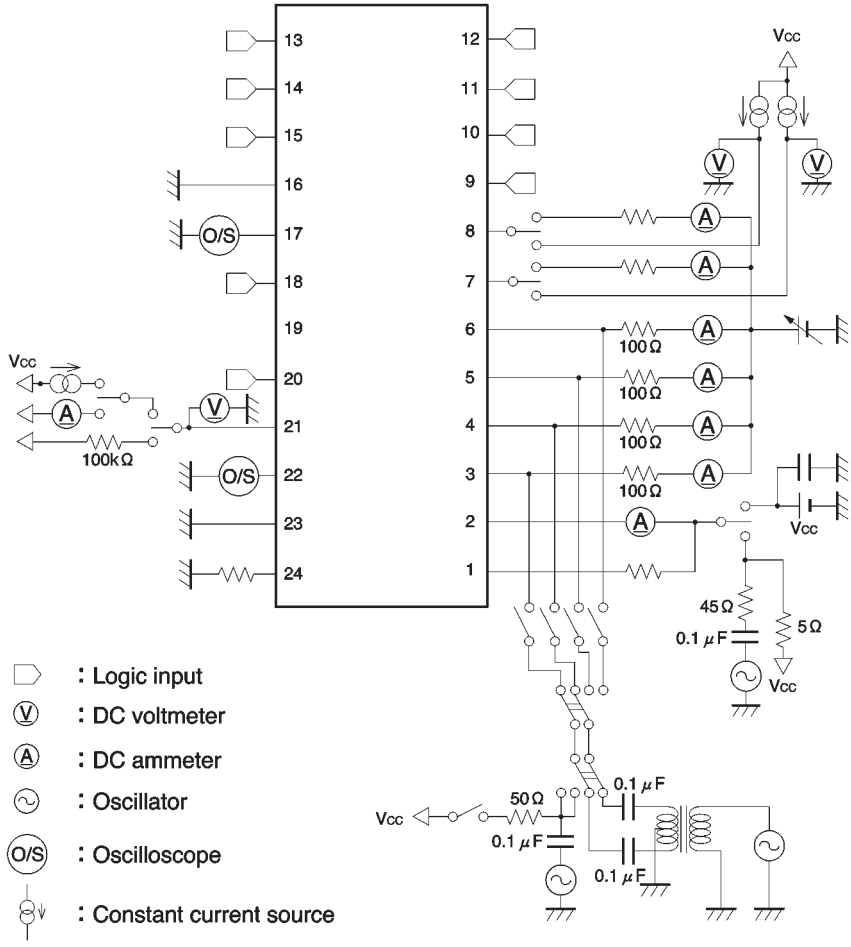


Fig. 2

●Circuit operation

(1) Read

The input signal from the head coils from each side of the disc is amplified by the preamplifier and then differentiated. The filter time constant can be set externally. After differentiation, the differential output is input to the comparator. The time domain filter detects zero cross, and the output is converted to read data. The monostable multivibrator width can be set externally, while the read data pulse width is a constant 400ns.

(2) Write

Input write data are converted to toggle movements by the internal flip-flops, operating the write driver. The write driver current is supplied by the write current generator, but the externally set current can be controlled according to density and by selecting inner track/ outer track.

(3) Erase

An open collector output pin is used, and the erase current is set with a resistor between it and the head.

(4) Power supply

When the low level voltage detector detects a drop in the supply voltage, writing and erasing are prohibited.

●Operation notes

(1) Use a short pattern for V_{CC}, and a sufficiently wide AGND and DGND. Keep the impedance between V_{CC} and GND low by inserting a bypass capacitor.

(2) Use a pattern that will minimize interference between digital signals and the head.

●Electrical characteristic curves

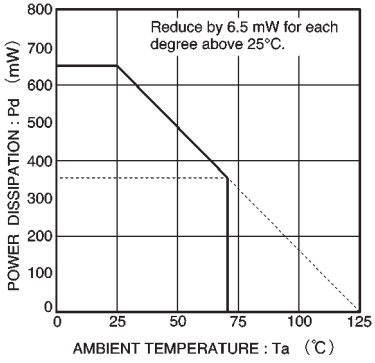


Fig. 3 Thermal derating characteristics

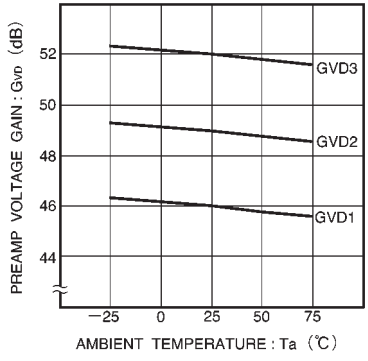


Fig. 4 Preamp voltage gain vs. ambient temperature

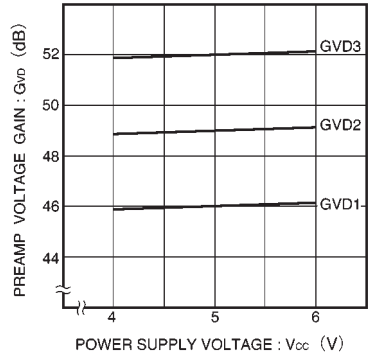


Fig. 5 Preamp voltage gain vs. power supply voltage

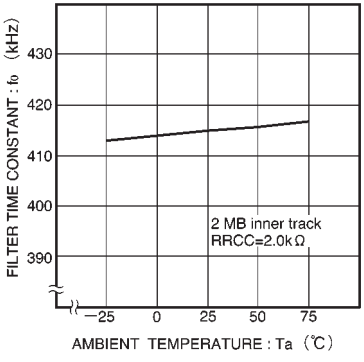


Fig. 6 Filter time constant (f_0) vs. ambient temperature

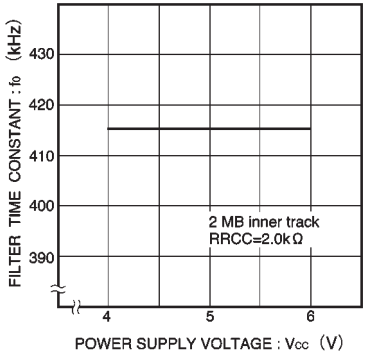


Fig. 7 Filter time constant (f_0) vs. power supply voltage

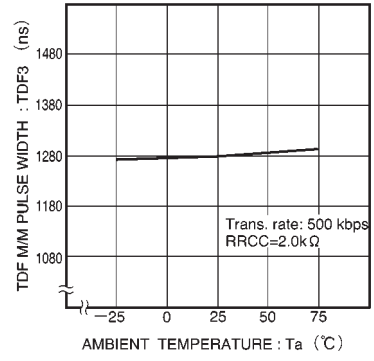


Fig. 8 TDF time constant vs. ambient temperature

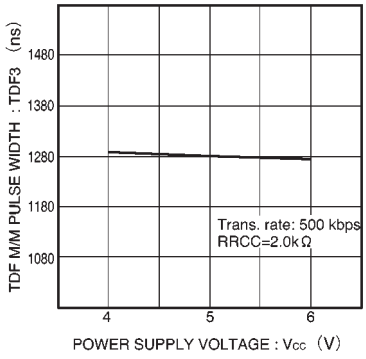


Fig. 9 TDF time constant vs. power supply voltage

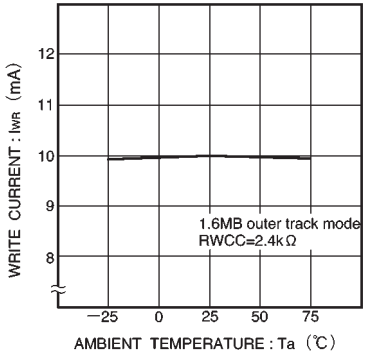


Fig. 10 Write current vs. ambient temperature

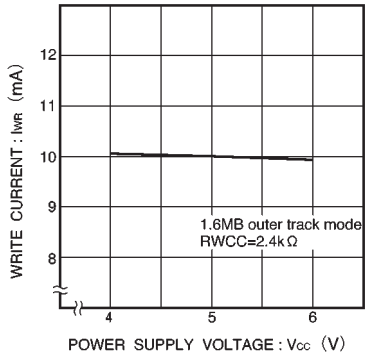


Fig. 11 Write current and power supply voltage

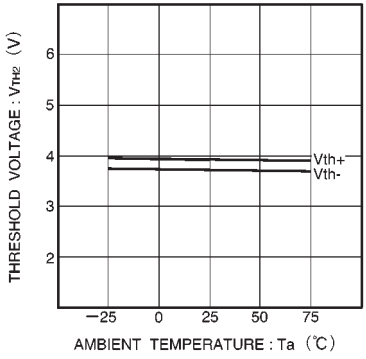


Fig. 12 Low level detection voltage vs. ambient temperature

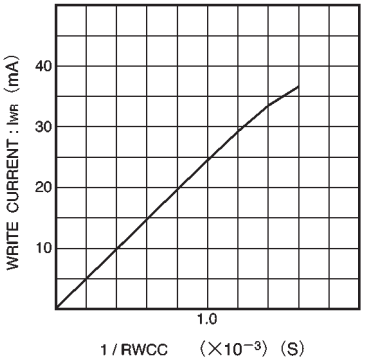


Fig. 13 Write current vs. write current adjustment resistance

●External dimensions (Units: mm)