LR38630

Digital Signal Processor for CIF CMOS Image Cameras

DESCRIPTION

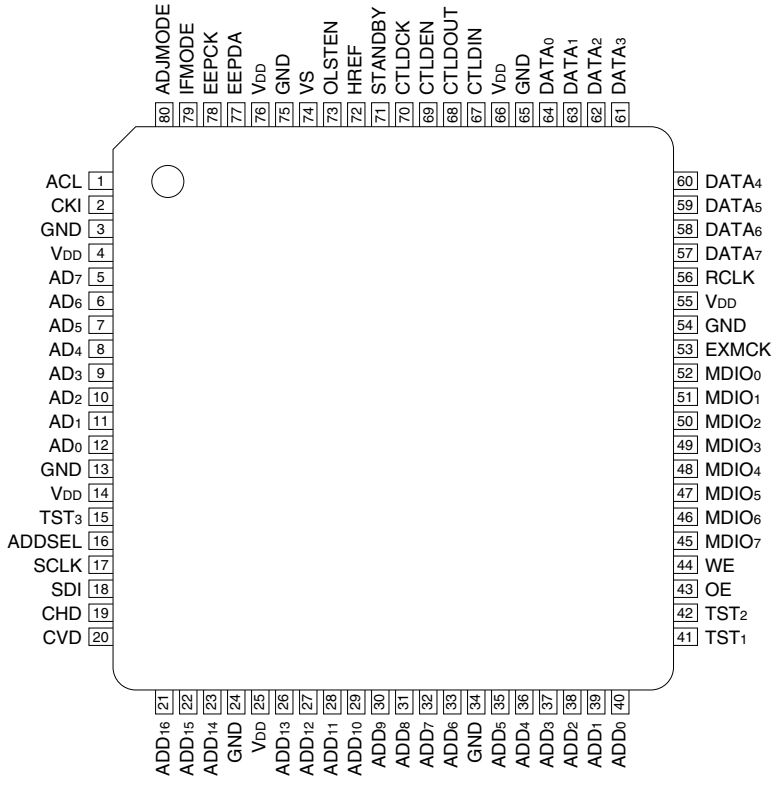
The LR38630 is a CMOS digital signal processor for color camera systems of 110 k-pixel CMOS image sensor with primary color mosaic filters. The camera system consists of CIF CMOS image sensor (LZ34C10) and DSP IC (LR38630) with 2 k-bit EEPROM. Depending on application, 1 M-bit SRAM can be added in order to get slower frame rate at video output.

FEATURES

- Designed for 110 k-pixel color CMOS image sensors with R, G, and B color mosaic filters
- Compatible with CIF standard
- External control interface input/output
- Variable GAMMA and KNEE response
- 8-bit digital input
- Available for digital video 4 : 2 : 2 (U/Y/V/Y) output
- Built-in synchronous signal generation circuit to drive CMOS image sensor
- Built-in 2 k-bit EEPROM controller to set the camera adjustment data
- Built-in auto exposure control
- Built-in auto white balance control
- Built-in auto carrier balance control
- Built-in white blemish compensator
- Lower power consumption by dual clocking signal process technology
- Single +3.0 V power supply
- Package :
  80-pin LQFP (LQFP080-P-1212) 0.5 mm pin-pitch

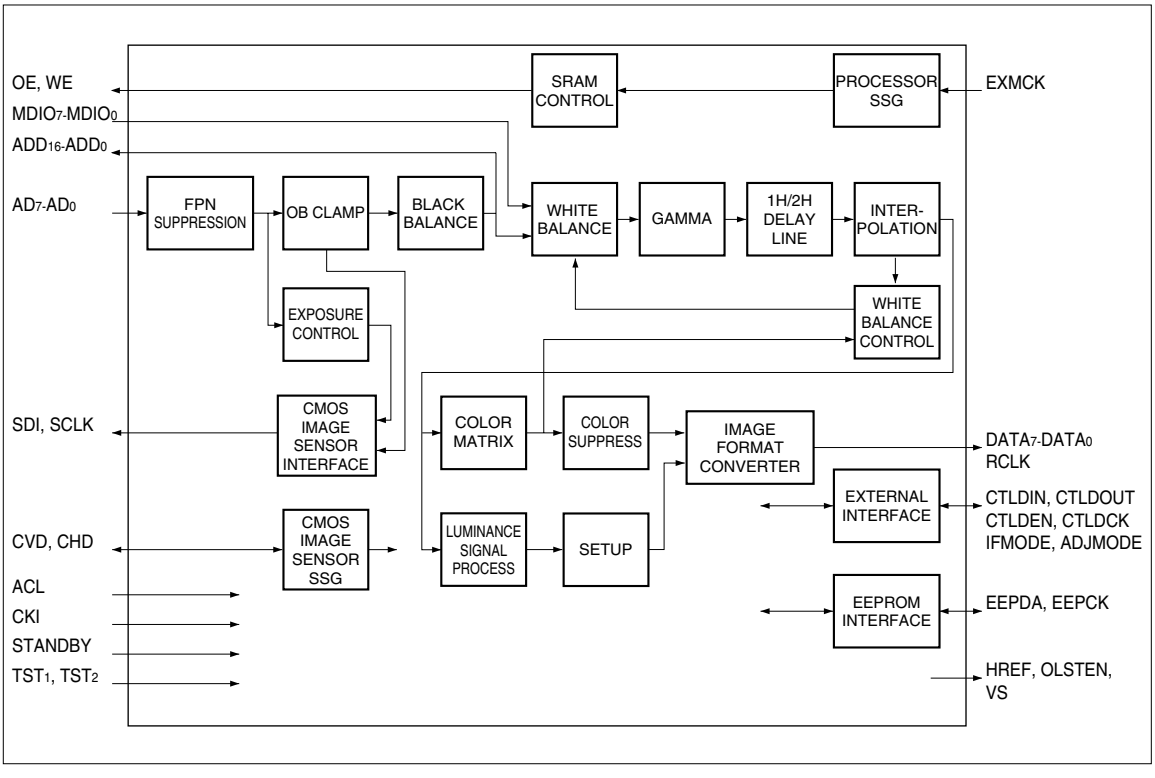
PIN CONNECTIONS

80-PIN LQFP TOP VIEW



(LQFP080-P-1212)

BLOCK DIAGRAM



PIN DESCRIPTION

PIN NO.	SYMBOL	I/O	POLARITY	DESCRIPTION
1	ACL	IC		Initializing input.
2	CKI	IC		Clock input. Connect to pin 14 of LZ34C10.
3	GND	–		A grounding pin.
4	V_{DD}	–		Supply of +3.0 V power.
5	AD_7	IC		Digital signal input, fed from pin 23 of LZ34C10 (MSB).
6	AD_6	IC		Digital signal input, fed from pin 22 of LZ34C10.
7	AD_5	IC		Digital signal input, fed from pin 21 of LZ34C10.
8	AD_4	IC		Digital signal input, fed from pin 20 of LZ34C10.
9	AD_3	IC		Digital signal input, fed from pin 19 of LZ34C10.
10	AD_2	IC		Digital signal input, fed from pin 18 of LZ34C10.
11	AD_1	IC		Digital signal input, fed from pin 17 of LZ34C10.
12	AD_0	IC		Digital signal input, fed from pin 16 of LZ34C10 (LSB).
13	GND	–		A grounding pin.
14	V_{DD}	–		Supply of +3.0 V power.
15	TST_3	IC		A test pin. Connect to GND.
16	ADDSEL	IC		Pin to set MSB to be added on serial address data. Low : MSB = 0 (address 00h-7Fh), High : MSB = 1 (address 80h-FFh)
17	SCLK	OBF4M		Clock output of serial data, connected to pin 28 of LZ34C10.
18	SDI	OBF4M		Serial data output, connected to pin 27 of LZ34C10.
19	CHD	OBF4M		Horizontal drive pulse output, connected to pin 25 of LZ34C10.
20	CVD	OBF4M		Vertical drive pulse output, connected to pin 26 of LZ34C10.
21	ADD_{16}	OBF4M		Address output to drive an external SRAM.
22	ADD_{15}	OBF4M		Address output to drive an external SRAM.
23	ADD_{14}	OBF4M		Address output to drive an external SRAM.
24	GND	–		A grounding pin.
25	V_{DD}	–		Supply of +3.0 V power.
26	ADD_{13}	OBF4M		Address output to drive an external SRAM.
27	ADD_{12}	OBF4M		Address output to drive an external SRAM.
28	ADD_{11}	OBF4M		Address output to drive an external SRAM.
29	ADD_{10}	IO4M		Address output to drive an external SRAM.
30	ADD_9	IO4M		Address output to drive an external SRAM.
31	ADD_8	IO4M		Address output to drive an external SRAM.
32	ADD_7	IO4M		Address output to drive an external SRAM.
33	ADD_6	IO4M		Address output to drive an external SRAM.
34	GND	–		A grounding pin.
35	ADD_5	IO4M		Address output to drive an external SRAM.
36	ADD_4	IO4M		Address output to drive an external SRAM.
37	ADD_3	IO4M		Address output to drive an external SRAM.
38	ADD_2	IO4M		Address output to drive an external SRAM.
39	ADD_1	IO4M		Address output to drive an external SRAM.

PIN NO.	SYMBOL	I/O	POLARITY	DESCRIPTION
40	ADD_0	IO4M		Address output to drive an external SRAM.
41	TST_1	IC		A test pin. Connected to GND.
42	TST_2	IC		A test pin. Connected to GND.
43	OE	OBF4M		Output enable to drive an external SRAM.
44	WE	OBF4M		Write enable to drive an external SRAM.
45	$MDIO_7$	IO4MU		Address output to drive an external SRAM.
46	$MDIO_6$	IO4MU		Address output to drive an external SRAM.
47	$MDIO_5$	IO4MU		Address output to drive an external SRAM.
48	$MDIO_4$	IO4MU		Address output to drive an external SRAM.
49	$MDIO_3$	IO4MU		Address output to drive an external SRAM.
50	$MDIO_2$	IO4MU		Address output to drive an external SRAM.
51	$MDIO_1$	IO4MU		Address output to drive an external SRAM.
52	$MDIO_0$	IO4MU		Address output to drive an external SRAM.
53	EXMCK	IC		External clock input.
54	GND	–		A grounding pin.
55	V_{DD}	–		Supply of +3.0 V power.
56	RCLK	OBF4M		Clock output for digital video output signal.
57	$DATA_7$	OBF4M		Data input/output to drive an external SRAM.
58	$DATA_6$	OBF4M		Data input/output to drive an external SRAM.
59	$DATA_5$	OBF4M		Data input/output to drive an external SRAM.
60	$DATA_4$	OBF4M		Data input/output to drive an external SRAM.
61	$DATA_3$	OBF4M		Data input/output to drive an external SRAM.
62	$DATA_2$	OBF4M		Data input/output to drive an external SRAM.
63	$DATA_1$	OBF4M		Data input/output to drive an external SRAM.
64	$DATA_0$	OBF4M		Data input/output to drive an external SRAM.
65	GND	–		A grounding pin.
66	V_{DD}	–		Supply of +3.0 V power.
67	CTLDIN	IC		Serial data input.
68	CTLDOUT	OBF4M		Serial data input.
69	CTLDEN	IC		The rising edge enables the serial data to be available.
70	CTLDCK	IC		Clock input to set the data.
71	STANDBY	IC		High level puts this IC and LZ34C10 in standby mode.
72	HREF	OBF4M		Horizontal blanking pulse output keeping high level during the effective image period.
73	OLSTEN	OBF4M		Horizontal pulse output going to low level when starting in horizontal.
74	VS	OBF4M		Vertical blanking pulse output keeping high level during the effective image period.
75	GND	–		A grounding pin.
76	V_{DD}	–		Supply of +3.0 V power.
77	EEPDA	IO4M		Data input/output to/from EEPROM. Going to high-impedance with high level of pin 80.

PIN NO.	SYMBOL	I/O	POLARITY	DESCRIPTION
78	EEPCK	IO4M		Clock input/output to/from EEPROM. Going to high-impedance with high level of pin 80.
79	IFMODE	IC		The option of number of bits of serial data to adjust. High level : W/R flag + address 6 bits + data 16 bits Low level : W/R flag + address 8 bits + data 8 bits
80	ADJMODE	IC		Void input of internal automatic control circuit, connected to low level normally. High level input stops automatic control function. Power-on with high level input stops automatic loading of EEPROM data.

IO4M : Input/output pin (4 mA output, CMOS level input)
IO4MU : Input/output pin (4 mA output, CMOS level input with pull-up resistor)
OBF4M : Output pin (4 mA output)
IC : Input pin (CMOS level input)

INTERNAL COEFFICIENT TABLE

ADDRESS	NAME	BITS	FUNCTION
00h	–	–	Not used.
01h	–	–	Not used.
02h	MOS_MIR	2 (7) (6)	Option of the output image type. 00 : Normal 01 : Inverted top and bottom 10 : Reversed left and right 11 : Reversed all
	MOS_SAD	2 (5) (4)	Option of AD converter clock phase. 00 : Reference 01 : Delayed by 90˚ 10 : Delayed by 180˚ 11 : Delayed by 270˚
	MOS_AGC	3 (3) (2) (1)	Option of AGC offset gain. 000 : 3 dB 001 : 4 dB 010 : 5 dB 011 : 6 dB 100 : 7 dB 101 : 8 dB 110 : 9 dB 111 : 10 dB
	MOS_STD	1 (0)	Under low level at pin 71, this bit can make CMOS image sensor standby. 0 : Operating 1 : Standby
03h	QCIF_SEL	1 (7)	Option of sampling position in QCIF. 0 : Red filter 1 : Green filter
	CA_HOLD	1 (6)	Carrier balance function. 0 : Automatic added an offset (coefficient) 1 : 0h added an offset (coefficient)
	BLC	1 (5)	Option of exposure level reference. 0 : Data of address 06h 1 : Data of address 09h
	WB_MODE	2 (4) (3)	Option of white balance mode. 00 : Automatic 01 : Preset WB1 1X : Preset WB2
	EE_HOLD	2 (2) (1)	Option of electronic exposure mode. 00 : Automatic electronic shutter speed and AGC ON 01 : Fixed electronic shutter speed and AGC ON 10 : Automatic electronic shutter speed and AGC OFF 11 : Fixed electronic shutter speed and AGC OFF
	OFSET_AUTO	1 (0)	Option of optical black level control. 0 : Automatic 1 : Fixed level

ADDRESS	NAME	BITS	FUNCTION
04h	OUT_SEL	2 (7) (6)	Option of output mode. 00 : QCIF1 01 : CIF 10 : QVGA 11 : QCIF2
	IN_TIM	2 (5) (4)	Clock timing for input. 00 : Delayed by one CK 01 : Delayed by two CK 10 : Not delayed
	ACT_MODE	4 (3) (2) (1) (0)	0000 : CIF image output with CKI clock of CMOS image sensor 0001 : 1 frame of image output per second with CKI clock 0010 : 2 frames of image output per second with CKI clock 0011 : 15 frames of image output per second with CKI clock 0101 : 1 frame of image output per second with EXCK clock (1 frame data is written to RAM in vertical blanking.) 0110 : 2 frames of image output per second with EXCK clock (2 frames data are written to RAM in vertical blanking.) 0111 : Image output with EXMCK clock (EXMCK should be lower than 4.5 MHz.) 1XXX : Except 0000, works with 30 frames after power-on. (example) 1001 : 1 frame of image output per second with CKI starting with 30 frames after power-on. 1000 : Prohibited to use
05h	ACT_TIM	8	Setting a period to work with 30 frames after power-on. A period = (Data + 1) x frame rate
06h	REF_IRIS	8	Electronic exposure reference level.
07h	CTLD_01	8	The second target area of electronic exposure control. In the case that exposure control data is within (data of address 06h ± data of address 07h), the exposure control is completed.
08h	CTLD_02	8	The first target area of electronic exposure control. If exposure control data is over (data of address 06h ± data of address 08h), the exposure control is restarted.
09h	REF_BLC	8	Exposure reference level in BLC (valid with BLC of address 03h = 1).
0Ah	CTLD_11	8	The second target area of electronic exposure control in BLC. In the case that exposure control data is within (data of address 09h ± data of address 0Ah), the exposure control is completed.
0Bh	CTLD_12	8	The first target area of electronic exposure control in BLC. If exposure control data is over (data of address 09h ± data of address 0Bh), the exposure control is restarted.

ADDRESS	NAME	BITS	FUNCTION
0Ch	SH_MAX	2 (7) (6)	Option of maximum electronic shutter speed in automatic. Electronic exposure control. 00 : 1/9 900 s 01 : 1/4 950 s 10 : 1/1 980 s 11 : 1/1 100 s
	EE_SPD	2 (5) (4)	Option of electronic shutter speed and AGC speed change. 00 : Shutter speed is changed by 10-19 pitches. 01 : Shutter speed is changed by 8-10 pitches. 1X : Shutter speed is changed by 1 pitch (the finest)
	EE_RATIO	2 (3) (2)	Window option of automatic electronic exposure control. 00 : Center weighted 1 01 : Center weighted 2 10 : No window 11 : Lower-position weighted
	EE_LPF	2 (1) (0)	Option of time constant in electronic exposure control. 00 : Longer time constant 01 : Long time constant 1X : No time constant
0Dh	SH_HOLD2	1	MSB of fixed electronic shutter speed.
0Eh	SH_HOLD1	8	Lower bits of fixed electronic shutter speed. Data between 000 and 149 can be set by address 0Dh and 0Eh.
0Fh	AGC_HOLD	8	Preset gain in making AGC OFF (EE_HOLD = 1X at address 03h).
10h	OFSET_HOLD	8	Fixed optical black level (OFSET_AUTO =1 at address 03h).
11h	OFSET_LPF	2 (4) (3)	Time constant option of automatic optical black level control. 00 : Longer time constant 01 : Long time constant 1X : No time constant
	WBFIX1	1 (2)	Option of automatic white balance control. 0 : Not accelerated 1 : Accelerated
	SEL_LPF	2 (1) (0)	Time constant option of automatic white balance control. 00 : Longer time constant 01 : Long time constant 1X : No time constant
12h	KGBGR1	8	The first target area of automatic white balance control in minus direction of high-speed mode. In the case that white balance control data is within (data of address 12h + data of address 13h), high-speed mode control is completed and then changed to normal-speed control mode.

ADDRESS	NAME	BITS	FUNCTION
13h	KGBGR2	8	The first target area of automatic white balance control in plus direction of high-speed mode. In the case that white balance control data is within (data of address 12h + data of address 13h), high-speed mode control is completed and then changed to normal-speed control mode.
14h	KGBGR3	8	The second target area of automatic white balance control in minus direction of high-speed mode. In the case that white balance control data is over (data of address 14h + data of address 15h), high-speed mode control is restarted.
15h	KGBGR4	8	The second target area of automatic white balance control in plus direction of high-speed mode. In the case that white balance control data is over (data of address 14h + data of address 15h), high-speed mode control is restarted.
16h	LIMIM	8	Limitation in making white balance data at minus I-axis.
17h	LIMIP	8	Limitation in making white balance data at plus I-axis.
18h	LIMQM	8	Limitation in making white balance data at minus Q-axis.
19h	LIMQP	8	Limitation in making white balance data at plus Q-axis.
1Ah	YLCL	8	Limitation in making white balance data. A pixel with lower luminance level than data of this address is neglected.
1Bh	YHCL	8	Limitation in making white balance data. A pixel with higher luminance level than data of this address is neglected.
1Ch	LIMWIIM	7	The first target area of auto white balance control in minus I-axis. In the case that white balance control data is within the area by address 1Ch, 1Dh, 1Eh and 1Fh, automatic white balance control is completed.
1Dh	LIMWIIP	7	The first target area of auto white balance control in plus I-axis.
1Eh	LIMWIQM	7	The first target area of auto white balance control in minus Q-axis.
1Fh	LIMWIQP	7	The first target area of auto white balance control in plus Q-axis.
20h	LIMWOI	7	The second target area of auto white balance control in I-axis. In the case that white balance control data is over the area by address 20h and 21h, automatic white balance control is restarted.
21h	LIMWOQ	7	The second target area of auto white balance control in Q-axis. In the case that white balance control data is over the area by address 20h and 21h, automatic white balance control is restarted.
22h	WBR_MAX	8	Maximum gain of red signal in automatic white balance control.
23h	WBR_MIN	8	Minimum gain of red signal in automatic white balance control.
24h	WBB_MAX	8	Maximum gain of blue signal in automatic white balance control.
25h	WBB_MIN	8	Minimum gain of blue signal in automatic white balance control.
26h	WBR1	8	White balance preset 1 : Red signal gain
27h	WBB1	8	White balance preset 1 : Blue signal gain
28h	WBR2	8	White balance preset 2 : Red signal gain
29h	WBB2	8	White balance preset 2 : Blue signal gain

ADDRESS	NAME	BITS	FUNCTION
2Ah	GAM_SLOPE0	8	Gamma curve setting : First straight line slope
2Bh	GAM_SLOPE1	8	Gamma curve setting : Second straight line slope
2Ch	GAM_SLOPE2	8	Gamma curve setting : Third straight line slope
2Dh	GAM_SLOPE3	8	Gamma curve setting : Fourth straight line slope
2Eh	GAM_SLOPE4	8	Gamma curve setting : Fifth straight line slope
2Fh	GAM_SLOPE5	8	Gamma curve setting : Sixth straight line slope
30h	GAM_SLOPE6	8	Gamma curve setting : Seventh straight line slope
31h	GAM_SLOPE7	8	Gamma curve setting : Eighth straight line slope
32h	GAM_SLOPE8	8	Gamma curve setting : Ninth straight line slope
33h	GAM_SLOPE9	8	Gamma curve setting : Tenth straight line slope
34h	GAM_OFSET1	8	Gamma curve setting : Second straight line offset
35h	GAM_OFSET2	8	Gamma curve setting : Third straight line offset
36h	GAM_OFSET3	8	Gamma curve setting : Fourth straight line offset
37h	GAM_OFSET4	8	Gamma curve setting : Fifth straight line offset
38h	GAM_OFSET5	8	Gamma curve setting : Sixth straight line offset
39h	GAM_OFSET6	8	Gamma curve setting : Seventh straight line offset
3Ah	GAM_OFSET7	8	Gamma curve setting : Eighth straight line offset
3Bh	GAM_OFSET8	8	Gamma curve setting : Ninth straight line offset
3Ch	GAM_OFSET9	8	Gamma curve setting : Tenth straight line offset
3Dh	KCBR	8	Carrier balance : Red signal compensation
3Eh	KCBB	8	Carrier balance : Blue signal compensation
3Fh	KCBG1	8	Carrier balance : Green signal compensation in RG line
40h	KCBG2	8	Carrier balance : Green signal compensation in BG line
41h	KY1	8	Gain in middle frequency components of luminance signal.
42h	KHC	6	Horizontal aperture level compression in lower luminance level.
43h	KHGA	8	Horizontal aperture gain.
44h	KVC	6	Vertical aperture level compression in lower luminance level.
45h	KVGA	8	Vertical aperture gain.
46h	KLL	8	Luminance level.
47h	KSU	6	Set up level.
48h	K0_MAT1	8	AWB color matrix : R – Y 1
49h	K1_MAT1	8	AWB color matrix : R – Y 2
4Ah	K2_MAT1	8	AWB color matrix : B – Y 1
4Bh	K3_MAT1	8	AWB color matrix : B – Y 2
4Ch	K0_MAT2	8	WB1 color matrix : R – Y 1
4Dh	K1_MAT2	8	WB1 color matrix : R – Y 2
4Eh	K2_MAT2	8	WB1 color matrix : B – Y 1
4Fh	K3_MAT2	8	WB1 color matrix : B – Y 2
50h	K0_MAT3	8	WB2 color matrix : R – Y 1
51h	K1_MAT3	8	WB2 color matrix : R – Y 2
52h	K2_MAT3	8	WB2 color matrix : B – Y 1

ADDRESS	NAME	BITS	FUNCTION
53h	K3_MAT3	8	WB2 color matrix : B – Y 2
54h	KCRGA	8	AWB color level : R – Y
55h	KCBGA	8	AWB color level : B – Y
56h	KCRGA1	8	WB1 color level : R – Y
57h	KCBGA1	8	WB1 color level : B – Y
58h	KCRGA2	8	WB2 color level : R – Y
59h	KCBGA2	8	WB2 color level : B – Y
5Ah	KCCR	7	R – Y color signal base clip level.
5Bh	KCCB	7	B – Y color signal base clip level.
5Ch	KCLC	8	Lower luminance level to suppress color signal level.
5Dh	KLGL	4	Gain to suppress color signal level by data of address 5Ch.
5Eh	KCHC	8	Higher luminance level to suppress color signal level.
5Fh	KLGH	4	Gain to suppress color signal level by data of address 5Eh.
60h	KLGE	8	Gain to suppress color edge signal.
61h	KILL_AGC	8	AGC gain to start the suppression of color signal level.
62h	KILL_AGCG	4	Gain to suppress color signal level by data of address 61h.
63h	APT_AGC	8	AGC gain to start the suppression of aperture level.
64h	APT_AGCG	4	Gain to suppress aperture level by data of address 63h.
65h	FPN_GA	8	Gain for fixed pattern noise signal.
66h	AGC_SLP1	8	AGC gain compensation 1 for fixed pattern noise signal.
67h	AGC_SLP2	8	AGC gain compensation 2 for fixed pattern noise signal.
68h	AGC_SLP3	8	AGC gain compensation 3 for fixed pattern noise signal.
69h	AGC_SLP4	8	AGC gain compensation 4 for fixed pattern noise signal.
6Ah	IN_OUT	1 (0)	Option of output mode. 0 : Normal processing 1 : Output of input signal1
6Bh	–	–	Not used.
6Ch	–	–	Not used.
6Dh	–	–	Not used.
6Eh	–	–	Not used.
6Fh	TEST	5	Data should be 00h.
70h	R_DATA1	8	Lower 8 bits of red signal to control auto white balance.
71h	R_DATA2	4	Upper 4 bits of red signal to control auto white balance.
72h	G_DATA1	8	Lower 8 bits of green signal to control auto white balance.
73h	G_DATA2	4	Upper 4 bits of green signal to control auto white balance.
74h	B_DATA1	8	Lower 8 bits of blue signal to control auto white balance.
75h	B_DATA2	4	Upper 4 bits of blue signal to control auto white balance.
76h	I_DATA1	8	Lower 8 bits of I signal to control auto white balance.
77h	I_DATA2	1	Sign bit of I signal to control auto white balance.
78h	Q_DATA1	8	Lower 8 bits of Q signal to control auto white balance.
79h	Q_DATA2	1	Sign bit of Q signal to control auto white balance.
7Ah	IRIS_DATA1	8	Lower 8 bits of luminance signal to control auto exposure.

ADDRESS	NAME	BITS	FUNCTION
7Bh	IRIS_DATA2	4	Upper 4 bits of luminance signal to control auto exposure.
7Ch	RCA_DATA	8	Red signal to control auto carrier balance.
7Dh	GRCA_DATA	8	Green signal in RG line to control auto carrier balance.
7Eh	BCA_DATA	8	Blue signal to control auto carrier balance.
7Fh	GBCA_DATA	8	Green signal in BG line to control auto carrier balance.
80h	WP00H1	8	Lower 8 bits of X-axis on the position of white blemish 1.
81h	WP00H2	1	MSB of X-axis on the position of white blemish 1.
82h	WP00V1	8	Lower 8 bits of Y-axis on the position of white blemish 1.
83h	WP00V2	1	MSB of Y-axis on the position of white blemish 1.
84h	WP01H1	8	Lower 8 bits of X-axis on the position of white blemish 2.
85h	WP01H2	1	MSB of X-axis on the position of white blemish 2.
86h	WP01V1	8	Lower 8 bits of Y-axis on the position of white blemish 2.
87h	WP01V2	1	MSB of Y-axis on the position of white blemish 2.
88h	WP02H1	8	Lower 8 bits of X-axis on the position of white blemish 3.
89h	WP02H2	1	MSB of X-axis on the position of white blemish 3.
8Ah	WP02V1	8	Lower 8 bits of Y-axis on the position of white blemish 3.
8Bh	WP02V2	1	MSB of Y-axis on the position of white blemish 3.
8Ch	WP03H1	8	Lower 8 bits of X-axis on the position of white blemish 4.
8Dh	WP03H2	1	MSB of X-axis on the position of white blemish 4.
8Eh	WP03V1	8	Lower 8 bits of Y-axis on the position of white blemish 4.
8Fh	WP03V2	1	MSB of Y-axis on the position of white blemish 4.
90h	WP04H1	8	Lower 8 bits of X-axis on the position of white blemish 5.
91h	WP04H2	1	MSB of X-axis on the position of white blemish 5.
92h	WP04V1	8	Lower 8 bits of Y-axis on the position of white blemish 5.
93h	WP04V2	1	MSB of Y-axis on the position of white blemish 5.
94h	WP05H1	8	Lower 8 bits of X-axis on the position of white blemish 6.
95h	WP05H2	1	MSB of X-axis on the position of white blemish 6.
96h	WP05V1	8	Lower 8 bits of Y-axis on the position of white blemish 6.
97h	WP05V2	1	MSB of Y-axis on the position of white blemish 6.
98h	WP06H1	8	Lower 8 bits of X-axis on the position of white blemish 7.
99h	WP06H2	1	MSB of X-axis on the position of white blemish 7.
9Ah	WP06V1	8	Lower 8 bits of Y-axis on the position of white blemish 7.
9Bh	WP06V2	1	MSB of Y-axis on the position of white blemish 7.
9Ch	WP07H1	8	Lower 8 bits of X-axis on the position of white blemish 8.
9Dh	WP07H2	1	MSB of X-axis on the position of white blemish 8.
9Eh	WP07V1	8	Lower 8 bits of Y-axis on the position of white blemish 8.
9Fh	WP07V2	1	MSB of Y-axis on the position of white blemish 8.
A0h	WP08H1	8	Lower 8 bits of X-axis on the position of white blemish 9.
A1h	WP08H2	1	MSB of X-axis on the position of white blemish 9.
A2h	WP08V1	8	Lower 8 bits of Y-axis on the position of white blemish 9.
A3h	WP08V2	1	MSB of Y-axis on the position of white blemish 9.

ADDRESS	NAME	BITS	FUNCTION
A4h	WP09H1	8	Lower 8 bits of X-axis on the position of white blemish 10.
A5h	WP09H2	1	MSB of X-axis on the position of white blemish 10.
A6h	WP09V1	8	Lower 8 bits of Y-axis on the position of white blemish 10.
A7h	WP09V2	1	MSB of Y-axis on the position of white blemish 10.
A8h	WP0AH1	8	Lower 8 bits of X-axis on the position of white blemish 11.
A9h	WP0AH2	1	MSB of X-axis on the position of white blemish 11.
AAh	WP0AV1	8	Lower 8 bits of Y-axis on the position of white blemish 11.
ABh	WP0AV2	1	MSB of Y-axis on the position of white blemish 11.
ACh	WP0BH1	8	Lower 8 bits of X-axis on the position of white blemish 12.
ADh	WP0BH2	1	MSB of X-axis on the position of white blemish 12.
AEh	WP0BV1	8	Lower 8 bits of Y-axis on the position of white blemish 12.
AFh	WP0BV2	1	MSB of Y-axis on the position of white blemish 12.
B0h	WP0CH1	8	Lower 8 bits of X-axis on the position of white blemish 13.
B1h	WP0CH2	1	MSB of X-axis on the position of white blemish 13.
B2h	WP0CV1	8	Lower 8 bits of Y-axis on the position of white blemish 13.
B3h	WP0CV2	1	MSB of Y-axis on the position of white blemish 13.
B4h	WP0DH1	8	Lower 8 bits of X-axis on the position of white blemish 14.
B5h	WP0DH2	1	MSB of X-axis on the position of white blemish 14.
B6h	WP0DV1	8	Lower 8 bits of Y-axis on the position of white blemish 14.
B7h	WP0DV2	1	MSB of Y-axis on the position of white blemish 14.
B8h	WP0EH1	8	Lower 8 bits of X-axis on the position of white blemish 15.
B9h	WP0EH2	1	MSB of X-axis on the position of white blemish 15.
BAh	WP0EV1	8	Lower 8 bits of Y-axis on the position of white blemish 15.
BBh	WP0EV2	1	MSB of Y-axis on the position of white blemish 15.
BCh	WP0FH1	8	Lower 8 bits of X-axis on the position of white blemish 16.
BDh	WP0FH2	1	MSB of X-axis on the position of white blemish 16.
BEh	WP0FV1	8	Lower 8 bits of Y-axis on the position of white blemish 16.
BFh	WP0FV2	1	MSB of Y-axis on the position of white blemish 16.
C0h	WP10H1	8	Lower 8 bits of X-axis on the position of white blemish 17.
C1h	WP10H2	1	MSB of X-axis on the position of white blemish 17.
C2h	WP10V1	8	Lower 8 bits of Y-axis on the position of white blemish 17.
C3h	WP10V2	1	MSB of Y-axis on the position of white blemish 17.
C4h	WP11H1	8	Lower 8 bits of X-axis on the position of white blemish 18.
C5h	WP11H2	1	MSB of X-axis on the position of white blemish 18.
C6h	WP11V1	8	Lower 8 bits of Y-axis on the position of white blemish 18.
C7h	WP11V2	1	MSB of Y-axis on the position of white blemish 18.
C8h	WP12H1	8	Lower 8 bits of X-axis on the position of white blemish 19.
C9h	WP12H2	1	MSB of X-axis on the position of white blemish 19.
CAh	WP12V1	8	Lower 8 bits of Y-axis on the position of white blemish 19.
CBh	WP12V2	1	MSB of Y-axis on the position of white blemish 19.
CCh	WP13H1	8	Lower 8 bits of X-axis on the position of white blemish 20.

ADDRESS	NAME	BITS	FUNCTION
CDh	WP13H2	1	MSB of X-axis on the position of white blemish 20.
CEh	WP13V1	8	Lower 8 bits of Y-axis on the position of white blemish 20.
CFh	WP13V2	1	MSB of Y-axis on the position of white blemish 20.
D0h	WP14H1	8	Lower 8 bits of X-axis on the position of white blemish 21.
D1h	WP14H2	1	MSB of X-axis on the position of white blemish 21.
D2h	WP14V1	8	Lower 8 bits of Y-axis on the position of white blemish 21.
D3h	WP14V2	1	MSB of Y-axis on the position of white blemish 21.
D4h	WP15H1	8	Lower 8 bits of X-axis on the position of white blemish 22.
D5h	WP15H2	1	MSB of X-axis on the position of white blemish 22.
D6h	WP15V1	8	Lower 8 bits of Y-axis on the position of white blemish 22.
D7h	WP15V2	1	MSB of Y-axis on the position of white blemish 22.
D8h	WP16H1	8	Lower 8 bits of X-axis on the position of white blemish 23.
D9h	WP16H2	1	MSB of X-axis on the position of white blemish 23.
DAh	WP16V1	8	Lower 8 bits of Y-axis on the position of white blemish 23.
DBh	WP16V2	1	MSB of Y-axis on the position of white blemish 23.
DCh	WP17H1	8	Lower 8 bits of X-axis on the position of white blemish 24.
DDh	WP17H2	1	MSB of X-axis on the position of white blemish 24.
DEh	WP17V1	8	Lower 8 bits of Y-axis on the position of white blemish 24.
DFh	WP17V2	1	MSB of Y-axis on the position of white blemish 24.
E0h	WP18H1	8	Lower 8 bits of X-axis on the position of white blemish 25.
E1h	WP18H2	1	MSB of X-axis on the position of white blemish 25.
E2h	WP18V1	8	Lower 8 bits of Y-axis on the position of white blemish 25.
E3h	WP18V2	1	MSB of Y-axis on the position of white blemish 25.
E4h	WP19H1	8	Lower 8 bits of X-axis on the position of white blemish 26.
E5h	WP19H2	1	MSB of X-axis on the position of white blemish 26.
E6h	WP19V1	8	Lower 8 bits of Y-axis on the position of white blemish 26.
E7h	WP19V2	1	MSB of Y-axis on the position of white blemish 26.
E8h	WP1AH1	8	Lower 8 bits of X-axis on the position of white blemish 27.
E9h	WP1AH2	1	MSB of X-axis on the position of white blemish 27.
EAh	WP1AV1	8	Lower 8 bits of Y-axis on the position of white blemish 27.
EBh	WP1AV2	1	MSB of Y-axis on the position of white blemish 27.
ECh	WP1BH1	8	Lower 8 bits of X-axis on the position of white blemish 28.
EDh	WP1BH2	1	MSB of X-axis on the position of white blemish 28.
EEh	WP1BV1	8	Lower 8 bits of Y-axis on the position of white blemish 28.
EFh	WP1BV2	1	MSB of Y-axis on the position of white blemish 28.
F0h	WP1CH1	8	Lower 8 bits of X-axis on the position of white blemish 29.
F1h	WP1CH2	1	MSB of X-axis on the position of white blemish 29.
F2h	WP1CV1	8	Lower 8 bits of Y-axis on the position of white blemish 29.
F3h	WP1CV2	1	MSB of Y-axis on the position of white blemish 29.
F4h	WP1DH1	8	Lower 8 bits of X-axis on the position of white blemish 30.
F5h	WP1DH2	1	MSB of X-axis on the position of white blemish 30.

ADDRESS	NAME	BITS	FUNCTION
F6h	WP1DV1	8	Lower 8 bits of Y-axis on the position of white blemish 30.
F7h	WP1DV2	1	MSB of Y-axis on the position of white blemish 30.
F8h	WP1EH1	8	Lower 8 bits of X-axis on the position of white blemish 31.
F9h	WP1EH2	1	MSB of X-axis on the position of white blemish 31.
FAh	WP1EV1	8	Lower 8 bits of Y-axis on the position of white blemish 31.
FBh	WP1EV2	1	MSB of Y-axis on the position of white blemish 31.
FCh	WP1FH1	8	Lower 8 bits of X-axis on the position of white blemish 32.
FDh	WP1FH2	1	MSB of X-axis on the position of white blemish 32.
FEh	WP1FV1	8	Lower 8 bits of Y-axis on the position of white blemish 32.
FFh	WP1FV2	1	MSB of Y-axis on the position of white blemish 32.

Default Data Table

ADDRESS	DATA	ADDRESS	DATA	ADDRESS	DATA	ADDRESS	DATA
00h	–	20h	05	40h	00	60h	10
01h	–	21h	05	41h	40	61h	E0
02h	10	22h	FE	42h	04	62h	04
03h	00	23h	10	43h	00	63h	E0
04h	00	24h	FE	44h	04	64h	04
05h	00	25h	10	45h	00	65h	20
06h	30	26h	40	46h	80	66h	06
07h	03	27h	40	47h	00	67h	0B
08h	06	28h	40	48h	2D	68h	14
09h	3A	29h	40	49h	F9	69h	23
0Ah	04	2Ah	14	4Ah	39	6Ah	00
0Bh	08	2Bh	18	4Bh	ED	6Bh	–
0Ch	00	2Ch	20	4Ch	2D	6Ch	–
0Dh	00	2Dh	18	4Dh	F9	6Dh	–
0Eh	E7	2Eh	18	4Eh	39	6Eh	–
0Fh	00	2Fh	12	4Fh	ED	6Fh	00
10h	80	30h	0F	50h	2D	70h	–
11h	00	31h	0F	51h	F9	71h	–
12h	6B	32h	0E	52h	39	72h	–
13h	9A	33h	07	53h	ED	73h	–
14h	55	34h	14	54h	40	74h	–
15h	C0	35h	20	55h	40	75h	–
16h	80	36h	30	56h	40	76h	–
17h	80	37h	3C	57h	40	77h	–
18h	40	38h	48	58h	40	78h	–
19h	40	39h	5A	59h	40	79h	–
1Ah	04	3Ah	78	5Ah	04	7Ah	–
1Bh	FE	3Bh	B4	5Bh	04	7Bh	–
1Ch	02	3Ch	DE	5Ch	00	7Ch	–
1Dh	02	3Dh	00	5Dh	00	7Dh	–
1Eh	02	3Eh	00	5Eh	F0	7Eh	–
1Fh	02	3Fh	00	5Fh	08	7Fh	–

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Power supply voltage	V_{DD}	−0.3 to +4.3	V
Input voltage	V_I	−0.3 to V_{DD} + 0.3	V
Output voltage	V_O	−0.3 to V_{DD} + 0.3	V
Storage temperature	T_{STG}	−55 to +150	˚C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Power supply voltage	V_{DD}	2.7	3.0	3.3	V
Operating temperature	T_{OPR}	−20	+25	+70	˚C
Input clock frequency	f_{CK}		9.0		MHz

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.0±0.3 V, T_{OPR} = −20 to +70 ˚C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}				0.2V_{DD}	V	1
Input "High" voltage	V_{IH}		0.8V_{DD}			V	
Input "Low" current	$\lvert I_{IL1} \rvert$	V_{IN} = 0 V			1.0	µA	2
Input "High" current	$\lvert I_{IH1} \rvert$	V_{IN} = V_{DD}			1.0	µA	
Input "Low" current	$\lvert I_{IL2} \rvert$	V_I = 0 V	40	100	300	µA	3
Input "High" current	$\lvert I_{IH2} \rvert$	V_{IN} = V_{DD}			2.0	µA	
Output "Low" voltage	V_{OL}	I_{OL} = 4 mA			0.2V_{DD}	V	4
Output "High" voltage	V_{OH}	I_{OH} = −4 mA	0.8V_{DD}			V	

NOTES :

1. Applied to input (IC) and inputs/outputs (IO4M, IO4MU).
2. Applied to input (IC) and input/output (IO4M).
3. Applied to input/output (IO4MU).
4. Applied to output (OBF4M) and inputs/outputs (IO4M, IO4MU).

(APPENDIX)

Weighting area of exposure control

1 block = 44 pixels in horizontal and 36 lines in vertical

① (Bit 3, Bit 2) of address 0Ch = (0, 0)

2/4	2/4	2/4	2/4	2/4	2/4	2/4	2/4
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
1	1	5/4	5/4	5/4	5/4	1	1
1	1	5/4	5/4	5/4	5/4	1	1
1	1	5/4	5/4	5/4	5/4	1	1
1	1	5/4	5/4	5/4	5/4	1	1
1	1	1	1	1	1	1	1

② (Bit 3, Bit 2) of address 0Ch = (0, 1)

2/4	2/4	2/4	2/4	2/4	2/4	2/4	2/4
3/4	3/4	3/4	3/4	3/4	3/4	3/4	3/4
3/4	5/4	5/4	5/4	5/4	5/4	5/4	3/4
3/4	5/4	5/4	5/4	5/4	5/4	5/4	3/4
3/4	5/4	5/4	5/4	5/4	5/4	5/4	3/4
3/4	5/4	5/4	5/4	5/4	5/4	5/4	3/4
3/4	5/4	5/4	5/4	5/4	5/4	5/4	3/4
3/4	5/4	5/4	5/4	5/4	5/4	5/4	3/4

③ (Bit 3, Bit 2) of address 0Ch = (1, 0)

1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1

④ (Bit 3, Bit 2) of address 0Ch = (1, 1)

2/4	2/4	2/4	2/4	2/4	2/4	2/4	2/4
2/4	2/4	2/4	2/4	2/4	2/4	2/4	2/4
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
5/4	5/4	5/4	5/4	5/4	5/4	5/4	5/4
5/4	5/4	5/4	5/4	5/4	5/4	5/4	5/4
5/4	5/4	5/4	5/4	5/4	5/4	5/4	5/4
5/4	5/4	5/4	5/4	5/4	5/4	5/4	5/4

PACKAGE

(Unit : mm)

80 LQFP (LQFP080-P-1212)