HN62W448N Series

524288-word × 16-bit/1048576-word × 8-bit CMOS Mask Programmable ROM

HITACHI

ADE-203-484(A) (Z)
Preliminary
Rev. 0.1
Jun. 20, 1996

Description

The Hitachi HN62W448N is a 8-Mbit CMOS mask-programmable ROM organized either as 524288-words by 16-bits or as 1048576-words by 8-bits. Realizing low power consumption with low voltage operation, this memory is allowed for battery operation. And low voltage high speed page access of 60/70 ns and normal access of 120/150 ns are realized.

Features

- Low voltage operation : 3.3 V ± 0.3 V
- Access time:
  - — Normal access time: 120/150 ns (max)
  - — Page access time: 60/70 ns (max)
- Low power dissipation
  - — Active: 220 mW (max)
  - — Standby: 3 μW (max)
- Byte-wide or word-wide data organization (Switched by BHE terminal)
- 4-word page access mode
- Three-state data output for wired or-tying
- Directly LVTTL compatible (All inputs and outputs)

Preliminary: This document contains information an a new product. Specifications and information contained herein are subject to change without notice.

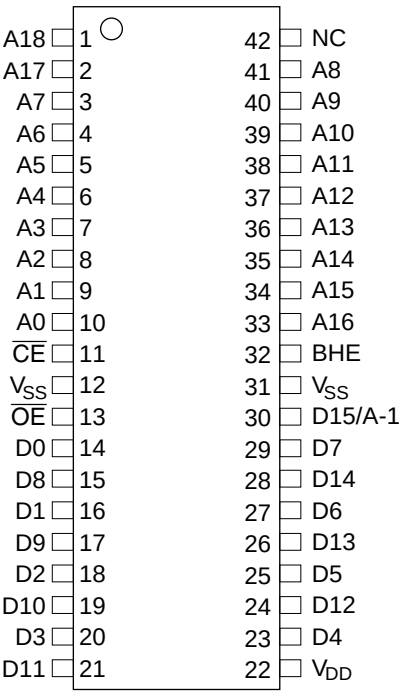
Hitachi semiconductor

Ordering Information

Type No.	Access time	Package
HN62W448NP-12 HN62W448NP-15	120 ns 150 ns	600mil 42-pin plastic DIP (DP-42)
HN62W448NFB-12 HN62W448NFB-15	120 ns 150 ns	44-pin plastic SOP (FP-44D)
HN62W448NTT-12 HN62W448NTT-15	120 ns 150 ns	44-pin plastic TSOP II (TTP-44D)

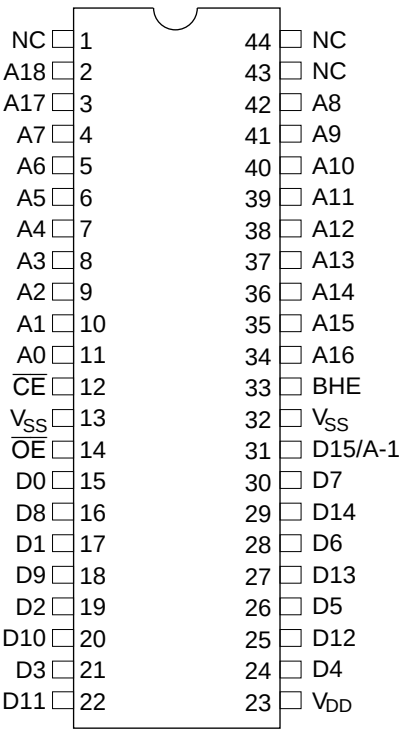
Pin Arrangement

HN62W448NP Series



(Top view)

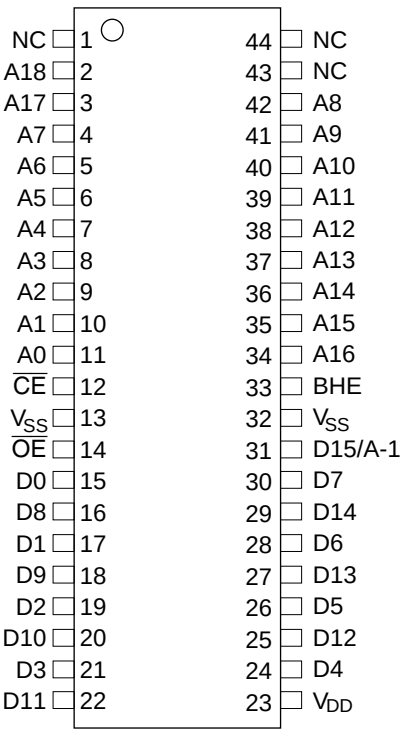
HN62W448NFB Series



(Top view)

Pin Arrangement (cont.)

HN62W448NTT Series

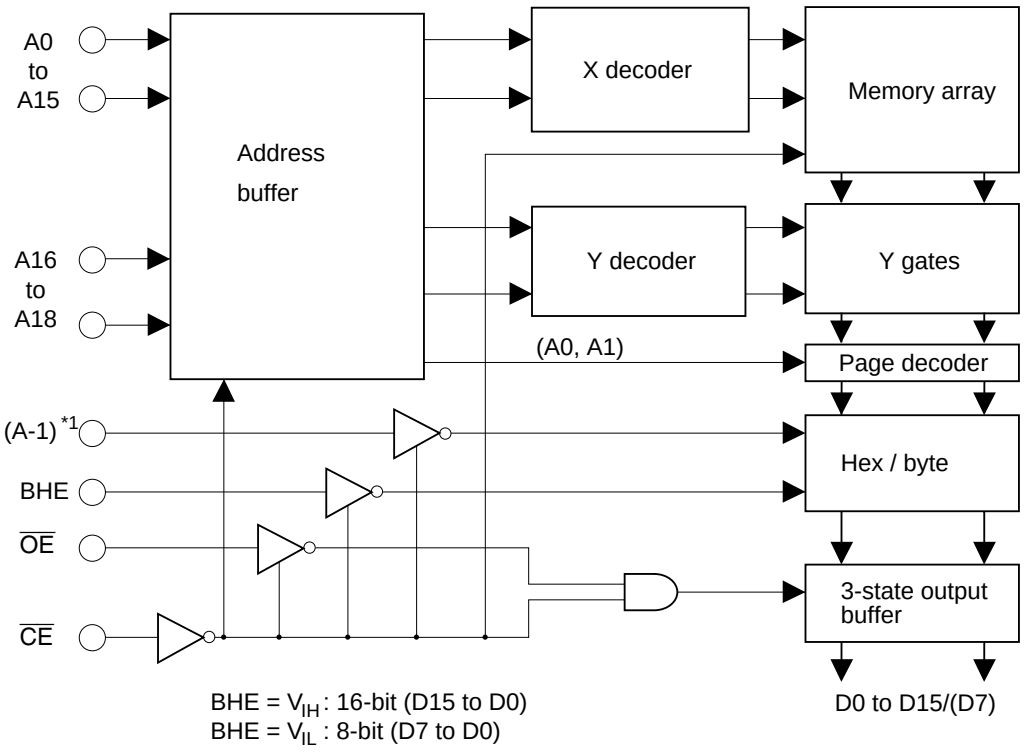


(Top view)

Pin Description

Pin name	Function
A0 to A18	Address
D0 to D14	Output
D15/A-1	Output/address
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
BHE	Byte/word selection
V_{DD}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram



Note: 1. A-1 is least significant address.
When BHE is 'low', D14 to D8 goes the high impedance state.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Supply voltage	V_{DD}	–0.3 to +5.5	V	1
All input and output voltage	Vin, Vout	–0.3 to V_{DD} +0.3	V	1
Operating temperature range	Topr	0 to 70	°C	
Storage temperature range	Tstg	–55 to +125	°C	
Temperature under bias	Tbias	–20 to +85	°C	

Note: 1. With respect to V_{SS}.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	V_{DD} + 0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Characteristics (V_{DD} = 3.3 V ± 0.3V, V_{SS} = 0 V, Ta = 0 to +70°C)

Parameter		Symbol	Min	Max	Unit	Test conditions
Supply current	Active	I_{DD}	—	60	mA	V_{DD} = 3.6 V, I_{DOUT} = 0 mA, t_{RC} = 120/150 ns
	Standby	I_{SB1}	—	30	µA	V_{DD} = 3.6 V, $\overline{CE} \geq V_{DD}$ –0.2 V
	Standby	I_{SB2}	—	3	mA	V_{DD} = 3.6 V, $\overline{CE}$ = 2.2 V
Input leakage current		$\|I_{IL}\|$	—	10	µA	Vin = 0 to V_{DD}
Output leakage current		$\|I_{OL}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{DD}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –2.0 mA
		V_{OL}	—	0.4	V	I_{OL} = 2.0 mA

Capacitance (V_{DD} = 3.3 V ± 0.3V, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	10	pF
Output capacitance*1	Cout	—	15	pF

Note: 1. This parameter is periodically sampled and not 100% tested.

AC Characteristics (V_{DD} = 3.3 V ± 0.3V, V_{SS} = 0 V, Ta = 0 to + 70°C)

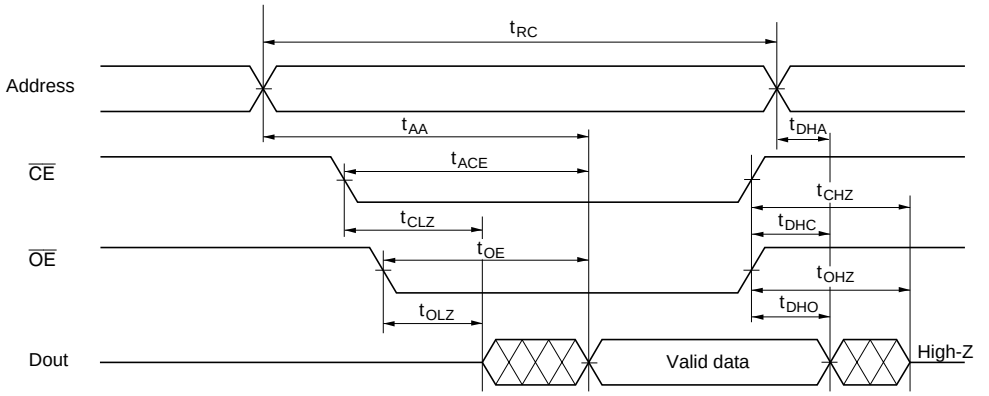
- Output load: 1TTL gate + C_L = 50 pF (including scope & jig)
- Input pulse levels: 0.4 to 2.4 V
- Input and output timing reference levels: 1.4V
- Input rise and fall time: 5 ns

		HN62W448N-12		HN62W448N-15		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	120	—	150	—	ns
Page read cycle time	t_{PC}	50	—	70	—	ns
Address access time	t_{AA}	—	120	—	150	ns
Page address access time	t_{PA}	—	50	—	70	ns
$\overline{CE}$ access time	t_{ACE}	—	120	—	150	ns
$\overline{OE}$ access time	t_{OE}	—	50	—	70	ns
BHE access time	t_{BHE}	—	120	—	150	ns
Output hold time from address change	t_{DHA}	0	—	0	—	ns
Output hold time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns
Output hold time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns
Output hold time from BHE	t_{DHB}	0	—	0	—	ns
$\overline{CE}$ to output in high-Z	t_{CHZ} *1	—	50	—	70	ns
$\overline{OE}$ to output in high-Z	t_{OHZ} *1	—	50	—	70	ns
BHE to output in high-Z	t_{BHZ} *1	—	50	—	70	ns
$\overline{CE}$ to output in low-Z	t_{CLZ}	5	—	5	—	ns
$\overline{OE}$ to output in low-Z	t_{OLZ}	5	—	5	—	ns
BHE to output in low-Z	t_{BLZ}	5	—	5	—	ns

Note: 1. t_{CHZ}, t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

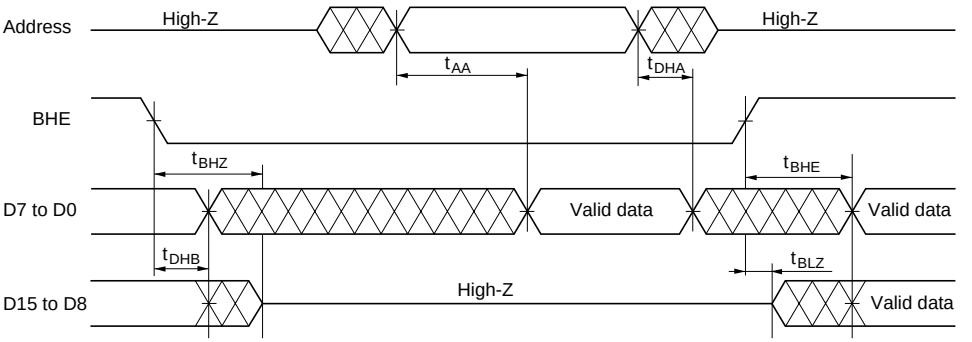
Timing Waveforms

Word Mode (BHE = 'V_{IH}') **or Byte Mode** (BHE = 'V_{IL}')



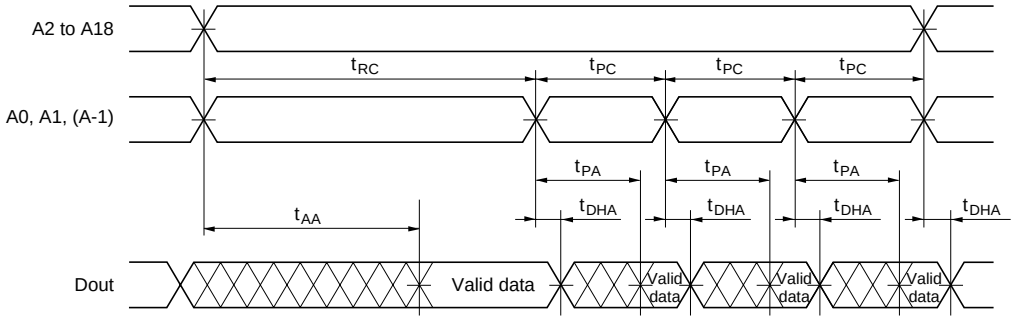
Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}: Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}: Determined by slower.
3. t_{CLZ}, t_{OLZ}: Determined by slower.

Word Mode, Byte Mode Switch



Notes: 1. $\overline{CE}$ and $\overline{OE}$ are enable A18 to A0 are valid.
2. D15/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable.
Therefore, the input signals of opposite phase to the output must not be applied to them.

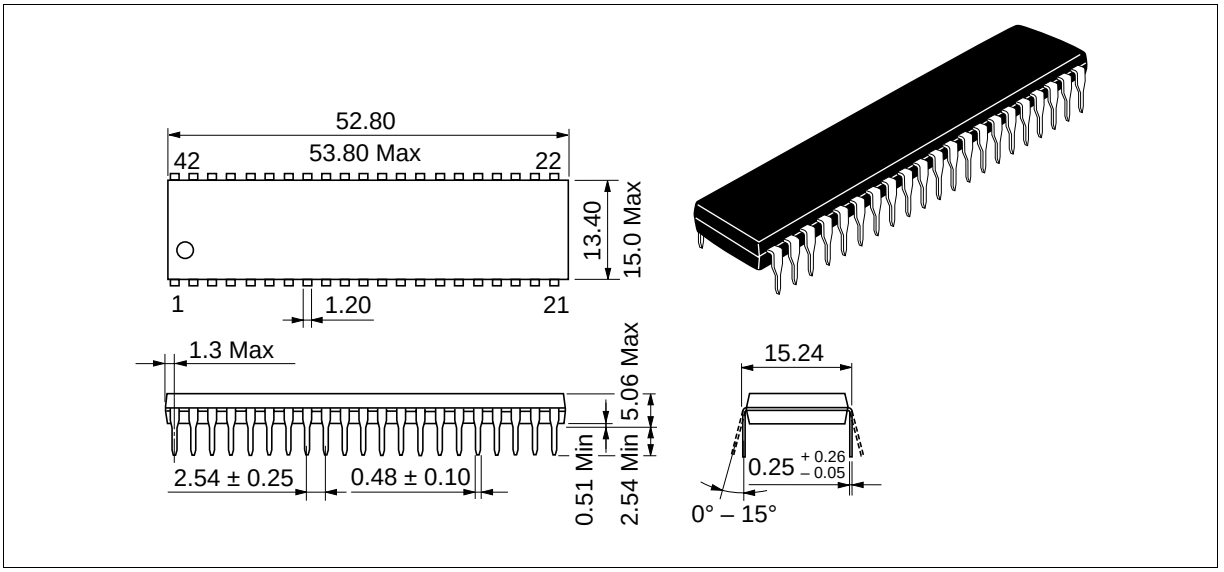
Page Mode



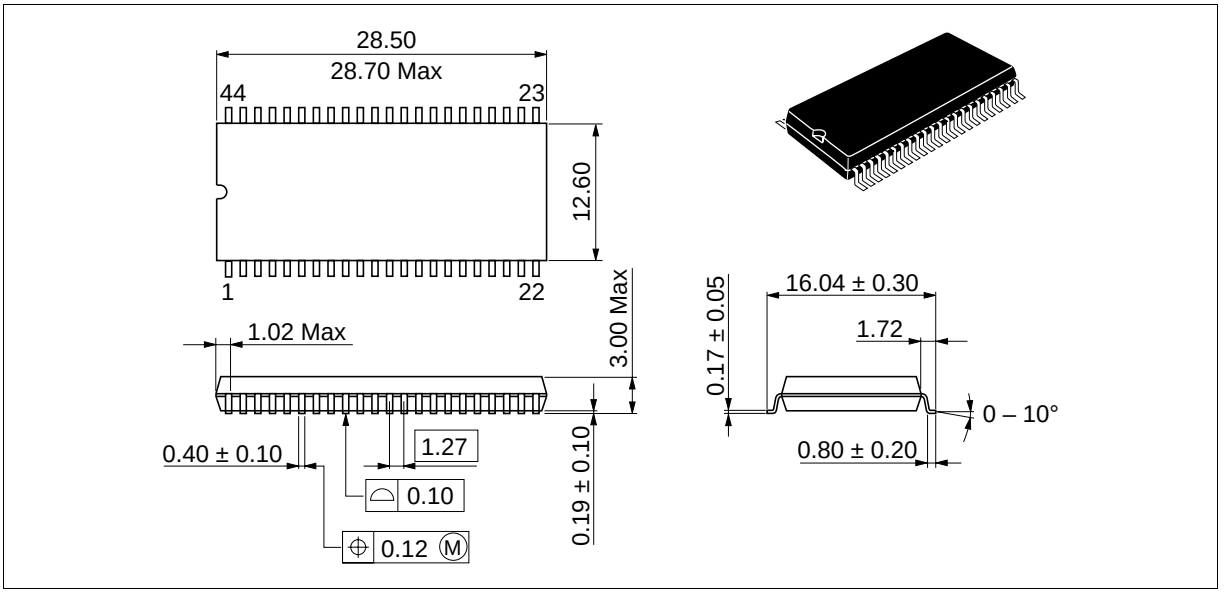
Note: $\overline{CE}$ and $\overline{OE}$ are enable.

Package Dimensions

HN62W448NP Series (DP-42) Unit: mm

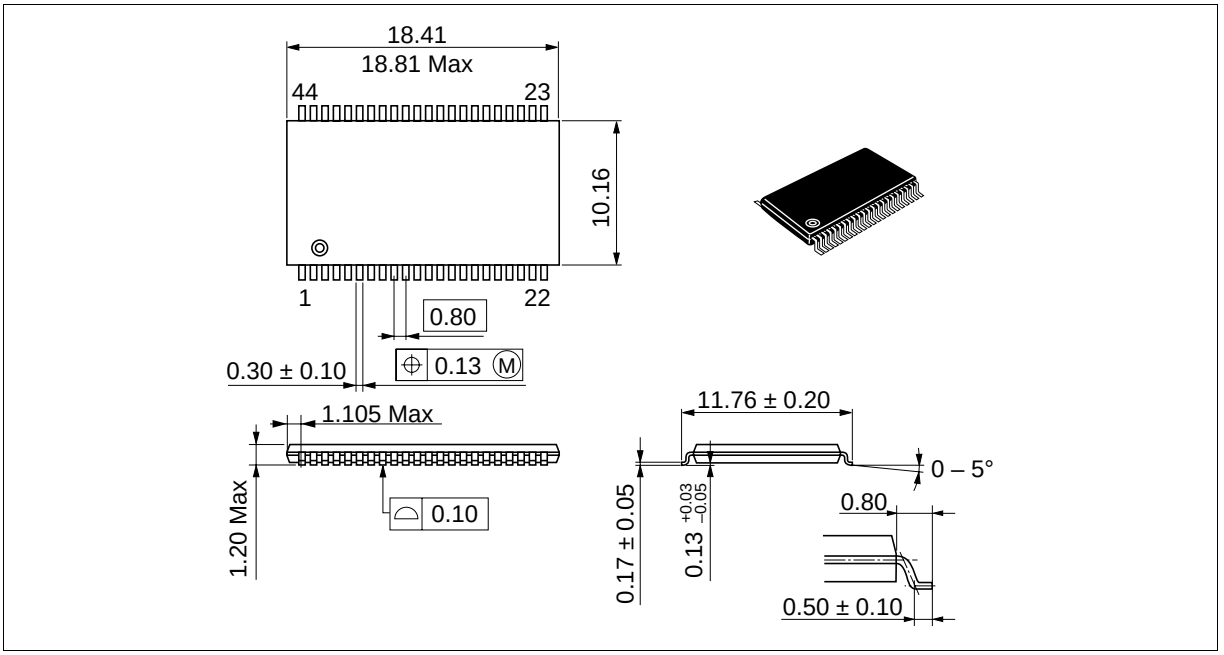


HN62W448NFB Series (FP-44D) Unit: mm



Package Dimensions (cont.)

HN62W448NTT Series (TTP-44D) Unit: mm



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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Nov. 22, 1995	Initial issue	Y. Yamada	T. Wada
0.1	Jun. 20, 1996	AC Characteristics Output load: 1TTL + C_L = 100 pF to 1TTL + C_L = 50 pF t_{PC} min: 60/70 ns to 50/70 ns t_{PA}, t_{OE}, t_{CHZ}, t_{OHZ}, t_{BHZ} max: 60/70 ns to 50/70 ns Deletion of timing waveform for power up sequence		