

MB88352

R-2R TYPE 12-BIT D/A CONVERTER WITH OPERATIONAL AMPLIFIER OUTPUT BUFFER

DESCRIPTION

The Fujitsu MB88352 is an R-2R type 12-bit resolution digital-to-analog converter (DAC), designed for interface with a wide range of general 4-bit and 8-bit microcontrollers including Fujitsu's MB88200 family, MB8850 family, and MB88500 family 4-bit single-chip microcontrollers.

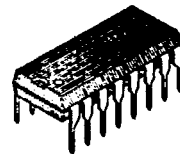
The MB88352 has 12-bit resolution 2 channels D/A converters; an 12-bit x 1 channel D/A converter and an 12-bit x 1 channel D/A converter with an operational amplifier output buffer. Digital data are input serially by individual channel units. The loaded digital data are converted into analog DC voltages by the D/A converter in maximum 30 μ s settling time. Also, the MB88352 has an operational amplifier output buffer. This operational amplifier output buffer is connected to a channel of the D/A converter, and provides high current drive capability. The MB88352 is suitable for electronic volumes and replacement for potentiometers for adjustment, in addition to normal D/A converter applications.

FEATURES

- Conversion method : R-2R resistor ladder
- 12-bit x 2 channels D/A converters:
 - 12-bit x 1 channel DAC : with an operational amplifier output buffer
 - 12-bit x 1 channel DAC : without an operational amplifier output buffer
- Max. 2.5MHz Serial data input
- Serial data output for cascade connection
- Max. 30 μ s DAC output settling time
- Max. +1.0/-1.0 mA analog output sink/source current
- Two separate power supply/ground lines for MCU interface block/operational amplifier output buffer block and D/A converter block
- Low power consumption : Typ. 13.8 mW
- Single +5V power supply
- Wide operating temperature range: -20°C to +85°C
- Silicon-gate CMOS process
- Three package options :
 - 16-pin plastic DIP (Suffix : -P), 16-pin plastic SOP (Suffix : -PF),
 - 20-pin plastic SSOP (Suffix : -PFV)

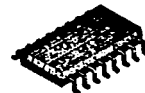
PRELIMINARY

MB88352-P



PLASTIC DIP
(DIP-16P-M04)

MB88352-PF



PLASTIC SOP
(FPT-16P-M06)

MB88352-PFV



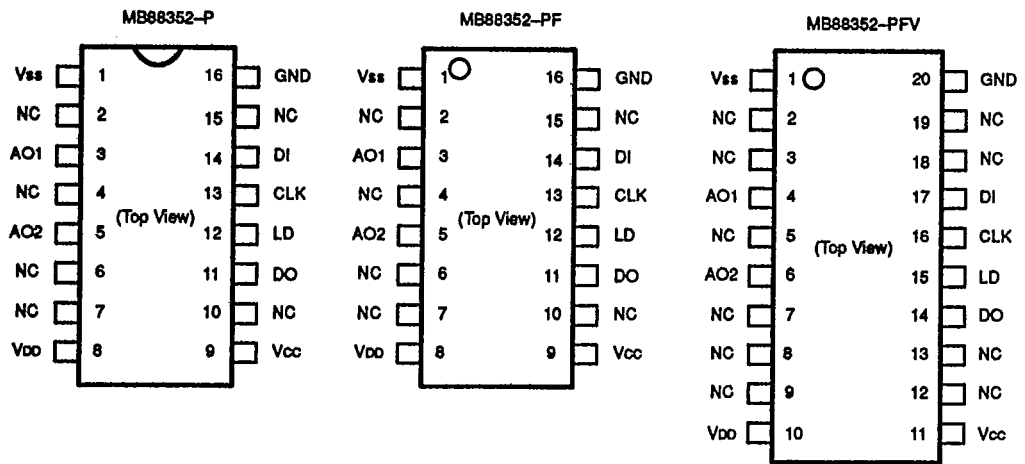
PLASTIC SSOP
(FPT-20P-M03)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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Figure 1 Pin Assignment



Note:
NC : No connection

Figure 2 Logic Symbol

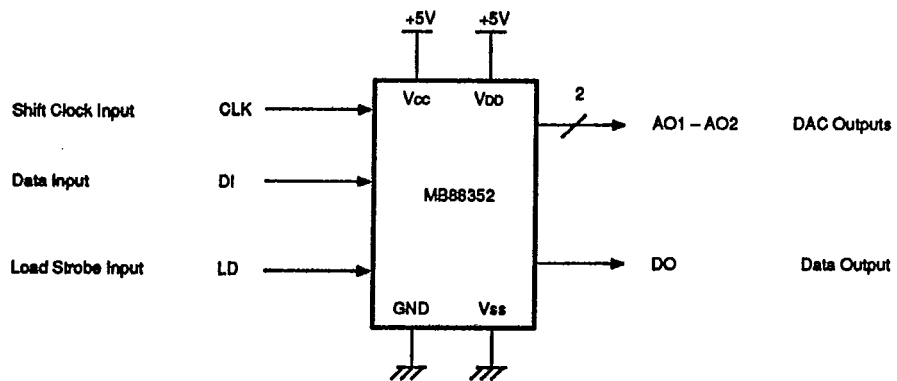
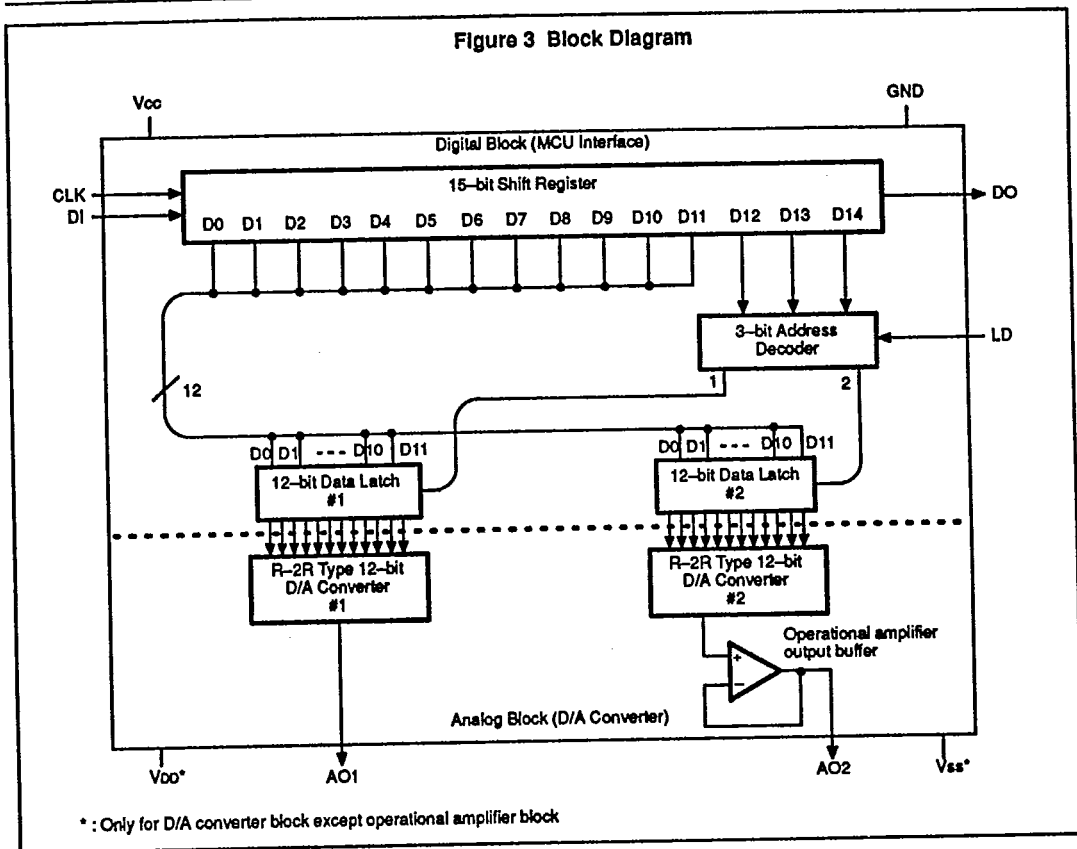


Figure 3 Block Diagram



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PIN DESCRIPTION

Figure 1 and Table 1 show the pin assignment and pin description of the MB88352.

Table 1 Pin Description

| Symbol | Pin No. | | Type | Name & Function |
|--------------------------|--------------------------|---|------|--|
| | DIP/SOP | SSOP | | |
| Power Supply | | | | |
| Vcc | 9 | 11 | - | +5V DC power supply pin for the digital block (MCU interface) and operational amplifier output buffer. |
| GND | 16 | 20 | - | Ground pin for the digital block (MCU interface) and operational amplifier output buffer. |
| V _{DO} | 8 | 10 | - | DC power supply pin for the analog block (D/A converter) except operational amplifier output buffer. |
| V _{SS} | 1 | 1 | - | Ground pin for the analog block (D/A converter) except operational amplifier output buffer. |
| Control Input | | | | |
| CLK | 13 | 16 | I | Shift clock input to the internal 15-bit shift register: At the rising edge of CLK data on the DI pin is shifted into the LSB of the shift register and contents of the shift register are shifted right (to the MSB). |
| LD | 12 | 15 | I | Load strobe input for a 15-bit address/data: A high level on the LD pin latches a 3-bit address (upper 3 bits: D14 to D12) of the internal 15-bit shift register into the internal address decoder, and writes 12-bit data (lower 12 bits: D11 to D0) of the shift register into an internal data latch selected by the latched address. |
| Data Input/Output | | | | |
| DI | 14 | 17 | I | Serial address/data input to the internal 15-bit shift register: The address/data format is that upper 3 bits (D14 to D12) indicate an address and lower 12 bits (D11 to D0) indicate data. The D14 (MSB) is the first-in bit and D0 (LSB) is the last-in bit. |
| DO | 11 | 14 | O | Serial address/data output from the internal 15-bit shift register: This is an output pin of the MSB bit data of the 15-bit shift register. This pin allows a cascade connection of the device. |
| DAC Output | | | | |
| AO1 AO2 | 3 5 | 4 6 | O | 12-bit resolution D/A converter outputs: 2 channels (AO1 and AO2) of DAC outputs are provided. AO2 has an operational amplifier output buffer for analog output data. AO1 does not have an operational amplifier output buffer. |
| Others | | | | |
| NC | 2, 4, 6, 7, 10, 15 | 2, 3, 5, 7, 8, 9, 12, 13, 18, 19 | - | No connection. They must be left open. |

FUNCTIONAL DESCRIPTION

OVERVIEW

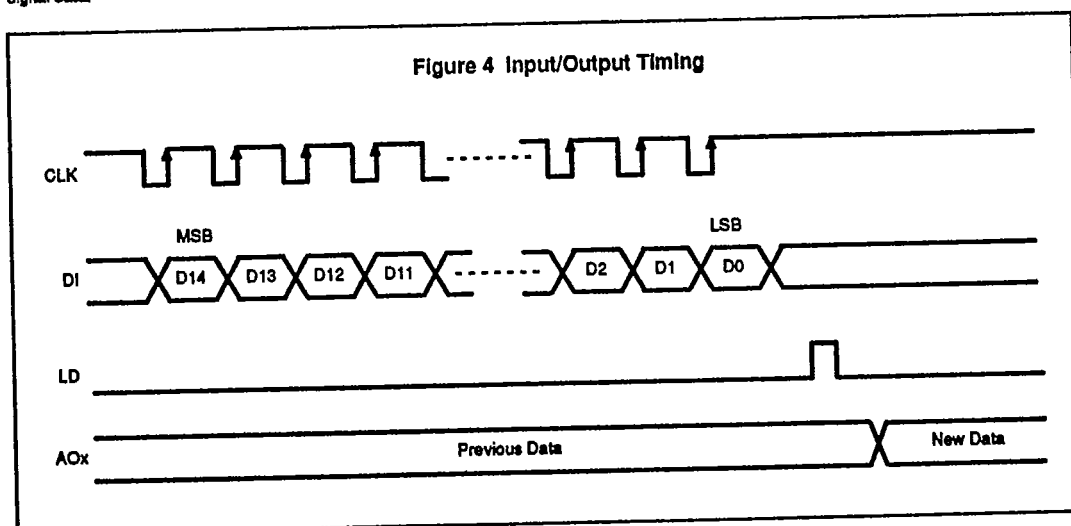
The MB88352 is an R-2R resistor ladder type, 12-bit resolution digital-to-analog converter (DAC) device. The MB88352 has 2 channels of D/A converters. As shown in Figure 3 Block Diagram, 1 channel of total 2 channels has an operational amplifier output buffer for analog output data. 12-bit digital data are loaded into internal data latches by individual DAC channel units. The loaded digital data are converted into analog DC voltages through the internal D/A converter in max. 30 μ s settling time. Furthermore, the analog DC voltages source/sink the output current through the operational amplifier output buffer. For cascade connection, a serial data output is provided.

DEVICE CONFIGURATION

As illustrated in Figure 3 block diagram, the MB88352 device is composed by the digital block (MCU interface) and analog block (D/A converter with an operational amplifier output buffer). The digital block consists of a 15-bit shift register, a 3-bit address decoder, and 2 channels of 12-bit data latches. The analog block includes 2 channels of 12-bit D/A converters. Of 2 channels DACs, 1 channel (AO2 pin) has an operational amplifier output buffer to provide an analog output high current drive capability. For electrically stable operation the power supply and ground lines are separate between the digital block (MCU interface) and an operational amplifier output buffer, and analog block except an operational amplifier output buffer.

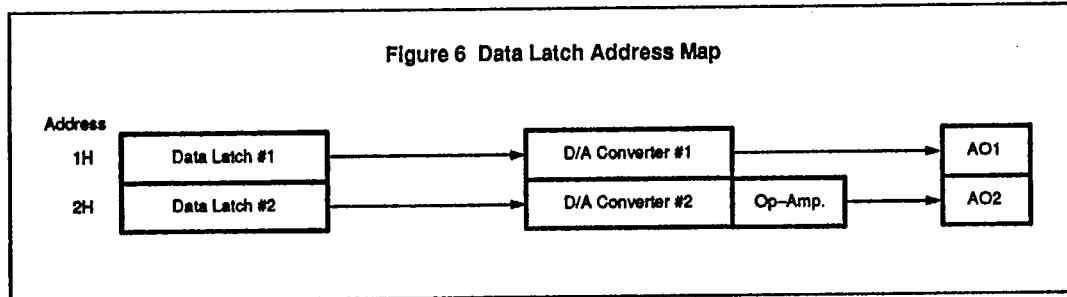
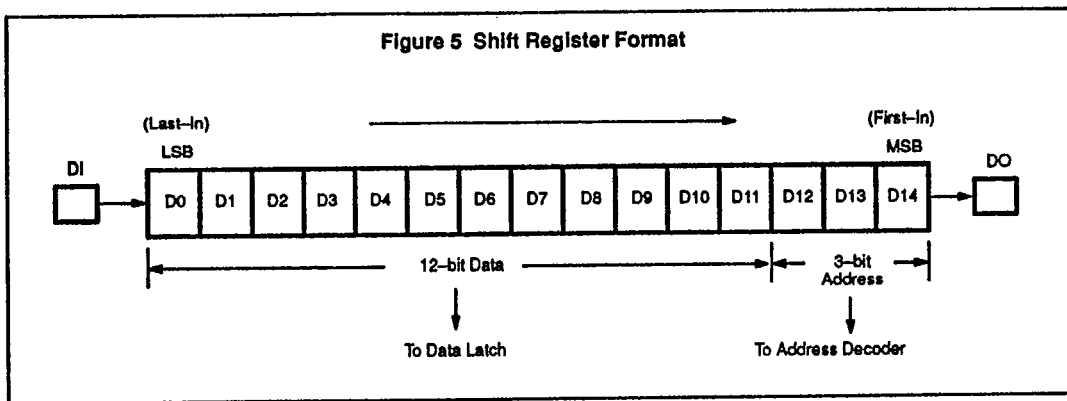
DEVICE OPERATION

Figure 4 shows the input/output timing. A 15-bit address/data is serially input into the shift register through the DI pin synchronously with the rising edge of CLK. The format of the shift register is shown in Figure 5. The lower 12 bits (D11 to D0) are data bits to be converted, and the upper 3 bits are address bits (D14 to D12) to select a data latch to be written. A high level on the LD pin loads the address decoder with the 3-bit address to select a data latch, and writes the 12-bit data into a selected data latch. Figure 6 shows the data latch address map, and Table 2 lists the address decoding. 12-bit data written into individual data latches are converted into analog DC voltages, dividing the supply voltage $[V_{CC}-V_{SS}]$ through R-2R resistor ladders of D/A converters. The operational amplifier output buffer at D/A converter #2 output (AO2 pin) can source up to 1 mA of the output current. Figure 7 shows a configuration of the R-2R resistor ladder D/A converter with an operational amplifier, and Table 3 lists the analog DC voltages corresponding to each digital data.



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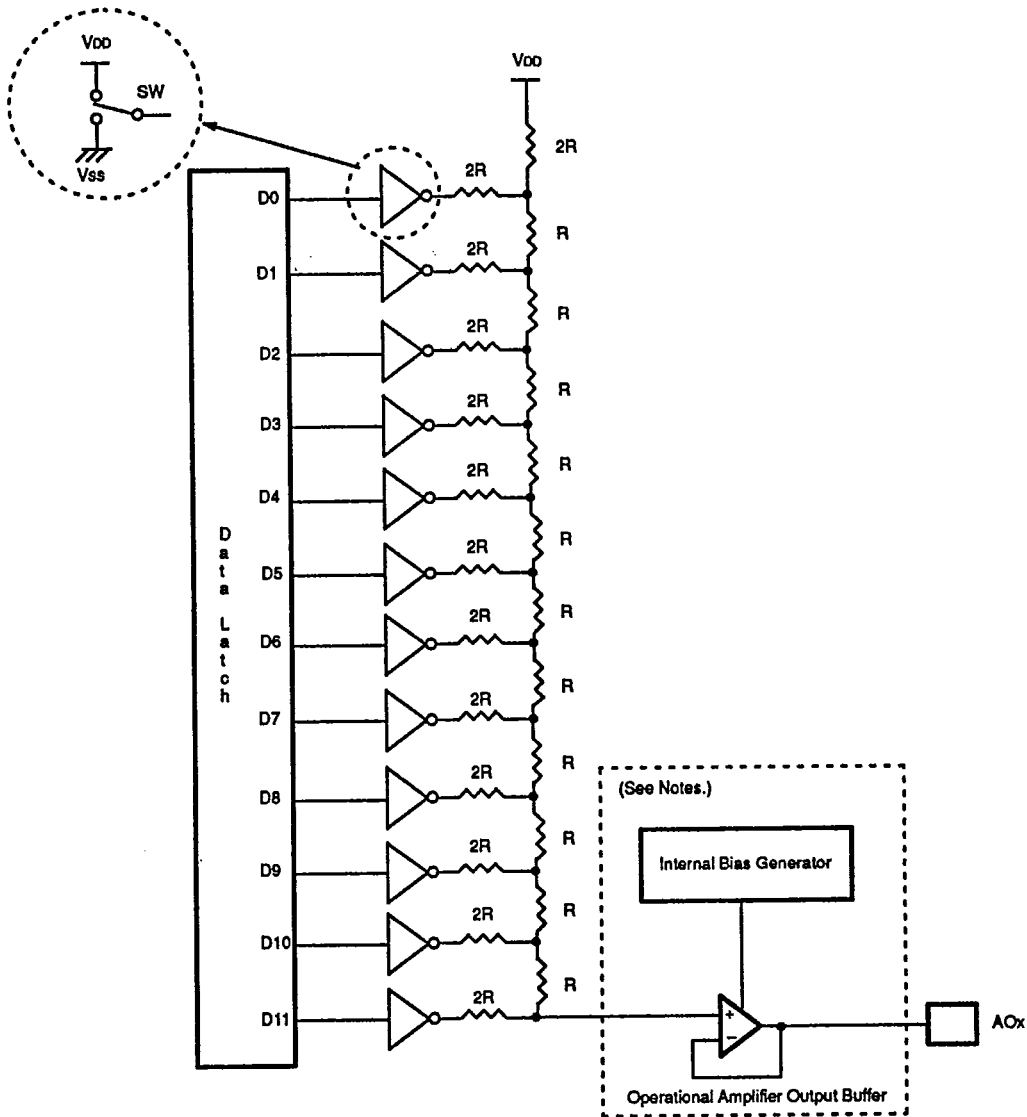
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Figure 7 Configuration of R-2R Resistor Ladder D/A Converter with Operational Amplifier Output Buffer



Notes : This operational amplifier output buffer is only available for 1 channel DAC (AO2 pin). Another DAC (AO1 pin) unit does not have an operational amplifier output buffer. Also, the operational amplifier output buffer is powered/grounded by the Vcc and GND pins.

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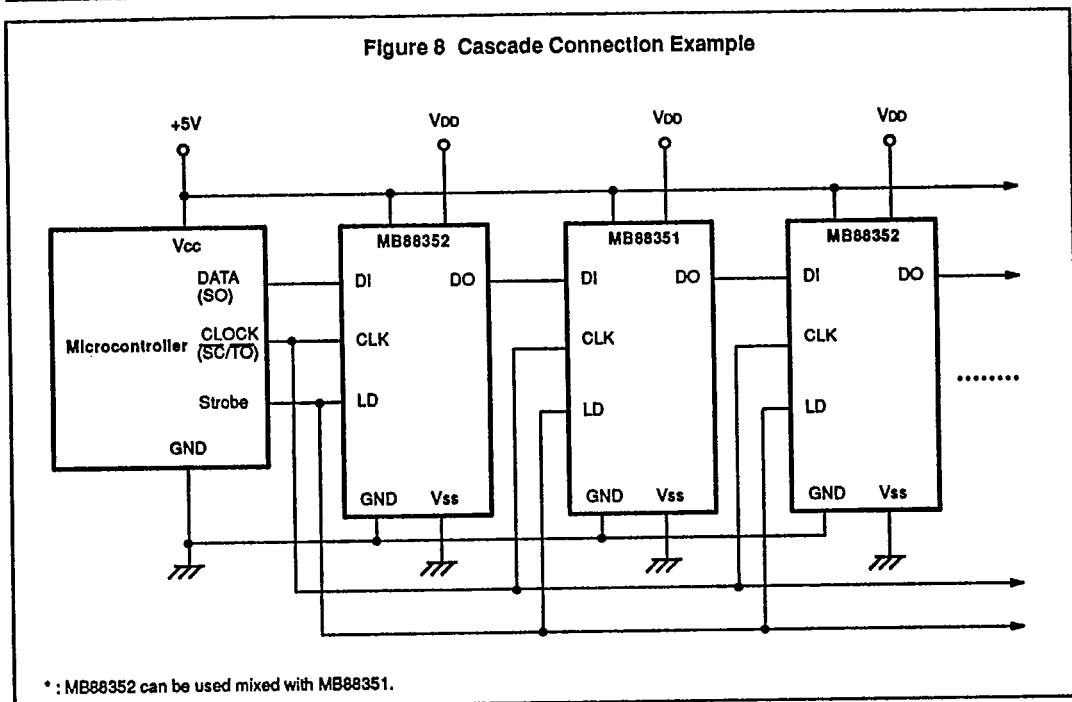
Table 2 Address Decoding

| Address | | | Data Latch Selected |
|---------|-----|-----|---------------------|
| D12 | D13 | D14 | MB88352 |
| 0 | 0 | 0 | Deselected |
| 0 | 0 | 1 | Data Latch #1 |
| 0 | 1 | 0 | Data Latch #2 |
| 0 | 1 | 1 | Deselected |
| 1 | 0 | 0 | Deselected |
| 1 | 0 | 1 | Deselected |
| 1 | 1 | 0 | Deselected |
| 1 | 1 | 1 | Deselected |

Table 3 Data Conversion

| Data | | | | | | | | | | | | DAC Output Level |
|------|-----|----|----|----|----|----|----|----|----|----|----|---|
| D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | AOx |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = Vss |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | $\approx (V_{DD} - V_{SS}) \times 1/4095 + V_{SS}$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | $\approx (V_{DD} - V_{SS}) \times 2/4095 + V_{SS}$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | $\approx (V_{DD} - V_{SS}) \times 3/4095 + V_{SS}$ |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | $\approx (V_{DD} - V_{SS}) \times 4092/4095 + V_{SS}$ |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | $\approx (V_{DD} - V_{SS}) \times 4093/4095 + V_{SS}$ |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | $\approx (V_{DD} - V_{SS}) \times 4094/4095 + V_{SS}$ |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | = VDD |

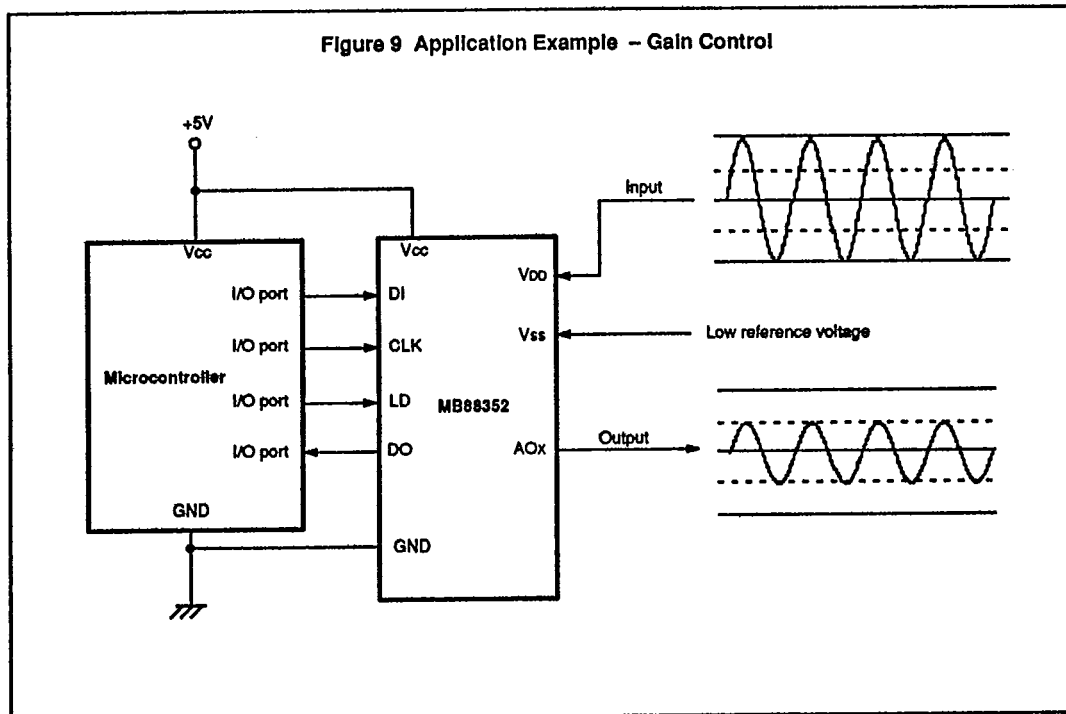
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APPLICATION DESCRIPTION

The MB88352 is suitable for electronic volumes and replacement for adjustment potentiometers, in addition to normal D/A converter applications. Figure 9 illustrates application example for a gain control.



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ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (See NOTE)

| Parameter | Symbol | Rating | | | Unit | Condition |
|-------------------------------|------------------|--------|-----|---------|------|--|
| | | Min | Typ | Max | | |
| Supply Voltage | Vcc | -0.3 | | 7.0 | V | Ta = +25°C GND = 0 V V _{DD} ≤ Vcc |
| | V _{DD} | -0.3 | | 7.0 | V | |
| Input Voltage | V _{IN} | -0.3 | | Vcc+0.3 | V | Ta = 25°C GND = 0 V Should not exceed Vcc + 0.3V |
| Output Voltage | V _{OUT} | -0.3 | | Vcc+0.3 | V | |
| Power Dissipation | P _D | | | 250 | mW | |
| Operating Ambient Temperature | T _A | -20 | | +85 | °C | |
| Storage Temperature | T _{STG} | -55 | | +150 | °C | |

NOTE : Permanent device damage may occur if the above ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Value | | | Unit | Condition |
|--|-----------------|-------|-----|-----------|------|---|
| | | Min | Typ | Max | | |
| Supply Voltage (for MCU Interface/ Op.-Amp. Block) | Vcc | 4.5 | 5.0 | 5.5 | V | Vcc ≥ V _{DD} |
| | GND | | 0 | | V | |
| Supply Voltage (for Analog Block*) | V _{DD} | 2.0 | | Vcc | V | Vcc ≥ V _{DD} , V _{DD} - V _{SS} ≥ 2.0V |
| | V _{SS} | GND | | Vcc - 2.0 | V | |
| Analog Output Source Current | I _{AL} | | | -1.0 | mA | |
| Analog Output Sink Current | I _{AH} | | | +1.0 | mA | |
| Analog Output Load Capacitance for oscillation limit | C _{AL} | | | 1.0 | μF | |
| Operating Ambient Temperature | T _A | -20 | | +85 | °C | |

* : Except operational amplifier output buffer block

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DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Digital Block (MCU Interface)

| Parameter | Symbol | Value | | | Unit | Condition |
|---|--------|---------|------|---------|------|----------------------|
| | | Min. | Typ. | Max. | | |
| Active Supply Current (Vcc) * | Icc | | 0.8 | 2.0 | mA | CLK = 1MHz, Unloaded |
| Input Leakage Current (CLK, DI, and LD) | ILK | -10 | | +10 | μA | VIN = 0 to Vcc |
| Input Low Voltage (CLK, DI, and LD) | VIL | | | 0.2*Vcc | V | |
| Input High Voltage (CLK, DI, and LD) | VIH | 0.8*Vcc | | | V | |
| Output Low Voltage (DC) | VOL | | | 0.4 | V | IOL = 2.5 mA |
| Output High Voltage (DC) | VOH | Vcc-0.4 | | | V | IOH = -400 μA |

* : Including the supply current to the operational amplifier block

Analog Block (D/A Converters with Operational Amplifier Output Buffer)

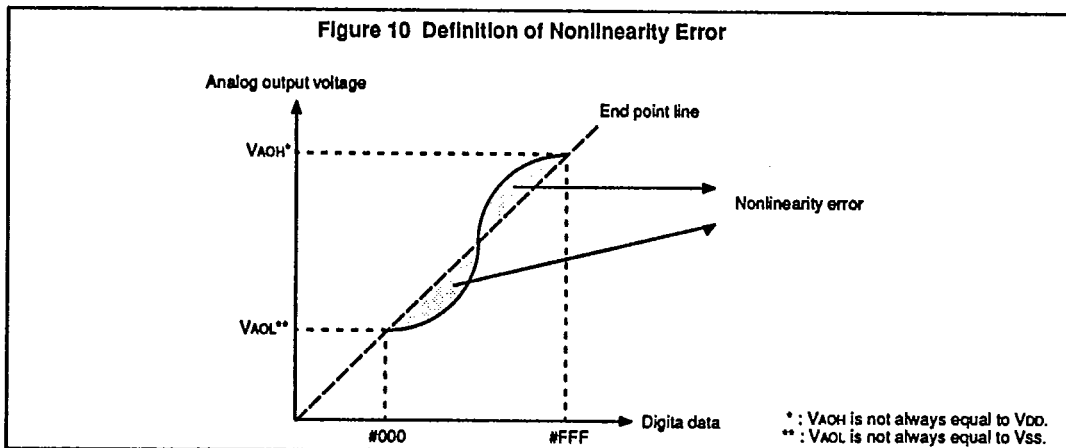
| Parameter | Symbol | Value | | | Unit | Condition |
|----------------------------------|--------|-------|------|---------|------|-----------------------------|
| | | Min. | Typ. | Max. | | |
| Supply Current (Vcc) ** | IDD | | 0.15 | 0.5 | mA | Unloaded |
| Analog Supply Voltage (VDD, VSS) | VDD | 2.0 | | Vcc | V | VDD-VSS≥2.0V |
| | VSS | GND | | Vcc-2.0 | V | |
| Resolution (AO1, AO2) | Res | | 12 | | bit | |
| Monotonicity (AO1, AO2) | Rem | | 9 | | bit | |
| Offset Error 1 (AO1) | RE01 | -5.0 | | +5.0 | mV | Unloaded |
| Offset Error 2 (AO2) | RE02 | -100 | | +100 | mV | Unloaded |
| Nonlinearity Error 1 (AO1) | ENL1 | -8.0 | | +8.0 | LSB | Digital Data = #000 to #AFF |
| | | -4.0 | | +4.0 | | Digital Data = #B00 to #FFF |
| Nonlinearity Error 2 (AO2) | ENL2 | -8.0 | | +8.0 | LSB | Digital Data = #000 to #AFF |
| | | -4.0 | | +4.0 | | Digital Data = #B00 to #FFF |

** : Excluding the supply current to the operational amplifier block

Analog Block (D/A Converters with Operational Amplifier Output Buffers) – Continued

| Parameter | Symbol | Pin/Port | Value | | | Unit | Condition |
|------------------------------------|--------|----------|-----------|-----|-----------|------|---|
| | | | Min | Typ | Max | | |
| Min. Analog Output Voltage 1 (AOx) | VAOL1 | AO1 | GND | | GND+0.005 | V | Unloaded, VDD=VCC, VSS=GND, Digital data=#000 |
| | | AO2 | GND | | GND+0.1 | | |
| Max. Analog Output Voltage 1 (AOx) | VAOH1 | AO1 | VCC-0.005 | | VCC | V | Unloaded, VDD=VCC, VSS=GND, Digital data=#FFF |
| | | AO2 | VCC-0.1 | | VCC | | |
| Min. Analog Output Voltage 2 (AOx) | VAOL2 | AO2 | GND | | GND+0.1 | V | VDD=VCC=5.0V, VSS=GND=0V, IAL=-400μA, Digital data=#000 |
| Min. Analog Output Voltage 3 (AOx) | VAOL3 | AO2 | GND | | GND+0.3 | V | VDD=VCC=5.0V, VSS=GND=0V, IAL=-1.0mA, Digital data=#000 |
| Min. Analog Output Voltage 4 (AOx) | VAOL4 | AO2 | GND-0.1 | GND | GND+0.1 | V | VDD=VCC=5.0V, VSS=GND=0V, IAH=+400μA, Digital data=#000 |
| Min. Analog Output Voltage 5 (AOx) | VAOL5 | AO2 | GND-0.3 | GND | GND+0.3 | V | VDD=VCC=5.0V, VSS=GND=0V, IAH=+1.0mA, Digital data=#000 |
| Max. Analog Output Voltage 2 (AOx) | VAOH2 | AO2 | VCC-0.1 | VCC | VCC+0.1 | V | VDD=VCC=5.0V, VSS=GND=0V, IAL=-400μA, Digital data=#FFF |
| Max. Analog Output Voltage 3 (AOx) | VAOH3 | AO2 | VCC-0.3 | VCC | VCC+0.3 | V | VDD=VCC=5.0V, VSS=GND=0V, IAL=-1.0mA, Digital data=#FFF |
| Max. Analog Output Voltage 4 (AOx) | VAOH4 | AO2 | VCC-0.1 | | VCC | V | VDD=VCC=5.0V, VSS=GND=0V, IAH=+400μA, Digital data=#FFF |
| Max. Analog Output Voltage 5 (AOx) | VAOH5 | AO2 | VCC-0.3 | | VCC | V | VDD=VCC=5.0V, VSS=GND=0V, IAH=+1.0mA, Digital data=#FFF |

Figure 10 Definition of Nonlinearity Error



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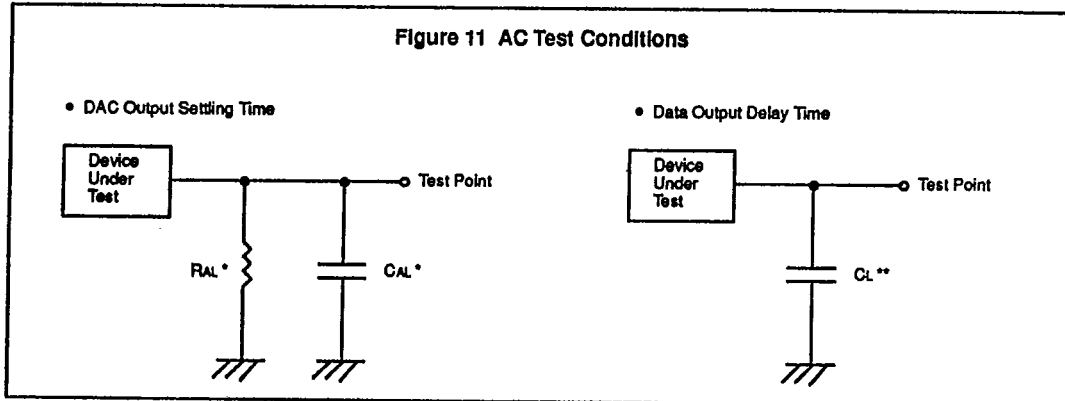
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AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

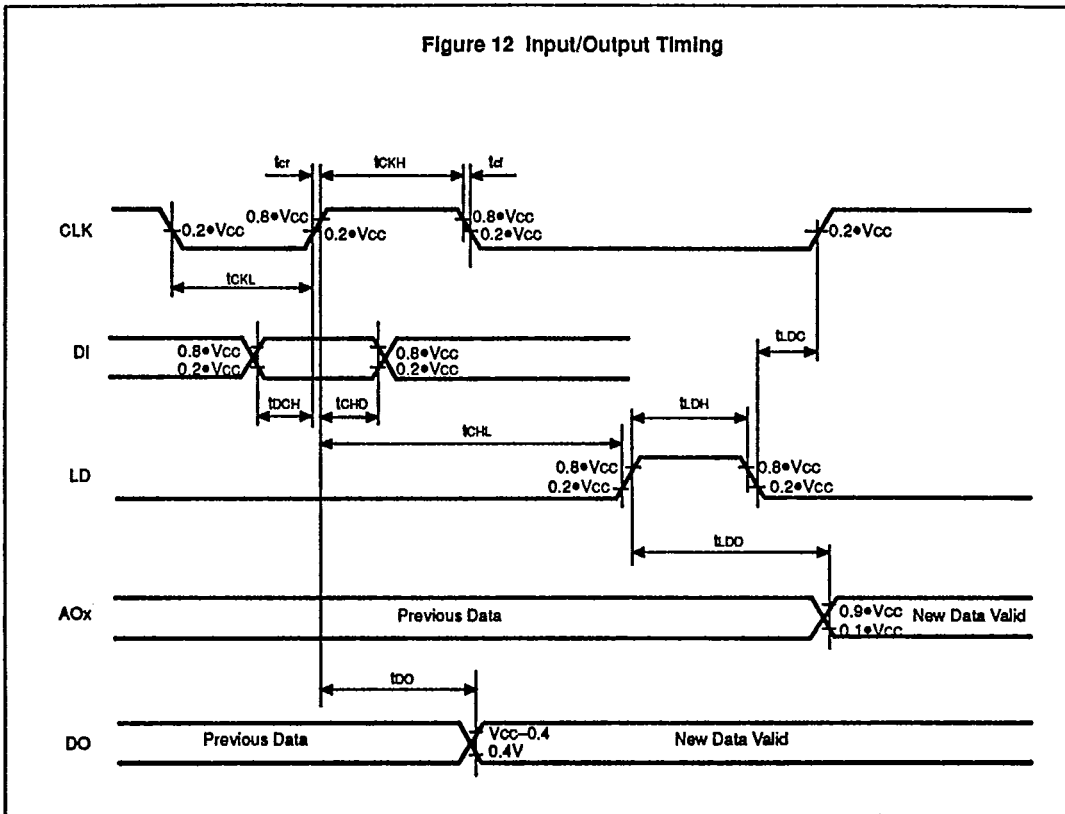
| Parameter | Symbol | Value | | Unit | Condition |
|----------------------------------|-------------------|-------|-----|------|---|
| | | Min | Max | | |
| Clock Low Time | t _{CKL} | 200 | | ns | |
| Clock High Time | t _{CKH} | 200 | | ns | |
| Clock Rise Time | t _{Cr} | | 200 | ns | |
| Clock Fall Time | t _{Cf} | | 200 | ns | |
| Data Setup Time | t _{DCH} | 30 | | ns | |
| Data Hold Time | t _{CHD} | 60 | | ns | |
| Load Strobe High Time | t _{LDH} | 100 | | ns | |
| Load Strobe Setup Time | t _{CHL} | 200 | | ns | |
| Load Strobe Hold Time | t _{LDC} | 100 | | ns | |
| DAC Output Settling Time 1 (AO1) | t _{LDO1} | | 60 | μs | Unloaded |
| DAC Output Settling Time 2 (AO2) | t _{LDO2} | | 30 | μs | *R _{AL} = 10 kΩ, C _{AL} = 50 pF |
| Data Output Delay Time | t _{DO} | 70 | 350 | ns | **C _L = 20 pF (Min.), 100 pF (Max.) |

Figure 11 AC Test Conditions



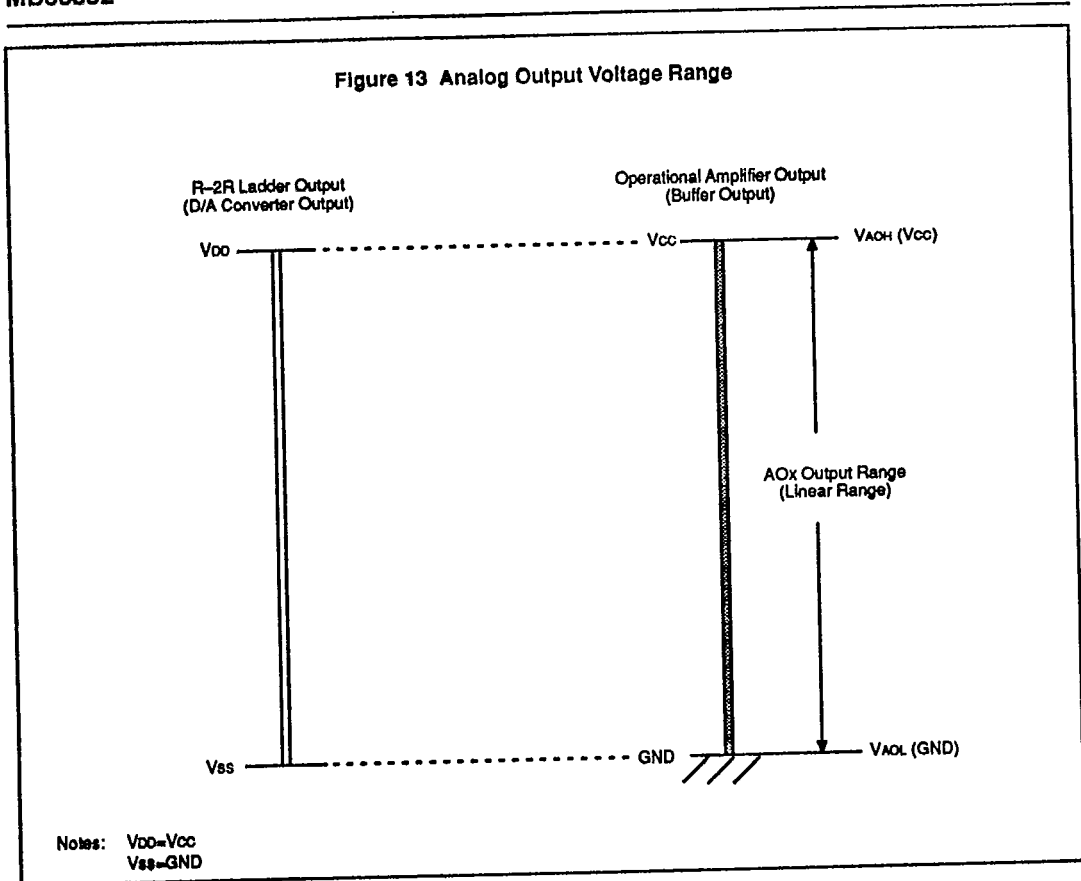
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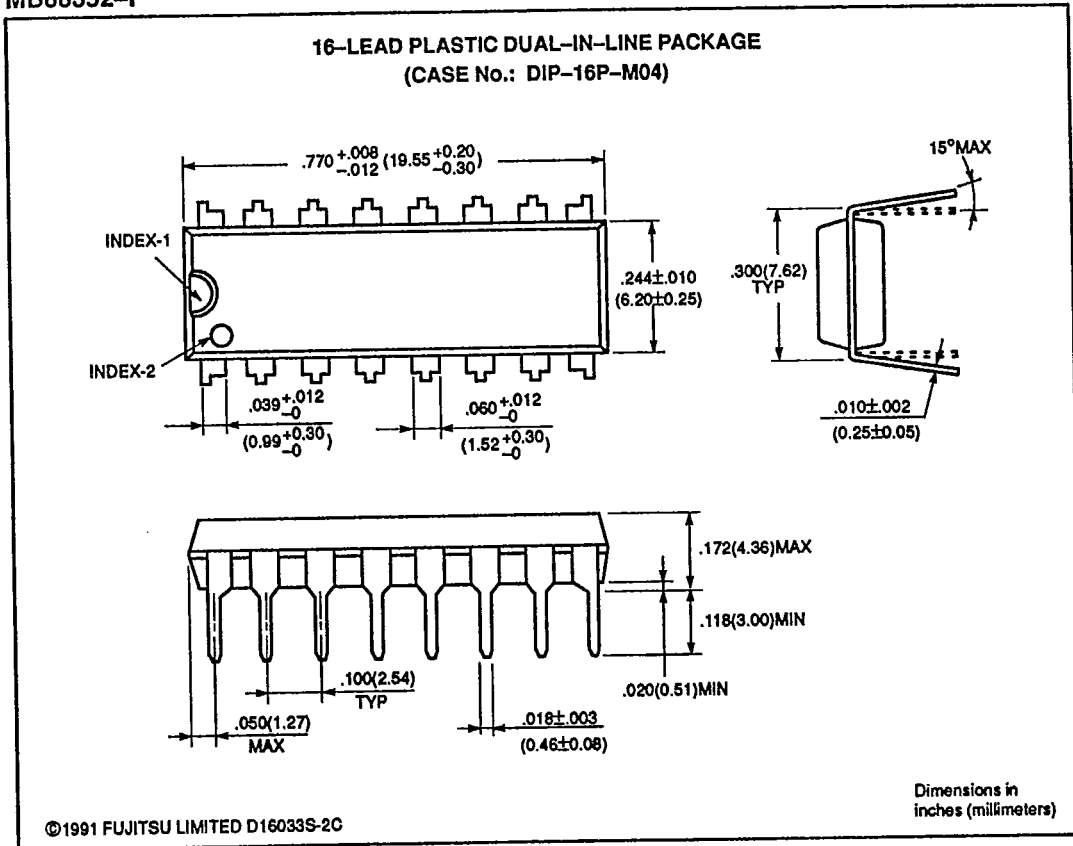


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PACKAGE DIMENSIONS

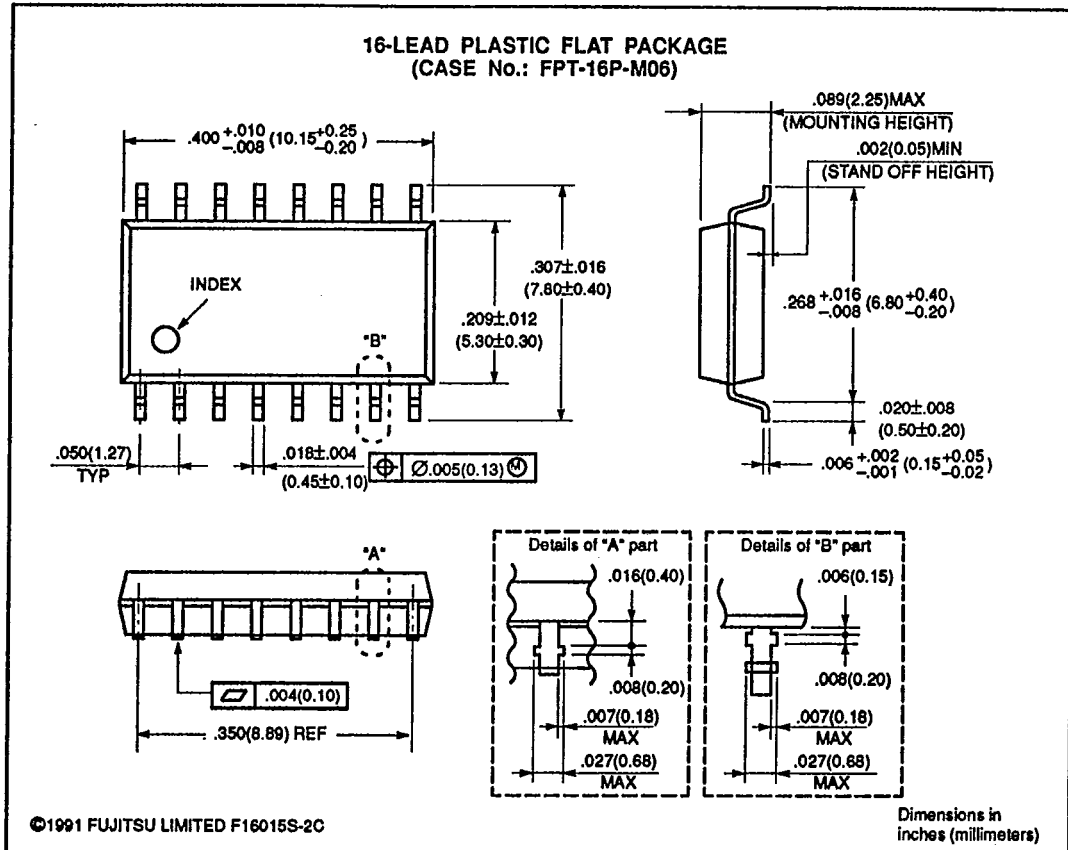
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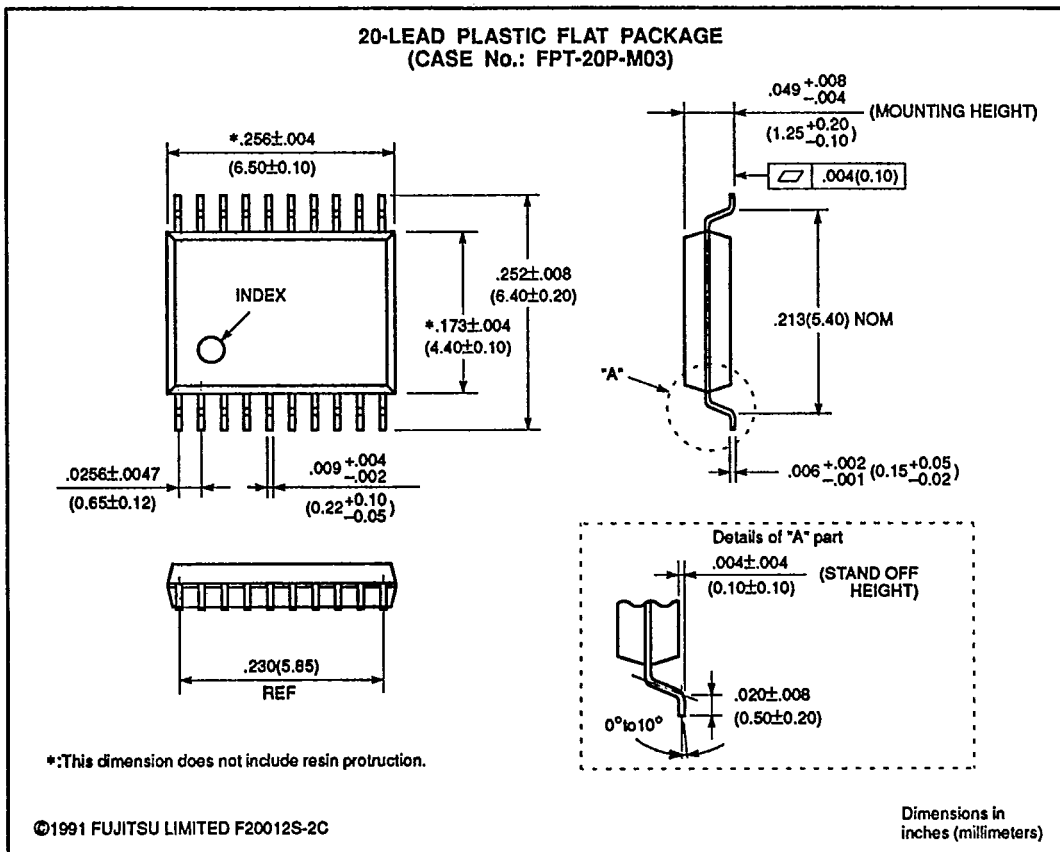
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