



Actions Semiconductor Co.,Ltd

# **ATJ2073 (LQFP128)**

## **DATA SHEET**

Ver. 1.10



## Revision History

1. Initial revision on Sep. 10, 2003.



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## 1. Short Descriptions

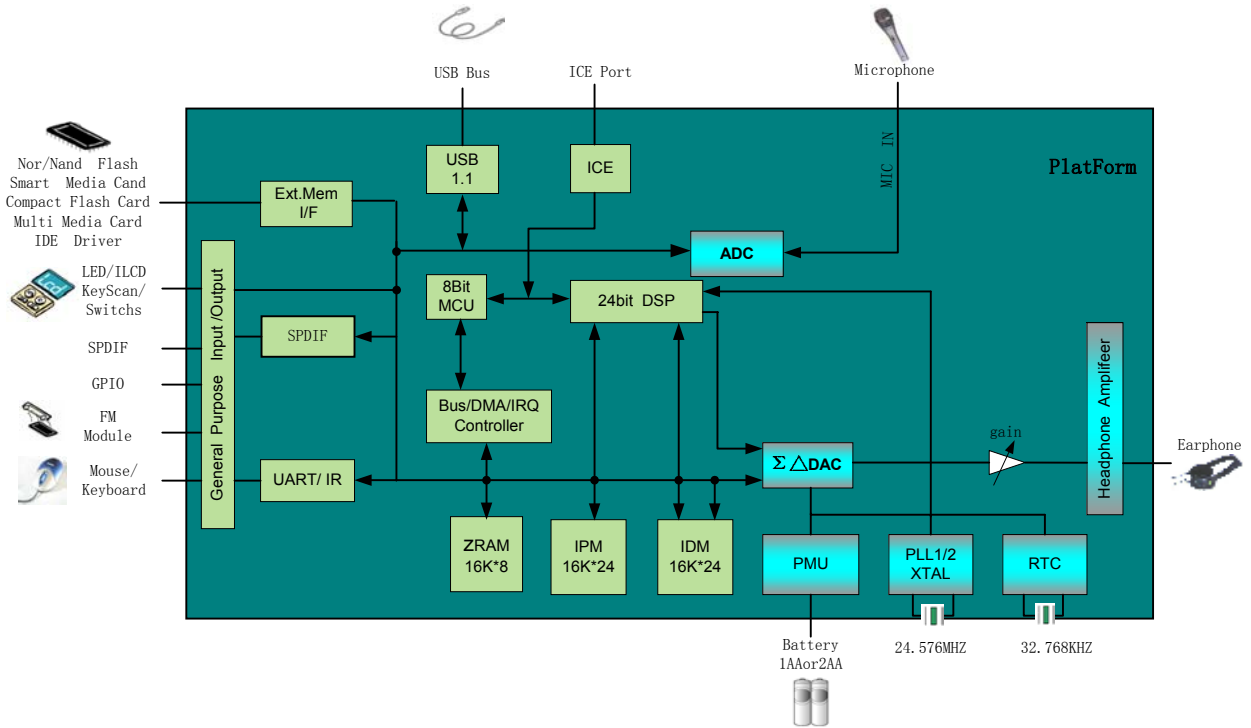
The ATJ2073 is a single-chip highly-integrated digital music system solution for devices such as dedicated audio players, PDAs, and cell phones. It includes an audio decoder with a high performance DSP with embedded RAM, ADPCM/AG record capabilities and USB interface for downloading music and uploading voice recordings. ATJ2073 also provides an interface to S/PDIF audio data input, flash memory, LED/LCD, button and switch inputs, headphone, and microphone, and FM radio control. The ATJ2073's programmable architecture supports the MP3 and other digital audio standards. For devices like USB Flash Disk, the ATJ2073 can act as a USB mass storage slave device to personal computer system. The ATJ2073 has low power consumption to allow long battery life and an efficient flexible on-chip DC-DC converter that allows many different battery configurations, including 1xAA, 1xAAA, 2xAA,2xAAA.

## 2. Features

- 24-bit DSP Core with on-chip ICE support
- On-chip DSP 16Kx24 PM and (16K-256)x24 DM, can be switched to be MCU memory space
- Integrated 8bit MCU with on-chip ICE support which the instructions are compatible with the Z80 CPU
- Internal 16k bytes SRAM accessed by MCU
- External up to 25-bit code address space with 7 chips select
- Support 14.318MHz/16.368MHz/17.734475MHz/24.576MHz OSC with on-chip PLL for DSP
- Supported up to 3\*4Gbyte Nand type Flash
- 2-channel DMA for MCU
- 1-channel CTC(Counter/Timer Controller) for MCU
- On-chip interrupt controller for MCU
- Built-in power management unit(PMU), supporting 1 or 2 batteries operation
- Support RTC with 32.768kHz or 76.8kHz OSC
- Built-in USB1.1 interface
- Support SPDIF IN/UART/IR interface
- Support on-chip Stereo 18 bit Sigma-Delta DAC
- Support external 6800 or 8086 series interface LCM
- Support 4x13 matrix Keyboard Circuit Auto Scan
- Support 20 General Purpose Input/Output
- Support external Epson Series LCM Frame Buffer up to 320x240 dots
- Support on-chip 1/3 biased 1/4 duty LCD driver(4x13dots, multiplexed )
- Support external CMOS image sensor interface
- On-chip 16-bit ADC for Microphone input support , sample rate at 8K/11K/12K/16K/22K/24KHz
- On-chip 2 channel headphone power amplifiers
- 128-pin 14x14x1.4mm LQFP package



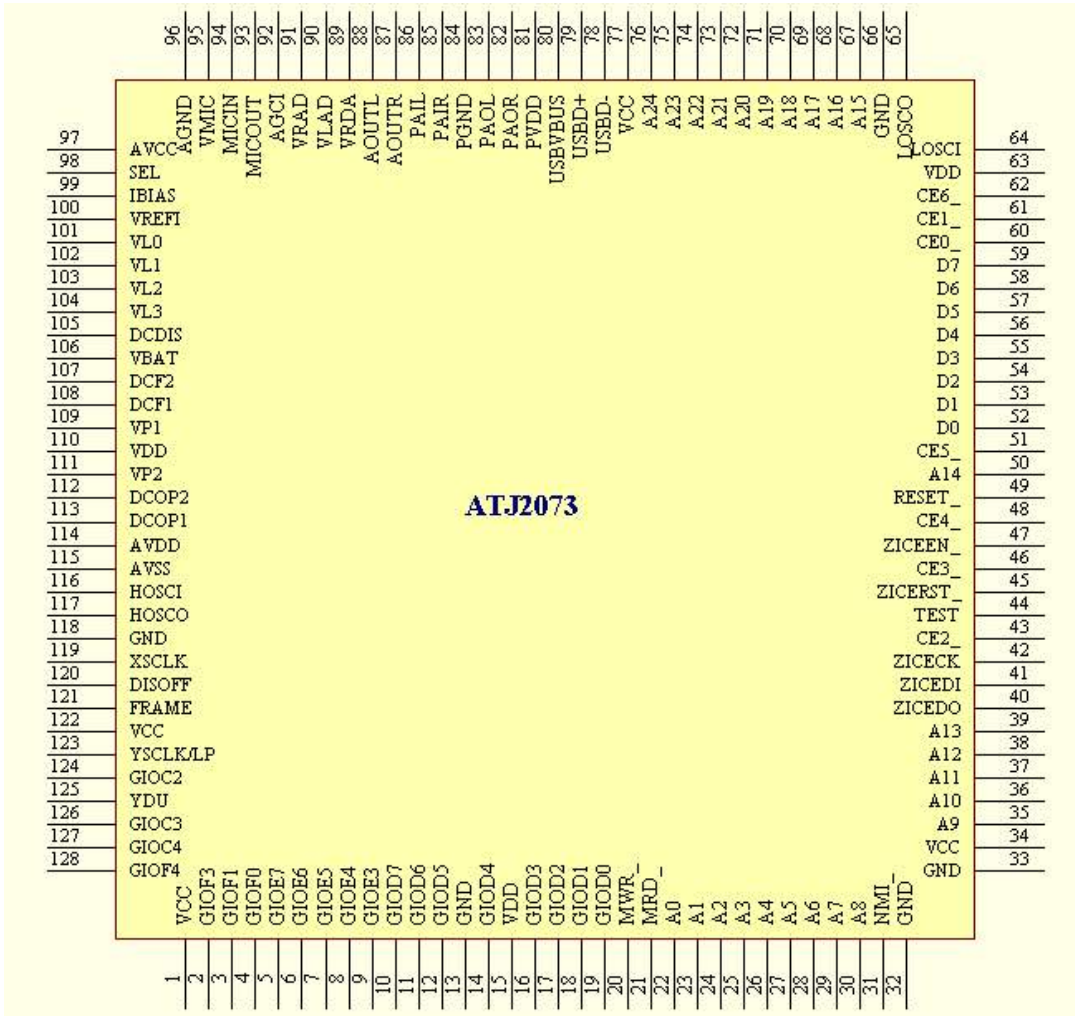
### 3. Architecture Overview





### 4. Pin Descriptions

#### 4.1 Pinout





## 4.2 Pin sort by number

Pin No.	Pin Name	I/O Type	Reset Default	Short Description
1	VCC	PWR		Power supply for Pads circuits
2	GIOF3	BI	Z	Bit3 of general purpose I/O port F
2 <sup>(1)</sup>	KEYO3	O	Z	Bit3 of key scan circuit output
2 <sup>(3)</sup>	SEG15	O	Z	SEG15 of int. 4comX28seg LCD driver
3	GIOF1	BI	Z	Bit1 of general purpose I/O port F
3 <sup>(1)</sup>	KEYO1	O	Z	Bit1 of key scan circuit output
3 <sup>(3)</sup>	SEG13	O	Z	SEG13 of int. 4comX28seg LCD driver
4	GIOF0	BI	Z	Bit0 of general purpose I/O port F
4 <sup>(1)</sup>	KEYO0	O	Z	Bit0 of key scan circuit output
4 <sup>(3)</sup>	SEG12	O	Z	SEG12 of int. 4comX28seg LCD driver
5	GIOE7	BI	Z	Bit7 of general purpose I/O port E
5 <sup>(1)</sup>	KEYI11	I	Z	Bit11 of key scan circuit input
5 <sup>(3)</sup>	SEG11	O	Z	SEG11 of int. 4comX28seg LCD driver
6	GIOE6	BI	Z	Bit6 of general purpose I/O port E
6 <sup>(1)</sup>	KEYI10	I	Z	Bit10 of key scan circuit input
6 <sup>(3)</sup>	SEG10	O	Z	SEG10 of int. 4comX28seg LCD driver
7	GIOE5	BI	Z	Bit5 of general purpose I/O port E
7 <sup>(1)</sup>	KEYI9	I	Z	Bit9 of key scan circuit input
7 <sup>(3)</sup>	SEG9	O	Z	SEG9 of int. 4comX28seg LCD driver
8	GIOE4	BI	Z	Bit4 of general purpose I/O port E
8 <sup>(1)</sup>	KEYI8	I	Z	Bit8 of key scan circuit input
8 <sup>(3)</sup>	SEG8	O	Z	SEG8 of int. 4comX28seg LCD driver
9	GIOE3	BI	Z	Bit3 of general purpose I/O port E
9 <sup>(1)</sup>	KEYI7	I	Z	Bit7 of key scan circuit input
9 <sup>(3)</sup>	SEG7	O	Z	SEG7 of int. 4comX28seg LCD driver
10	GIOD7	BI	Z	Bit7 of general purpose I/O port D
10 <sup>(1)</sup>	TCPD7	O	Z	Bit7 of Epson Series LCM data bus
10 <sup>(2)</sup>	KEYI3	I	Z	Bit3 of key scan circuit input
10 <sup>(3)</sup>	SEG3	O	Z	SEG3 of int. 4comX28seg LCD driver
11	GIOD6	BI	Z	Bit6 of general purpose I/O port D
11 <sup>(1)</sup>	TCPD6	O	Z	Bit6 of Epson Series LCM data bus



11 <sup>(2)</sup>	KEYI2	I	Z	Bit2 of key scan circuit input
11 <sup>(3)</sup>	SEG2	O	Z	SEG2 of int. 4comX28seg LCD driver
12	GIOD5	BI	Z	Bit5 of general purpose I/O port D
12 <sup>(1)</sup>	TCPD5	O	Z	Bit5 of Epson Series LCM data bus
12 <sup>(2)</sup>	KEYI1	I	Z	Bit1 of key scan circuit input
12 <sup>(3)</sup>	SEG1	O	Z	SEG1 of int. 4comX28seg LCD driver
13	GND	PWR	/	Digital signal ground
14	GIOD4	BI	Z	Bit4 of general purpose I/O port D
14 <sup>(1)</sup>	TCPD4	O	Z	Bit4 of Epson Series LCM data bus
14 <sup>(2)</sup>	KEYI0	I	Z	Bit0 of key scan circuit input
14 <sup>(3)</sup>	SEG0	O	Z	SEG0 of int. 4comX28seg LCD driver
15	VDD	PWR		Power supply for core
16	GIOD3	BI	Z	Bit3 of general purpose I/O port D
16 <sup>(1)</sup>	TCPD3	O	Z	Bit3 of Epson Series LCM data bus
16 <sup>(3)</sup>	COM3	O	Z	COM3 of int. 4comX28seg LCD driver
17	GIOD2	BI	Z	Bit2 of general purpose I/O port D
17 <sup>(1)</sup>	TCPD2	O	Z	Bit2 of Epson Series LCM data bus
17 <sup>(3)</sup>	COM2	O	Z	COM2 of int. 4comX28seg LCD driver
18	GIOD1	BI	Z	Bit1 of general purpose I/O port D
18 <sup>(1)</sup>	TCPD1	O	Z	Bit1 of Epson Series LCM data bus
18 <sup>(3)</sup>	COM1	O	Z	COM1 of int. 4comX28seg LCD driver
19	GIOD0	BI	Z	Bit0 of general purpose I/O port D
19 <sup>(1)</sup>	TCPD0	O	Z	Bit0 of Epson Series LCM data bus
19 <sup>(3)</sup>	COM0	O	Z	COM0 of int. 4comX28seg LCD driver
20	MWR-	BI	H	Ext. memory write active signal
20 <sup>(1)</sup>	WE-	O	H	Nand type flash write enable
21	MRD-	BI	H	Ext. memory read active signal
21 <sup>(1)</sup>	RE	O	H	Nand type flash read enable
22	A0	BI	L	Bit0 of ext. memory address bus
23	A1	BI	L	Bit1 of ext. memory address bus
24	A2	BI	L	Bit2 of ext. memory address bus
25	A3	BI	L	Bit3 of ext. memory address bus
26	A4	BI	L	Bit4 of ext. memory address bus
27	A5	BI	L	Bit5 of ext. memory address bus





28	A6	BI	L	Bit6 of ext. memory address bus
29	A7	BI	L	Bit7 of ext. memory address bus
30	A8	BI	L	Bit8 of ext. memory address bus
31	NMI-	SIU	H	Ext. non-maskable interrupt input
32	GND	PWR	/	Digital signal ground
33	GND	PWR	/	Digital signal ground
34	VCC	PWR		Power supply for Pads circuits
35	A9	BI	L	Bit9 of ext. memory address bus
36	A10	BI	L	Bit10 of ext. memory address bus
37	A11	BI	L	Bit11 of ext. memory address bus
38	A12	BI	L	Bit12 of ext. memory address bus
39	A13	BI	L	Bit13 of ext. memory address bus
40	ZICEDO	O	L	Debug pin, data output from DSU
41	ZICEDI	SIU	H	Debug pin, data input to DSU
42	ZICECK	SIU	H	Debug pin, clock into DSU
43	CE2-	O	H	Ext. memory chip select 2
44	TEST	SI	L	Test mode control, 0:normal mode 1:test mode
45	ZICERST-	SIU	H	Debug pin, to reset DSU
46	CE3-	O	H	Ext. memory chip select 3
47	ZICEEN-	SIU	H	Debug pin, to enable DSU
48	CE4-	O	H	Ext. memory chip select 4
49	RESET-	SI	H	System reset input
50	A14	O	L	Bit14 of ext. memory address bus
51	CE5-	O	H	Ext. memory chip select 5
52	D0	BI	Z	Bit0 of ext. memory data bus
53	D1	BI	Z	Bit1 of ext. memory data bus
54	D2	BI	Z	Bit2 of ext. memory data bus
55	D3	BI	Z	Bit3 of ext. memory data bus
56	D4	BI	Z	Bit4 of ext. memory data bus
57	D5	BI	Z	Bit5 of ext. memory data bus
58	D6	BI	Z	Bit6 of ext. memory data bus
59	D7	BI	Z	Bit7 of ext. memory data bus
60	CE0-	O	H	Ext. memory chip select 0
61	CE1-	O	H	Ext. memory chip select 1



62	CE6-	O	H	Ext. memory chip select 6
63	VDD	PWR		Power supply for core
64	LOSCI	AI	/	Low frequency crystal OSC input
65	LOSCO	AO	/	Low frequency crystal OSC output
66	GND	PWR	/	Digital signal ground
67	A15	O	L	Bit15 of ext. memory address bus
67 <sup>(1)</sup>	CLE	O	L	Command latch enable of Nand type flash
68	A16	O	L	Bit16 of ext. memory address bus
68 <sup>(1)</sup>	ALE	O	L	Address latch enable of Nand type flash
69	A17	O	L	Bit17 of ext. memory address bus
70	A18	O	L	Bit18 of ext. memory address bus
71	A19	O	L	Bit19 of ext. memory address bus/GPO
72	A20	O	L	Bit20 of ext. memory address bus/GPO
73	A21	O	L	Bit21 of ext. memory address bus/GPO
74	A22	O	L	Bit22 of ext. memory address bus/GPO
75	A23	O	L	Bit23 of ext. memory address bus/GPO
76	A24	O	L	Bit24 of ext. memory address bus/GPO
77	VCC	PWR		Power supply for Pads circuits
78	USBD-	A	/	USB negative connect
79	USBD+	A	/	USB positive connect
80	USBVBUS	I	L	USB cable power signal
81	PVDD	A	/	Bypass capacitor for power amplifier
82	PAOR	A	/	Output of right channel power amplifier
83	PAOL	A	/	Output of left channel power amplifier
84	PGND	PWR	/	Ground for power amplifier circuits
85	PAIR	A	/	Input of right channel power amplifier
86	PAIL	A	/	Input of left channel power amplifier
87	AOUTR	A	/	Int. sigma-delta DAC right channel analog output
88	AOUTL	A	/	Int. sigma-delta DAC left channel analog output
89	VRDA	A	/	Reference voltage for ADC
90	NC	/	/	
91	VRAD	A	/	Reference voltage for ADC
92	AGCI	A	/	Microphone ADC amplifier input



93	MICOUT	A	/	Microphone pre-amplifier output
94	MICIN	A	/	Microphone pre-amplifier input
95	VMIC	A	/	Power supply for microphone bias circuits
96	AGND	PWR	/	Analog ground for record, and ADC blocks
97	AVCC	PWR		Power supply for record, and ADC blocks
98	BATSEL	I		Battery select, 0:one battery 1:two batteries
99	IBIAS	I		Int. bias pin with a ext.R(1.5Mohm) to ground
100	VREFI	A		Reference voltage input (1.5v)
101	VL0	AI		Battery monitor reference voltage input ( for example 1.40v)
102	VL1	AI		Battery monitor reference voltage input (for example 1.30v)
103	VL2	AI		Battery monitor reference voltage input (for example 1.15v)
104	VL3	AI		Battery monitor reference voltage input (for example 1.05v)
105	DCDIS	I	L	Int DC-DC converter disable, 0:enable 1:disable
106	VBAT	I		Battery signal input (1.0-1.5v)
107	DCF2	AI	/	VCC DC-DC feedback pin
108	DCF1	AI	/	VDD DC-DC feedback pin
109	VP1	PWR		Power supply for int. regulator
110	VDD	PWR		Power supply for core
111	VP2	AI	/	Input for int. power switch
112	DCOP2	AO	/	VCC DC-DC pulse output
113	DCOP1	AO	/	VDD DC-DC pulse output
114	AVDD	PWR		Power supply for PLL analog circuits
115	AVSS	PWR	/	Ground for PLL analog circuits
116	HOSCI	AI	/	High frequency crystal OSC input
117	HOSCO	AO	/	High frequency crystal OSC output
118	GND	PWR	/	Digital signal ground
119	XSCLK	O	H	Epson Series LCM XSCLK output
120	DISPOFF	O	Z	Epson Series LCM display off control output
121	FRAME	O	Z	Epson Series LCM frame signal output
121 <sup>(1)</sup>	LCM_CE	O	Z	6800 Series LCM CE
121 <sup>(3)</sup>	V2	O	Z	Int. 4comX28seg LCD driver V2



122	VCC	PWR		Power supply for Pads circuits
123	YSCLK_LP	O	L	Epson Series LCM YSCLK/LP signal output
123 <sup>(1)</sup>	LCM_RW-	O	L	6800 Series LCM RW-
124	GIOC2	BI	Z	Bit2 of general purpose I/O port C
124 <sup>(1)</sup>	SIN2	I	Z	UART2 serial input
124 <sup>(2)</sup>	IRRX	I	Z	IR receive input
125	YDU	O	Z	Epson Series LCM YDU signal output
125 <sup>(1)</sup>	LCM_CS-	O	Z	6800 Series LCM CS-
125 <sup>(3)</sup>	V1	O	Z	Int. 4comX28seg LCD driver V1
126	GIOC3	BI	Z	Bit3 of general purpose I/O port C
126 <sup>(1)</sup>	SOUT2	O	Z	UART2 serial output
126 <sup>(2)</sup>	IRTX	O	Z	IR transmit output
127	GIOC4	BI	Z	Bit4 of general purpose I/O port C
127 <sup>(1)</sup>	SPDIFRX	BI	Z	SPDIF receive input
128	GIOF4	BI	Z	Bit4 of general purpose I/O port F
128 <sup>(1)</sup>	KEYO4	O	Z	Bit4 of key scan circuit output
128 <sup>(3)</sup>	SEG16	O	Z	SEG16 of int. 4comX28seg LCD driver



## 4.3 Pin sort by Function

Type	Pin No.	Pin Name	I/O Type	Reset Default	Short Description
Power	1	VCC	PWR		Power supply for Pads circuits
	34	VCC	PWR		Power supply for Pads circuits
	77	VCC	PWR		Power supply for Pads circuits
	122	VCC	PWR		Power supply for Pads circuits
	97	AVCC	PWR		Power supply for record, and ADC blocks
	15	VDD	PWR		Power supply for core
	63	VDD	PWR		Power supply for core
	110	VDD	PWR		Power supply for core
	114	AVDD	PWR		Power supply for PLL analog circuits
	13	GND	PWR	/	Digital signal ground
	32	GND	PWR	/	Digital signal ground
	33	GND	PWR	/	Digital signal ground
	66	GND	PWR	/	Digital signal ground
	118	GND	PWR	/	Digital signal ground
	84	PGND	PWR	/	Ground for power amplifier circuits
	96	AGND	PWR	/	Analog ground for record, t and ADC blocks
	115	AVSS	PWR	/	Ground for PLL analog circuits
109	VP1	PWR		Power supply for int. regulator	
DC-DC	98	BATSEL	I		Battery select, 0:one battery 1:two batteries
	99	IBIAS	I		Int. bias pin with a ext.R(1.5Mohm) to ground
	100	VREFI	A		Reference voltage input (1.5v)
	101	VL0	AI		Battery monitor reference voltage input (for example 1.40v)
	102	VL1	AI		Battery monitor reference voltage input (for example 1.30v)
	103	VL2	AI		Battery monitor reference voltage input (for example 1.15v)
	104	VL3	AI		Battery monitor reference voltage input (for example 1.05v)



	105	DCDIS	I	L	Int DC-DC converter disable, 0:enable 1:disable
	106	VBAT	I		Battery signal input (1.0-1.5v)
	107	DCF2	AI	/	VCC DC-DC feedback pin
	108	DCF1	AI	/	VDD DC-DC feedback pin
	111	VP2	AI	/	Input for int. power switch
	112	DCOP2	AO	/	VCC DC-DC pulse output
	113	DCOP1	AO	/	VDD DC-DC pulse output
ICE Interface	45	ZICERST-	SIU	H	Debug pin, to reset DSU
	47	ZICEEN-	SIU	H	Debug pin, to enable DSU
	41	ZICEDI	SIU	H	Debug pin, data input to DSU
	42	ZICECK	SIU	H	Debug pin, clock into DSU
	40	ZICEDO	O	L	Debug pin, data output from DSU
INT	31	NMI-	SIU	H	Ext. non-maskable interrupt input
TEST	44	TEST	SI	L	Test mode control, 0:normal mode 1:test mode
Reset-	49	RESET-	SI	H	System reset input
Chip Select Interface	60	CE0-	O	H	Ext. memory chip select 0
	61	CE1-	O	H	Ext. memory chip select 1
	43	CE2-	O	H	Ext. memory chip select 2
	46	CE3-	O	H	Ext. memory chip select 3
	48	CE4-	O	H	Ext. memory chip select 4
	51	CE5-	O	H	Ext. memory chip select 5
	62	CE6-	O	H	Ext. memory chip select 6
KeyBoard Interface	4	GIOF0	BI	Z	Bit0 of general purpose I/O port F
		KEYO0	O	Z	Bit0 of key scan circuit output
		SEG12	O	Z	SEG12 of LCD4*28
	3	GIOF1	BI	Z	Bit1 of general purpose I/O port F
		KEYO1	O	Z	Bit1 of key scan circuit output
		SEG13	O	Z	SEG13 of LCD4*28
	2	GIOF3	BI	Z	Bit3 of general purpose I/O port F
		KEYO3	O	Z	Bit3 of key scan circuit output
		SEG14	O	Z	SEG14 of LCD4*28
	128	GIOF4	BI	Z	Bit4 of general purpose I/O port F
KEYO4		O	Z	Bit4 of key scan circuit output	
SEG15		O	Z	SEG15 of LCD4*28	



	9	GIOE3	BI	Z	Bit3 of general purpose I/O port E
		KEYI7	I	Z	Bit7 of key scan circuit input
		SEG7	O	Z	SEG7 of LCD4*28
	8	GIOE4	BI	Z	Bit4 of general purpose I/O port E
		KEYI8	I	Z	Bit8 of key scan circuit input
		SEG8	O	Z	SEG8 of LCD4*28
	7	GIOE5	BI	Z	Bit5 of general purpose I/O port E
		KEYI9	I	Z	Bit9 of key scan circuit input
		SEG9	O	Z	SEG9 of LCD4*28
	6	GIOE6	BI	Z	Bit6 of general purpose I/O port E
		KEYI10	I	Z	Bit10 of key scan circuit input
		SEG10	O	Z	SEG10 of LCD4*28
5	GIOE7	BI	Z	Bit7 of general purpose I/O port E	
	KEYI11	I	Z	Bit11 of key scan circuit input	
	SEG11	O	Z	SEG11 of LCD4*28	
Display Epson Series LCM Interface	19	GIOD0	BI	Z	Bit0 of general purpose I/O port D
		TCPD0	O	Z	Bit0 of Epson Series LCM data bus
		COM0	O	Z	COM0 of LCD4*28
	18	GIOD1	BI	Z	Bit1 of general purpose I/O port D
		TCPD1	O	Z	Bit1 of Epson Series LCM data bus
		COM1	O	Z	COM1 of LCD4*28
	17	GIOD2	BI	Z	Bit2 of general purpose I/O port D
		TCPD2	O	Z	Bit2 of Epson Series LCM data bus
		COM2	O	Z	COM2 of LCD4*28
	16	GIOD3	BI	Z	Bit3 of general purpose I/O port D
		TCPD3	O	Z	Bit3 of Epson Series LCM data bus
		COM3	O	Z	COM3 of LCD4*28
	14	GIOD4	BI	Z	Bit4 of general purpose I/O port D
		TCPD4	O	Z	Bit4 of Epson Series LCM data bus
		KEYI0	I	Z	Bit0 of key scan circuit input
		SEG0	O	Z	SEG0 of LCD4*28
12	GIOD5	BI	Z	Bit5 of general purpose I/O port D	
	TCPD5	O	Z	Bit5 of Epson Series LCM data bus	
	KEYI1	I	Z	Bit1 of key scan circuit input	
	SEG1	O	Z	SEG1 of LCD4*28	



	11	GIOD6	BI	Z	Bit6 of general purpose I/O port D
		TCPD6	O	Z	Bit6 of Epson Series LCM data bus
		KEYI2	I	Z	Bit2 of key scan circuit input
		SEG2	O	Z	SEG2 of LCD4*28
	10	GIOD7	BI	Z	Bit7 of general purpose I/O port D
		TCPD7	O	Z	Bit7 of Epson Series LCM data bus
		KEYI3	I	Z	Bit3 of key scan circuit input
		SEG3	O	Z	SEG3 of LCD4*28
	119	XSCLK	O	H	Epson Series LCM XSCLK output
	120	DISPOFF	O	Z	Epson Series LCM display off control output
	121	FRAME	O	Z	Epson Series LCM frame signal output
		LCM_CE	O	Z	6800 Series LCM CE
	123	YSCLK_LP	O	L	Epson Series LCM YSCLK/LP signal output
		LCM_RW-	O	L	6800 Series LCM RW-
125	YDU	O	Z	Epson Series LCM YDU signal output	
	LCM_CS-	O	Z	6800 Series LCM CS-	
6800 Series LCM Interface	121	FRAME	O	Z	Epson Series LCM frame signal output
		LCM_CE	O	Z	6800 Series LCM CE
	123	YSCLK_LP	O	L	Epson Series LCM YSCLK/LP signal output
		LCM_RW-	O	L	6800 Series LCM RW-
	125	YDU	O	Z	Epson Series LCM YDU signal output
		LCM_CS-	O	Z	6800 Series LCM CS-
	52	D0	BI	Z	Bit0 of ext. memory data bus
	53	D1	BI	Z	Bit1 of ext. memory data bus
	54	D2	BI	Z	Bit2 of ext. memory data bus
	55	D3	BI	Z	Bit3 of ext. memory data bus
	56	D4	BI	Z	Bit4 of ext. memory data bus
	57	D5	BI	Z	Bit5 of ext. memory data bus
	58	D6	BI	Z	Bit6 of ext. memory data bus
	59	D7	BI	Z	Bit7 of ext. memory data bus
19	GIOD0	BI	Z	Bit0 of general purpose I/O port D	





Display LCD4*28 Interface		TCPD0	O	Z	Bit0 of Epson Series LCM data bus
		COM0	O	Z	COM0 of LCD4*28
	18	GIOD1	BI	Z	Bit1 of general purpose I/O port D
		TCPD1	O	Z	Bit1 of Epson Series LCM data bus
		COM1	O	Z	COM1 of LCD4*28
	17	GIOD2	BI	Z	Bit2 of general purpose I/O port D
		TCPD2	O	Z	Bit2 of Epson Series LCM data bus
		COM2	O	Z	COM2 of LCD4*28
	16	GIOD3	BI	Z	Bit3 of general purpose I/O port D
		TCPD3	O	Z	Bit3 of Epson Series LCM data bus
		COM3	O	Z	COM3 of LCD4*28
	14	GIOD4	BI	Z	Bit4 of general purpose I/O port D
		TCPD4	O	Z	Bit4 of Epson Series LCM data bus
		KEYI0	I	Z	Bit0 of key scan circuit input
		SEG0	O	Z	SEG0 of LCD4*28
	12	GIOD5	BI	Z	Bit5 of general purpose I/O port D
		TCPD5	O	Z	Bit5 of Epson Series LCM data bus
		KEYI1	I	Z	Bit1 of key scan circuit input
		SEG1	O	Z	SEG1 of LCD4*28
	11	GIOD6	BI	Z	Bit6 of general purpose I/O port D
		TCPD6	O	Z	Bit6 of Epson Series LCM data bus
		KEYI2	I	Z	Bit2 of key scan circuit input
		SEG2	O	Z	SEG2 of LCD4*28
	10	GIOD7	BI	Z	Bit7 of general purpose I/O port D
		TCPD7	O	Z	Bit7 of Epson Series LCM data bus
		KEYI3	I	Z	Bit3 of key scan circuit input
		SEG3	O	Z	SEG3 of LCD4*28
	9	GIOE3	BI	Z	Bit3 of general purpose I/O port E
KEYI7		I	Z	Bit7 of key scan circuit input	
SEG7		O	Z	SEG7 of LCD4*28	
8	GIOE4	BI	Z	Bit4 of general purpose I/O port E	
	KEYI8	I	Z	Bit8 of key scan circuit input	
	SEG8	O	Z	SEG8 of LCD4*28	
7	GIOE5	BI	Z	Bit5 of general purpose I/O port E	
	KEYI9	I	Z	Bit9 of key scan circuit input	



		SEG9	O	Z	SEG9 of LCD4*28
	6	GIOE6	BI	Z	Bit6 of general purpose I/O port E
		KEYI10	I	Z	Bit10 of key scan circuit input
		SEG10	O	Z	SEG10 of LCD4*28
	5	GIOE7	BI	Z	Bit7 of general purpose I/O port E
		KEYI11	I	Z	Bit11 of key scan circuit input
		SEG11	O	Z	SEG11 of LCD4*28
	4	GIOF0	BI	Z	Bit0 of general purpose I/O port F
		KEYO0	O	Z	Bit0 of key scan circuit output
		SEG12	O	Z	SEG12 of LCD4*28
	3	GIOF1	BI	Z	Bit1 of general purpose I/O port F
		KEYO1	O	Z	Bit1 of key scan circuit output
		SEG13	O	Z	SEG13 of LCD4*28
	2	GIOF3	BI	Z	Bit3 of general purpose I/O port F
		KEYO3	O	Z	Bit3 of key scan circuit output
SEG14		O	Z	SEG14 of LCD4*28	
128	GIOF4	BI	Z	Bit4 of general purpose I/O port F	
	KEYO4	O	Z	Bit4 of key scan circuit output	
	SEG15	O	Z	SEG15 of LCD4*28	
NAND TYPE FLASH Or SMC Interface	67	A15	O	L	Bit15 of ext. memory address bus
		CLE	O	L	Command latch enable of Nand type flash
	68	A16	O	L	Bit16 of ext. memory address bus
		ALE	O	L	Address latch enable of Nand type flash
	52	D0	BI	Z	Bit0 of ext. memory data bus
	53	D1	BI	Z	Bit1 of ext. memory data bus
	54	D2	BI	Z	Bit2 of ext. memory data bus
	55	D3	BI	Z	Bit3 of ext. memory data bus
	56	D4	BI	Z	Bit4 of ext. memory data bus
	57	D5	BI	Z	Bit5 of ext. memory data bus
	58	D6	BI	Z	Bit6 of ext. memory data bus
	59	D7	BI	Z	Bit7 of ext. memory data bus
	20	MWR-	BI	H	Ext. memory write active signal
		WE-	O	H	Nand type flash write enable
	21	MRD-	BI	H	Ext. memory read active signal



		RE	O	H	Nand type flash read enable
NOR TYPE FLASH Interface	20	MWR-	BI	H	Ext. memory write active signal
		WE-	O	H	Nand type flash write enable
	21	MRD-	BI	H	Ext. memory read active signal
		RE	O	H	Nand type flash read enable
	22	A0	BI	L	Bit0 of ext. memory address bus
	23	A1	BI	L	Bit1 of ext. memory address bus
	24	A2	BI	L	Bit2 of ext. memory address bus
	25	A3	BI	L	Bit3 of ext. memory address bus
	26	A4	BI	L	Bit4 of ext. memory address bus
	27	A5	BI	L	Bit5 of ext. memory address bus
	28	A6	BI	L	Bit6 of ext. memory address bus
	29	A7	BI	L	Bit7 of ext. memory address bus
	30	A8	BI	L	Bit8 of ext. memory address bus
	35	A9	BI	L	Bit9 of ext. memory address bus
	36	A10	BI	L	Bit10 of ext. memory address bus
	37	A11	BI	L	Bit11 of ext. memory address bus
	38	A12	BI	L	Bit12 of ext. memory address bus
	39	A13	BI	L	Bit13 of ext. memory address bus
	50	A14	O	L	Bit14 of ext. memory address bus
	67	A15	O	L	Bit15 of ext. memory address bus
		CLE	O	L	Command latch enable of Nand type flash
	68	A16	O	L	Bit16 of ext. memory address bus
		ALE	O	L	Address latch enable of Nand type flash
	69	A17	O	L	Bit17 of ext. memory address bus
	70	A18	O	L	Bit18 of ext. memory address bus
	71	A19	O	L	Bit19 of ext. memory address bus /GPO
72	A20	O	L	Bit20 of ext. memory address bus /GPO	
73	A21	O	L	Bit21 of ext. memory address bus /GPO	
74	A22	O	L	Bit22 of ext. memory address bus /GPO	
75	A23	O	L	Bit23 of ext. memory address bus /GPO	



	76	A24	O	L	Bit24 of ext. memory address bus /GPO
	52	D0	BI	Z	Bit0 of ext. memory data bus
	53	D1	BI	Z	Bit1 of ext. memory data bus
	54	D2	BI	Z	Bit2 of ext. memory data bus
	55	D3	BI	Z	Bit3 of ext. memory data bus
	56	D4	BI	Z	Bit4 of ext. memory data bus
	57	D5	BI	Z	Bit5 of ext. memory data bus
	58	D6	BI	Z	Bit6 of ext. memory data bus
	59	D7	BI	Z	Bit7 of ext. memory data bus
Crystal Interface	64	LOSCI	AI	/	Low frequency crystal OSC input
	65	LOSCO	AO	/	Low frequency crystal OSC output
	116	HOSCI	AI	/	High frequency crystal OSC input
	117	HOSCO	AO	/	High frequency crystal OSC output
USB Interface	78	USBD-	A	/	USB negative connect
	79	USBD+	A	/	USB positive connect
	80	USBVBUS	I	L	USB cable power signal
Power Amplifier Interface	81	PVDD	A	/	Bypass capacitor for power amplifier
	82	PAOR	A	/	Output of right channel power amplifier
	83	PAOL	A	/	Output of left channel power amplifier
	85	PAIR	A	/	Input of right channel power amplifier
	86	PAIL	A	/	Input of left channel power amplifier
DAC Output Interface	87	AOUTR	A	/	Int. sigma-delta DAC right channel analog output
	88	AOUTL	A	/	Int. sigma-delta DAC left channel analog output
ADC Interface	89	VRDA	A	/	Reference voltage for ADC
	90	NC	/	/	
	91	VRAD	A	/	Reference voltage for ADC
	92	AGCI	A	/	Microphone ADC amplifier input
	93	MICOUT	A	/	Microphone pre-amplifier output
	94	MICIN	A	/	Microphone pre-amplifier input
	95	VMIC	A	/	Power supply for microphone bias circuits



UART Interface	124	GIOC2	BI	Z	Bit2 of general purpose I/O port C
		SIN2	I	Z	UART2 serial input
		IRRX	I	Z	IR receive input
	126	GIOC3	BI	Z	Bit3 of general purpose I/O port C
		SOUT2	O	Z	UART2 serial output
		IRTX	O	Z	IR transmit output
IR Interface	124	GIOC2	BI	Z	Bit2 of general purpose I/O port C
		SIN2	I	Z	UART2 serial input
		IRRX	I	Z	IR receive input
	126	GIOC3	BI	Z	Bit3 of general purpose I/O port C
		SOUT2	O	Z	UART2 serial output
		IRTX	O	Z	IR transmit output
SPDIF Interface	127	GIOC4	BI	Z	Bit4 of general purpose I/O port C
		SPDIFRX	BI	Z	SPDIF receive input



## 5. Functional Description

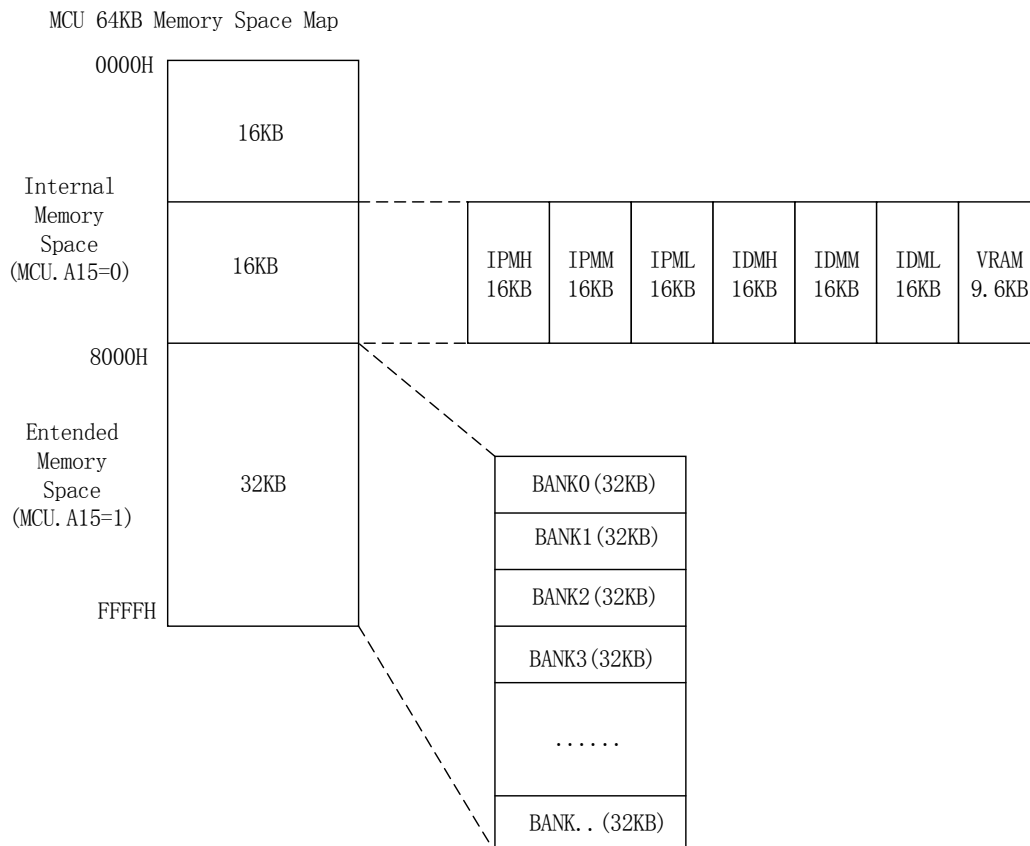
### 5.1 DSP Core

24-bit Harvard architecture DSP with on-chip ICE support is built in. it works with a memory word length of 24 bits. ATJ2073 has 16KB\*24bit Program Memory (PM) and (16KB-256)\*24bit Data Memory (DM). Memory-Mapped Register include DAC interface. Process capability is controlled by software Up to 48 MIPS.

### 5.2 MCU Core

Integrated 8-bit MCU with on-chip ICE support. Instruction set is compatible with Z80. Process capability is controlled by software Up to 24.576 MHz.

### 5.3 System Memory Mapping





Assuming MCU instruction uses A[15:0] to access memory space.

If A[15]=0 -> mapped to internal SRAM ,then

If A[14]=0, mapped to lower 16KB (ZRAM)

If A[14]=1, mapped to upper 16KB (IPMH/IPMM/IPML/IDMH/IDMM/IDML/VRAM) when they are mapped into MCU memory space. Additional three extended bits of SRAM Page Register (IO index=0x05) are used to decode which page to access.

Bit 2 1 0	Accessed Page
0 0 0	16K of IPM low byte
0 0 1	16K of IPM middle byte
0 1 0	16K of IPM high byte
0 1 1	reserved
1 0 0	16K of IDM low byte
1 0 1	16K of IDM middle byte
1 1 0	16K of IDM high byte
1 1 1	on-chip VRAM (Video RAM)

IPM/IDM can map to MCU memory space in 8K unit.

If A[15]=1 -> External address pin A25~A15 are IO mapped at 01h and 02h for EMA15-25. While EMA26-28 are used to decode CE0- ~ CE6-.

CE0- is used to access boot code from ROM/MASK/NOR-type Flash

CE1- to CE6- can be configured to access ROM, or RAM or NAND-type Flash

### 5.4 USB1.1 Interface

Compliant with USB SPEC 1.1. Certified by USB IF.

4 endpoints are provided. Support bulk, control, interrupt and isochronous transfer mode . Endpoint 1 and endpoint 2 employ two independent FIFOs for bulk or isochronous transfers. Endpoint 0 and endpoint 3 have 8 bytes maximum packet size. There are 4 interrupt requests for each endpoint respectively. Generally, this setting should be satisfying for most practical needs.

### 5.5 MPEG Decoder

With system software, ATJ2073 is competent for MPEG 1/2/2.5 Layer I/II/III decode.

Sample rates (SR) and bit rates (BR) supported is shown as the following table.

MPEG 2.5														
SR\BR	8	16	24	32	40	48	56	64	80	96	112	128	144	160
8	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
11.025	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
12	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MPEG 2														
SR\BR	8	16	24	32	40	48	56	64	80	96	112	128	144	160



16	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
22.05	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
24	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
<b>MPEG 1</b>														
SR\BR	32	40	48	56	64	80	96	112	128	160	192	224	256	320
32	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
44.1	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
48	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Table 1. Sample rates and Bit rates of Layer III supported

<b>MPEG 2</b>														
SR\BR	8	16	24	32	40	48	56	64	80	96	112	128	144	160
16	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
22.05	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
24	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
<b>MPEG 1</b>														
SR\BR	32	48	56	64	80	96	112	128	160	192	224	256	320	384
32	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
44.1	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
48	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Table 2. Sample rates and Bit rates of Layer II supported

<b>MPEG 2</b>														
SR\BR	32	48	56	64	80	96	112	128	144	160	176	192	224	256
16	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
22.05	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
24	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
<b>MPEG 1</b>														
SR\BR	32	64	96	128	160	192	224	256	288	320	352	384	416	448
32	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
44.1	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
48	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Table 3. Sample rates and Bit rates of Layer I supported

### 5.6 Microphone Interface

Microphone interface is composed of microphone pre-amplifier and 16-bit ADC.

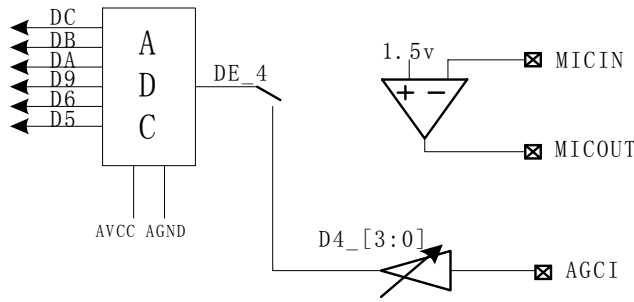
Microphone pre-amplifier has 35db gain at least for suitable recording volume so the noise of microphone power supply must be very low. It is composed of a regulator and an external first order RC LPF. AGC function is implemented by a variable gain amplifier and 4 register bits (MCU code control).

The ADC adopts switched-capacitor successive approximation method. Its input is from microphone pre-amplifier's output. Function enable, sampling frequency select, and some other control signals are all from





one register.



### 5.7 SPDIF Interface

The AES/EBU interface is a means for serially communicating digital audio data through one single transmission line. It provides two channels for audio data, a method for communicating control information, and has error detection capabilities. The control information is transmitted as one bit per sample and accumulates in a block structure. The data is bi-phase encoded, which enables the receiver to extract a clock from the data. Coding violations, defined as preambles, are used to identify sample and block boundaries.

2 8-level by 8-bit FIFO are used to buffer data for TX and RX. After received 192 frame- four bytes of channel status was appended into the RX FIFO. When TX FIFO is empty and SPDIF is enabled, 0 is send out for all frame.

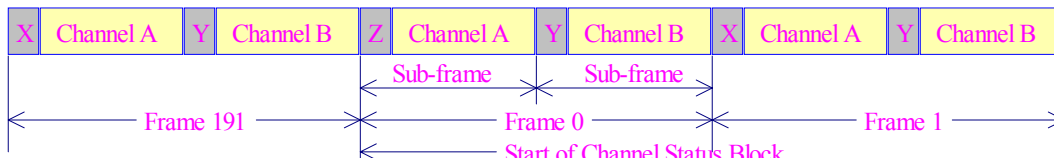


Figure 7.1. Frame/Block Format

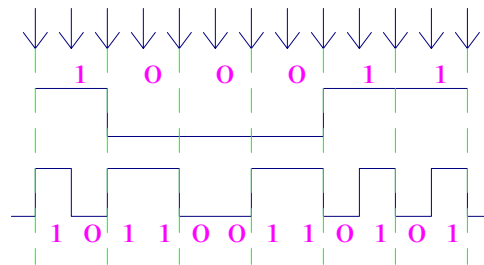


Figure 7.2. Biphase-Mark Encoding

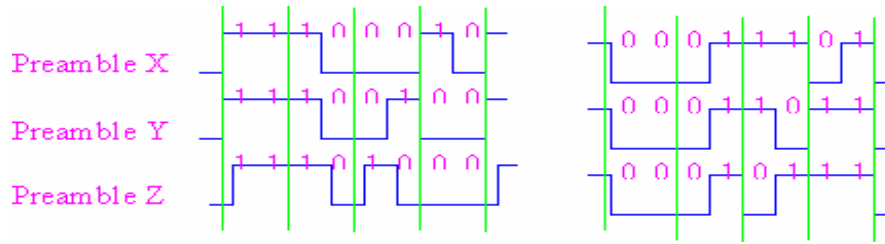


Figure 7.3. Preamble Forms

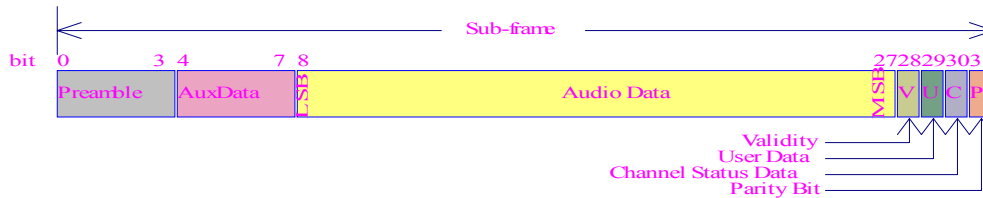


Figure 7.4. Sub-frame Format

### 5.8 Power Management Unit (PMU)

PMU consists of DC-DC converter and regulator and battery monitor.

ATJ2073 need two power trails if work rightly, VDD (Core Power) and VCC (I/O Power). The power level is decided by external voltage-divided resistance network . Due to describe clearly , we assume VDD=2.35V, VCC=3.15V.

There are two battery modes with ATJ2073, one-battery mode and two-battery mode, selected by BATSEL. In one-battery mode, if pin VBAT > 0.8V, some internal circuit (C1) begin to work first and it will rise up VDD. When VDD reaches 2.35V, that internal circuit (C1) stops and another circuit (C2) takes over the PFM for both VDD and VCC DC-DC converter.

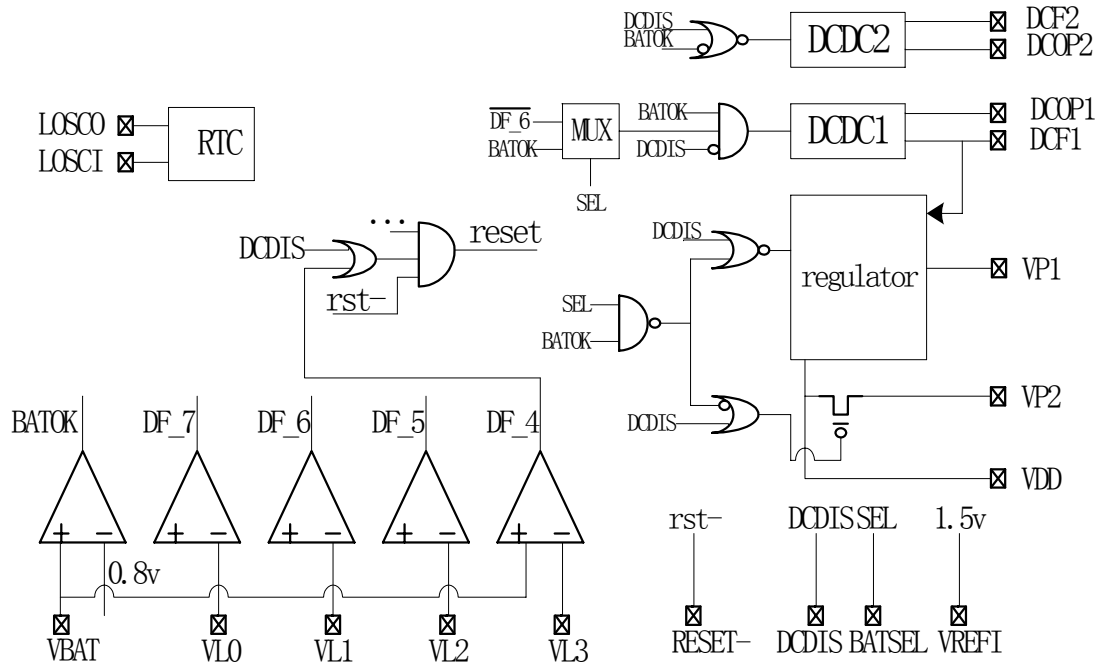
In two-battery mode, if pin VBAT > 1.3V, the internal regulator is enabled to supply VDD. If 0.8V < VBAT < 1.3V, C2 will stimulate VDD DC-DC converter to maintain VDD. The judgement between VBAT and 1.3V must have hysteresis for preventing ATJ2073 from unstable toggle between regulator mode and DC-DC mode. The VCC DC-DC converter always runs to maintain VCC.

Battery monitor compares the battery voltage at the VBAT pin with four reference voltage pins named VL0, VL1, VL2, VL3. The four reference voltages are decided by external resistance network. For normal dry battery (1.5V) , the value can be : 1.4V, 1.3V, 1.15V, and 1.05V.

If VBAT < VL3, ATJ2073 will go into STANDBY mode;

If VBAT < 0.8V, ATJ2073 will go into OFF mode, but the low frequency OSC and RTC timer are still active.

You can disable the clock of block when you do not use that block. Even more you can stop all the clock, but low frequency OSC, while you design appropriately.



## 6. Control Interfaces

### 6.1 How System Power Up

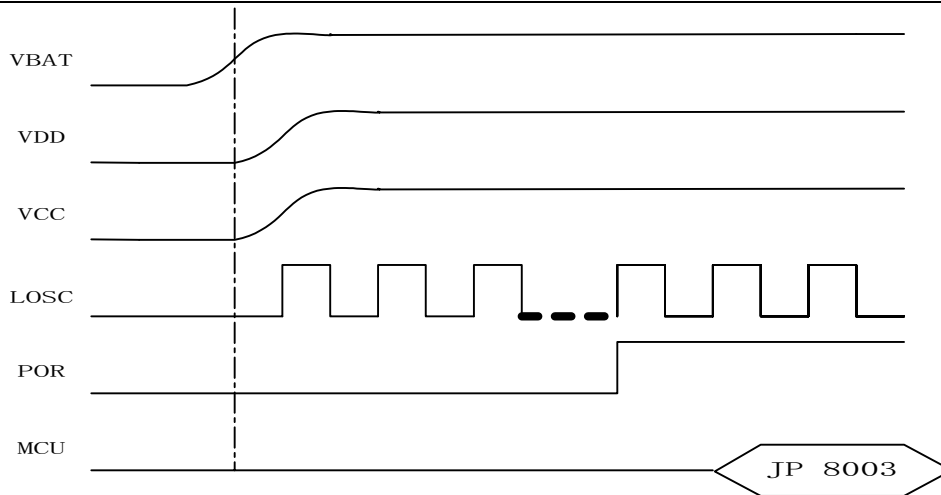
When pin VBAT get to about 0.8V level , DC-DC converter. will begin to rise up VDD and VCC. Low frequency oscillator will begin to work too. After a duration , POR(Power On Reset) will deassert . ATJ2073 finishes Power Up sequence . If pin RESET- is not assert, MCU will run from address=0x8000. Boot code at address=0x8000 will be as the following:

```

JP 8003h
LD A, 01h
OUT (04h), A
JP Start
... ..

```

Start:



## 6.2 Key Matrix Scan

When key scan circuit is enabled, ATJ2073 will scan the keyboard periodically. It drives pin KEYOUTn [n=0...7] low pulse in turn . When a key is pressed, pin KEYINn connecting the key will be found low level.

There are 12 internal 8-bit registers for key value latch per scan. But only another one register (Key Scan Data Register ) for MCU to access key value . Those 12 internal registers are mapped into this register, and an internal pointer is used to point to the current register to return scan data when read. Any IO write to this register will clear the internal register, and the pointer will increase by 1 and point to the next register after read is performed.



	KeyIn0		
	KeyIn1		
	KeyIn2		
	KeyIn3		
	KeyIn4		
	KeyIn5		
	KeyIn6		
	KeyIn7		
	KeyIn8		
	KeyIn9		
	KeyIn10		
	KeyIn11		
		1st Reg	2nd Reg
KeyOut0	b0b1 b2b3 b4b5 b6b7	b0b1 b2b3	
		2nd Reg	3rd Reg
KeyOut1	b4b5 b6b7 b0b1 b2b3	b4b5 b6b7	
		4th Reg	5th Reg
KeyOut2	b0b1 b2b3 b4b5 b6b7	b0b1 b2b3	
		5th Reg	6th Reg
KeyOut3	b4b5 b6b7 b0b1 b2b3	b4b5 b6b7	
		7th Reg	8th Reg
KeyOut4	b0b1 b2b3 b4b5 b6b7	b0b1 b2b3	
		8th Reg	9th Reg
KeyOut5	b4b5 b6b7 b0b1 b2b3	b4b5 b6b7	
		10th Reg	11th Reg
KeyOut6	b0b1 b2b3 b4b5 b6b7	b0b1 b2b3	
		11th Reg	12th Reg
KeyOut7	b4b5 b6b7 b0b1 b2b3	b4b5 b6b7	

Example:

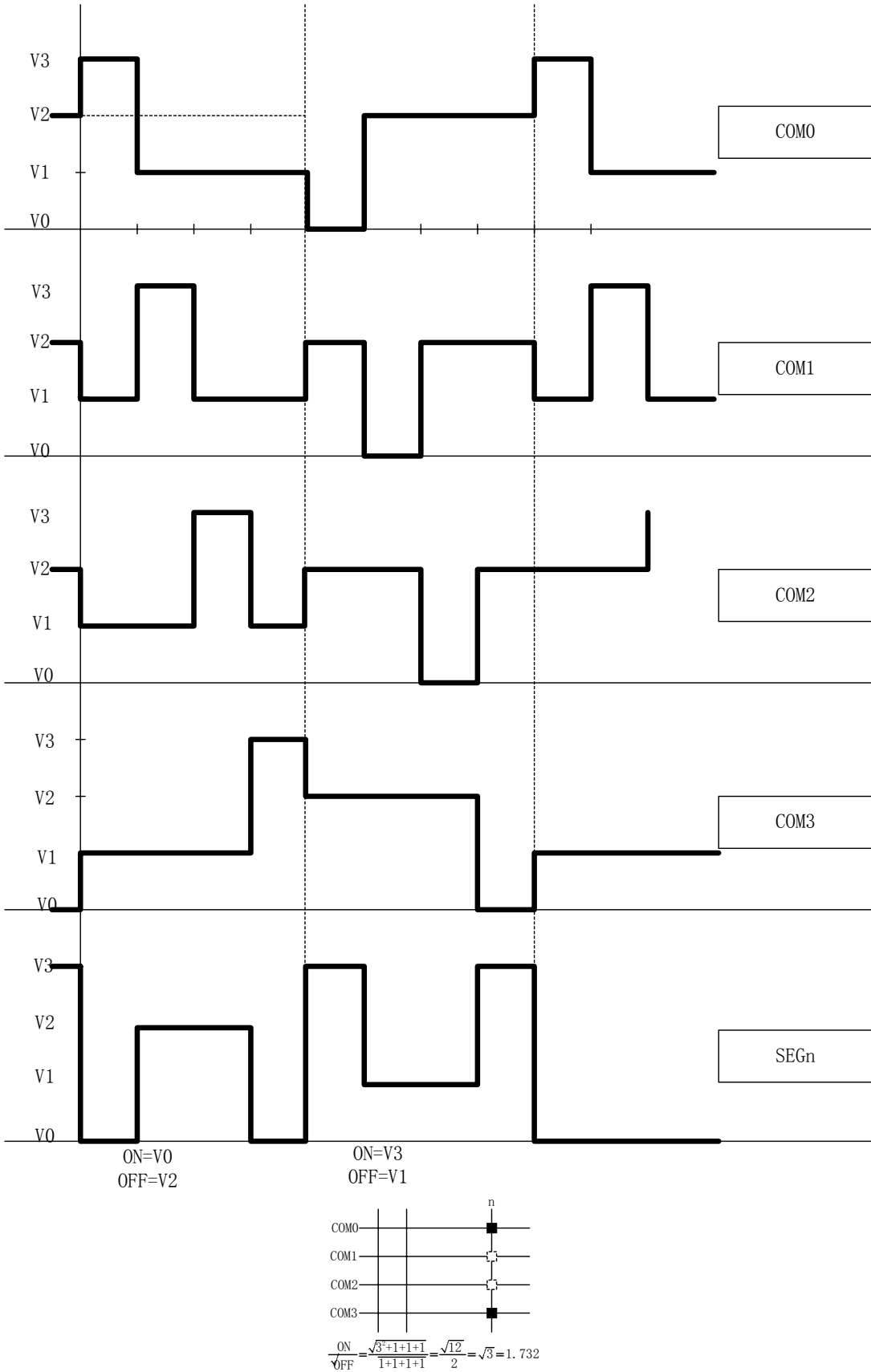
Reg\$C0 Readback is \$FF,\$AF,\$F7,\$FF,\$FF,\$FE,\$FF,\$FF,\$FF,\$FF,\$FF,\$FE,

indicate following 5 keys have pressed : [KeyOut ,KeyIn]

[1,0], [1,2], [1,7], [3,4], [7,4]

### 6.3 4\*13 LCD Driver

ATJ2073 builds in 1/3 biased 1/4 duty LCD driver. It outputs COM and SEG signals to LCD glass directly. Bias voltage pin V1 and V2 need connect by-pass capacitor to ground. V0=GND, V3=VCC.



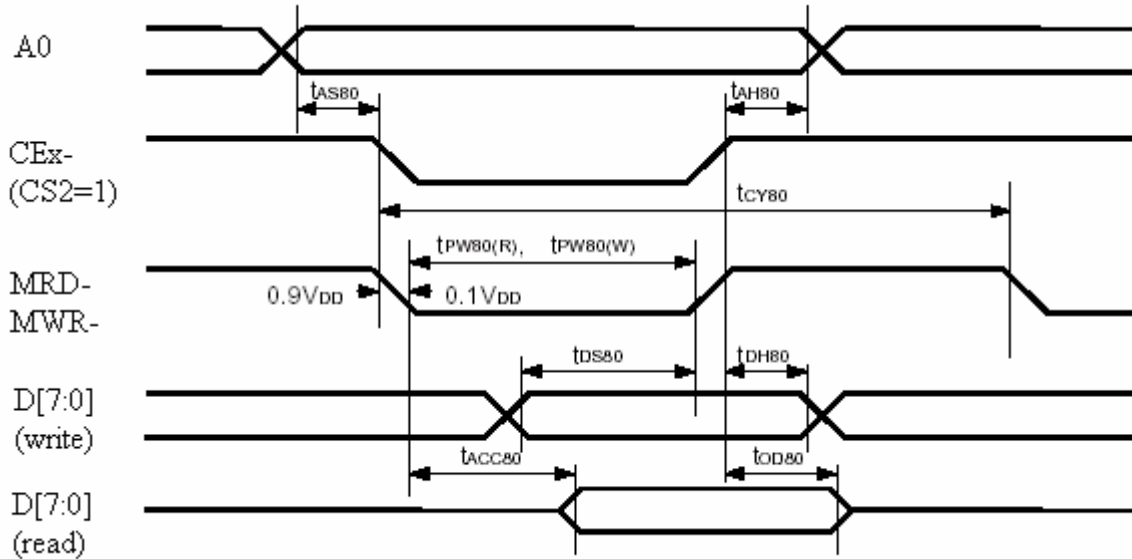
### 6.4 8080/6800 LCM Interface

ATJ2073 supports high-speed 8-bit parallel bi-directional LCM with 6800-series or 8080-series interface.



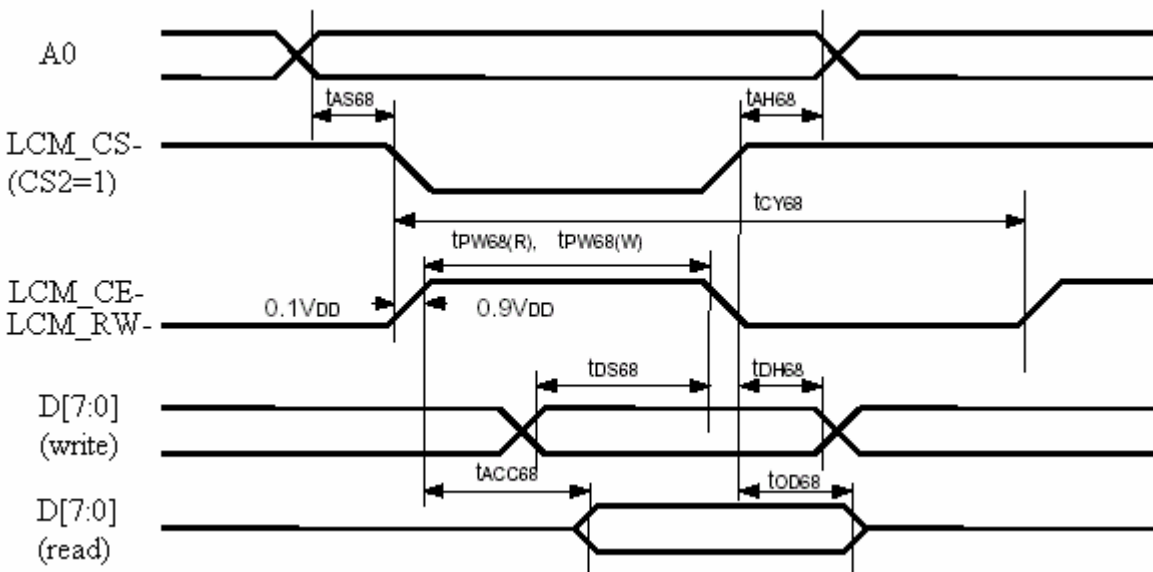
1. LCM with 8080-series interface:

Use A0 to select Data register or Command register in LCM.  
CEx- is used as chip select. Pin CS2 of LCM is pull high to VCC.  
MWR- is write enable signal, ATJ2073 latches D[7:0] at the rising edge.  
MRD- is read enable signal and LCM drives D[7:0] when MRD- is low.



2. LCM with 6800-series interface:

Use A0 to select Data register or Command register in LCM.  
LCM\_CS- is used as chip select. Pin CS2 of LCM is pull high to VCC.  
LCM\_RW- is read/write indication signal and high indicates read operation.  
LCM\_CE- is latch signal. It should latch D[7:0] at the falling edge.





## 7. Pin Configurations

ATJ2073 has many Multiple Function Pins (MFP), these pins are multiplexed by several functions.

Pin name will indicate the default function. Other functions can be enabled by system I/O register.

PIN		FUNCTION			
Number	Name	GPIO	SEGMENT LCD	KEY BOARD	TCP LCM
17	GIOD0	GIOD0	COM0		LCMD0
16	GIOD1	GIOD1	COM1		LCMD1
15	GIOD2	GIOD2	COM2		LCMD2
14	GIOD3	GIOD3	COM3		LCMD3
13	GIOD4	GIOD4	SEG0	KEYI0	LCMD4
12	GIOD5	GIOD5	SEG1	KEYI1	LCMD5
11	GIOD6	GIOD6	SEG2	KEYI2	LCMD6
10	GIOD7	GIOD7	SEG3	KEYI3	LCMD7
9	GIOE3	GIOE3	SEG7	KEYI7	
8	GIOE4	GIOE4	SEG8	KEYI8	
7	GIOE5	GIOE5	SEG9	KEYI9	
6	GIOE6	GIOE6	SEG10	KEYI10	
5	GIOE7	GIOE7	SEG11	KEYI11	
4	GIOF0	GIOF0	SEG12	KEYO0	
3	GIOF1	GIOF1	SEG13	KEYO1	
2	GIOF3	GIOF3	SEG15	KEYO3	
128	GIOF4	GIOF4	SEG16	KEYO4	
121	FRAME		V2		
125	YDU		V1		
<b>Enable Condition</b>		Default: IO[B0]=0x00, IO[B1]=0x00	IO[B0]=0x2A, IO[B1][7:5]=101	IO[B0]=0x3F, IO[B1][7:6]=11	IO[B0][5:2]=0101





PIN		FUNCTION			
Number	Name	NAND FLASH	UART	IrDA	SPDIF
20	MWR-	WE-			
21	MRD-	RE			
67	A15	CLE			
68	A16	ALE			
121	FRAME	LCM_CE			
123	YSCLK_LP	LCM_RW-			
125	YDU	LCM_CS-			
124	GIOC2		SIN2	IRRX	
126	GIOC3		SOUT2	IRTX	
127	GIOC4				SPDIFRX
<b>Enable Condition</b>	Default	IO[28]=0xFE	IO[70].1=1	IO[70].1=1	IO[70].2=1



## 8. Electrical Characteristics

### 8.1 Absolute Maximum Ratings

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Supply voltage	VDD		-0.5	+2.7	V
	VCC		-0.5	+3.6	V
Input voltage	Vi	VCC $\geq$ 3.3	-0.5	+3.9	V
		VCC < 3.3	-0.5	VCC+0.6	V
Storage temperature	Tstg		-50	+125	°C

#### Cautions

1. Do not short-circuit two or more output pins simultaneously.
2. If even one of the above parameters exceeds the absolute maximum ratings even momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, specify the value exceeding which the product may be physically damaged. Use the product well within these ratings.

The specifications and conditions shown in DC Characteristics and AC characteristics are the ranges for normal operation and quality assurance of the product.

### 8.2 Capacitance (TA = 25°C, VCC = 0 V)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	CI	fc = 1 MHz	—	15	pF
I/O capacitance	CIO	Unmeasured pins returned to 0 V	—	15	pF

### 8.3 DC Characteristics (TA = 25°C, VDD = 2.35 V, VCC = 3.15 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level output voltage	VOH	IOH = -2 mA	2.4	—	—	V
Low-level output voltage	VOL	IOL = 2 mA	—	—	0.4	V
High-level input voltage	VIH		0.6* VCC	—	VCC + 0.6	V
Low-level input voltage	VIL		-0.3	—	0.4V CC	V
Input leakage current	ILI	VCC = 3.6 V, VI = VCC, 0 V	—	—	±10	uA
Output leakage current	ILO	VCC = 3.6 V, VI = VCC, 0 V	—	—	±5	uA
GPIO	Idrive1	Gpioc1,Gpioc3,Gpioc5	—	2.60	—	mA



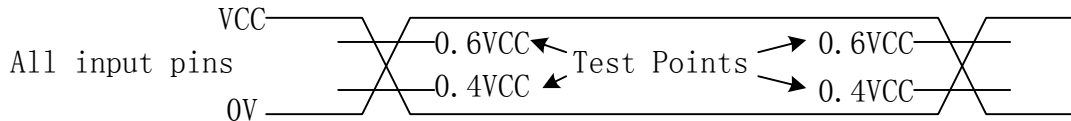
Drive	Idrive2	Other Gpio	—	1.25	—	mA
Supply Current (Two batteries mode)	Ivdd	In Fullspeed mode (MCU run 24.576MHz in internal SRAM,DSP run 24MIPS)	—	40	—	mA
		In Standby mode	—	100	—	uA
	Ivcc	In Fullspeed mode (MCU run 24.576MHz in internal SRAM,DSP run 24MIPS)	—	16	—	mA
		In Standby mode	—	18	—	uA

**Notes 1.** IvDD is a total core power supply current for the VDD power supply. IvDD is applied to the LOGIC and PLL and OSC block.

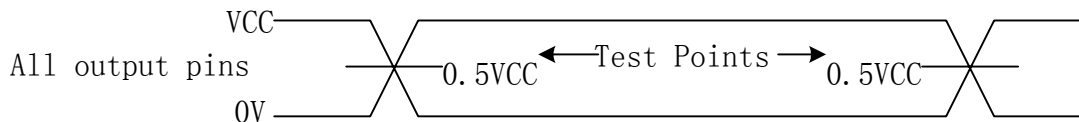
Ivcc is a total I/O power supply current for the 3.3 V power supply. Ivcc is applied to the USB, IO, TP, and AD block.

### 8.4 AC Characteristics (TA = 25°C, VDD = 2 to 2.7 V, VCC = 2.7 to 3.6 V)

AC test input waveform

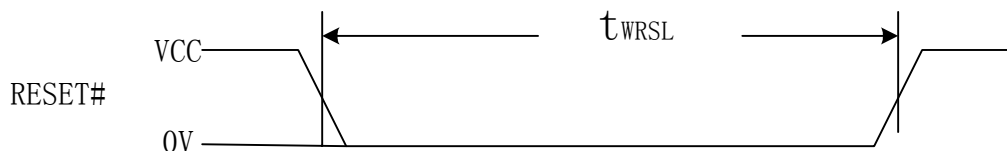


AC test output measuring points



#### (1) Reset parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Reset input low-level width	t <sub>WRSL</sub>	RESET# pin	160		□ns

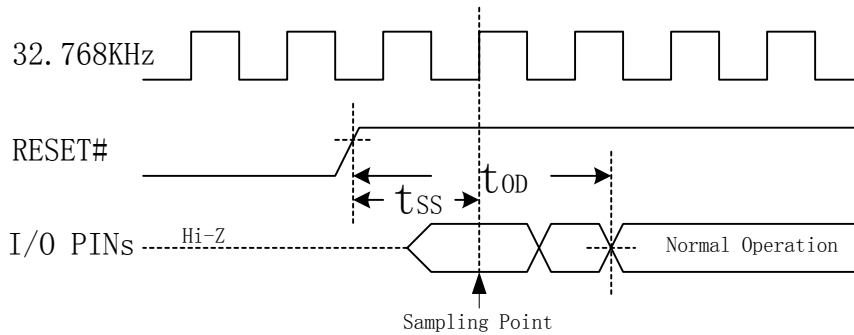


#### (2) Initialization parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data sampling time (from RESET# □)	t <sub>SS</sub>			61.04	□us



Output delay time (from RESET# □)	t <sub>OD</sub>	61.04	□ μs
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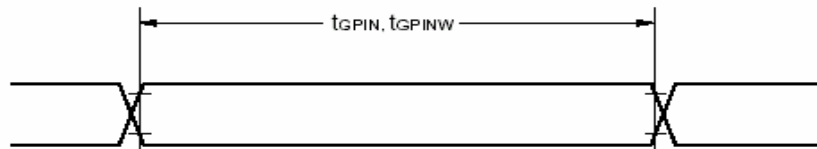


**(3) GPIO interface parameter**

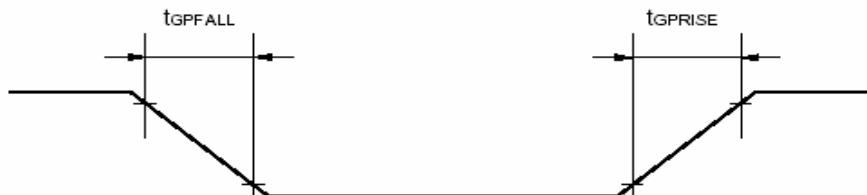
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input level width	t <sub>GPIN</sub>	Normal operation	11/ f <sub>MCUclk</sub>		□ s
GPIO input rise time	t <sub>GPRISE</sub>			200	ns
GPIO input fall time	t <sub>GPFALL</sub>			200	ns
Output level width	t <sub>GPOUT</sub>		11/ f <sub>MCUclk</sub>		ns

**Notes 1.** f<sub>MCUclk</sub> is the frequency that MCU is running upon.

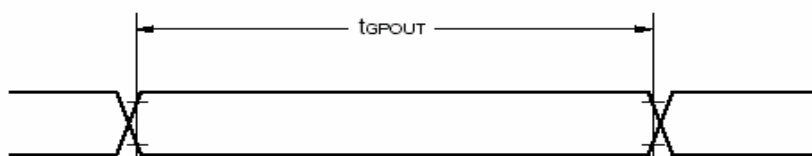
**(a) Input level width**



**(b) Input rise/fall time**



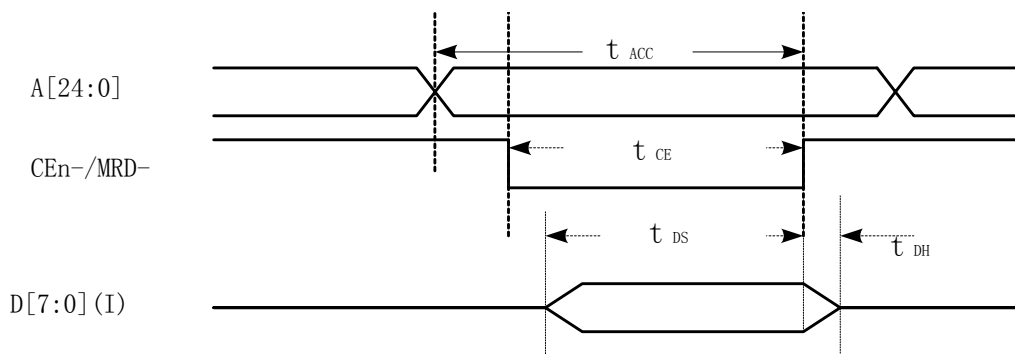
**(c) Output level width**





(4) Ordinary ROM parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data access time (from address) <sup>Note</sup>	t <sub>ACC</sub>	HOSC=24.576MHz Z	102		ns
Data access time (from CEx# □) <sup>Note</sup>	t <sub>CE</sub>	HOSC=24.576MHz Z	82		ns
Data input setup time	t <sub>DS</sub>	HOSC=24.576MHz Z	0		ns
Data input hold time	t <sub>DH</sub>	HOSC=24.576MHz Z	0		ns

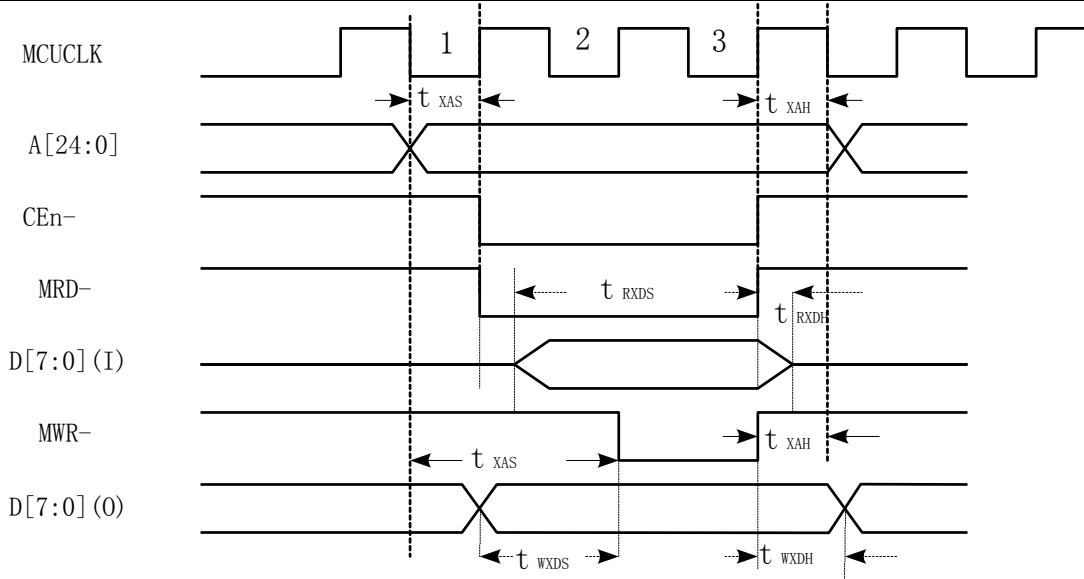


(5) External system bus parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Address setup time (to command signal □) <sup>Note 1, 2</sup>	t <sub>XAS</sub>	Memory Read	0.5T		ns
	t <sub>XAS</sub>	Memory Write	1.5T		ns
Address hold time (from command signal □) <sup>Note 1, 2</sup>	t <sub>XAH</sub>		0.5T		ns
Data output setup time (to command signal □) <sup>Note 1</sup>	t <sub>WXDS</sub>		0	T	ns
Data output hold time (from command signal □) <sup>Note 1</sup>	t <sub>WXDH</sub>		3	0.5T	ns
Data input setup time (to command signal □) <sup>Note 1</sup>	t <sub>RXDS</sub>		0	2T	ns
Data input hold time (from command signal □) <sup>Note 1</sup>	t <sub>RXDH</sub>		0		ns

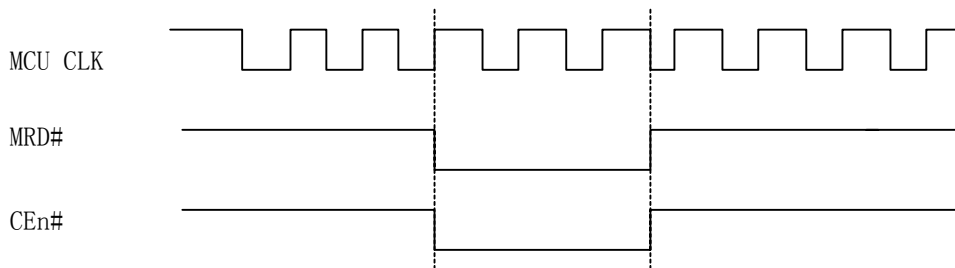
Notes 1. MRD#, MWR# are called the command signals for the External System Bus Interface.

2. T (ns) = 1000 / fMCUCLK

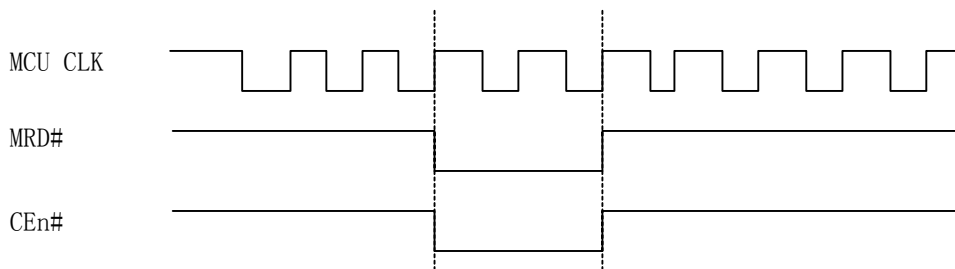


**Bus Operation**

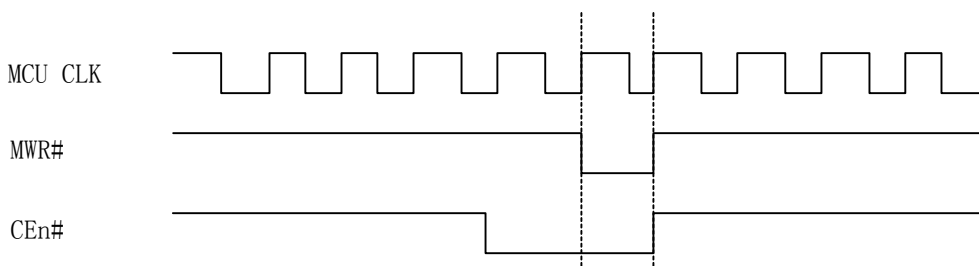
**(a) Instruction fetch cycle**



**(b) Memory read cycle**



**(c) Memory write cycle**





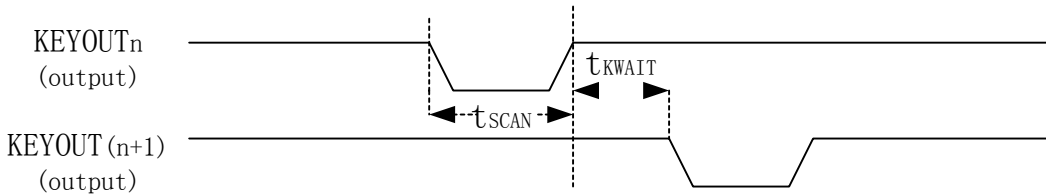
(6) Keyboard interface parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
KEYOUT (7:0) low-level width	tSCAN	Debounce time=2.5ms	130		μs
Voltage stabilization time (KEYOUT n □ □ KEYOUT (n+1) □)	tKWAIT	Debounce time=2.5ms	0		μs
Key scan interval time	tKI	Debounce time=2.5ms	130		μs
Key input delay time (from KEYOUT n □)	tKS	Debounce time=2.5ms	0		μs
Key input hold time (from KEYOUT n □)	tKH	Debounce time=2.5ms	0		μs

Remarks

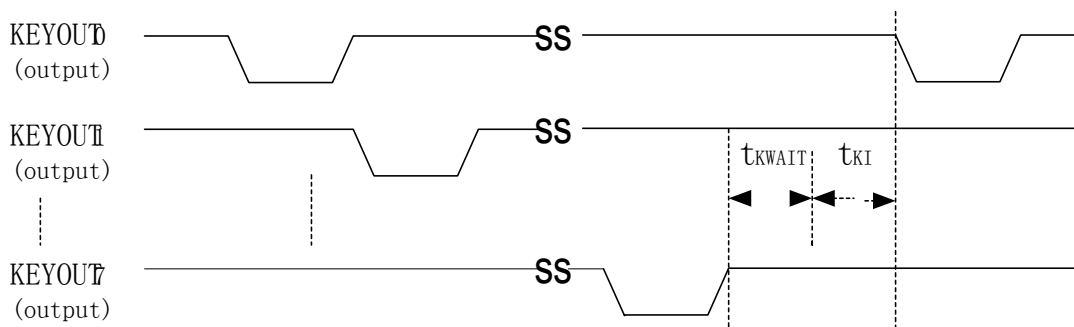
- KEYOUT(7:0) is multiplexed with GIOF(7:0); KEYIN(3:0) is multiplexed with GIOD(7:4); KEYIN(11:4) is multiplexed with GIOE(7:0)
- Keyscan Debouncing time is set thru Bit(2:0) of the MFP Configuration1 Register[0xB1h]
- n = 0 to 7

(a) Keyboard scan parameter 1

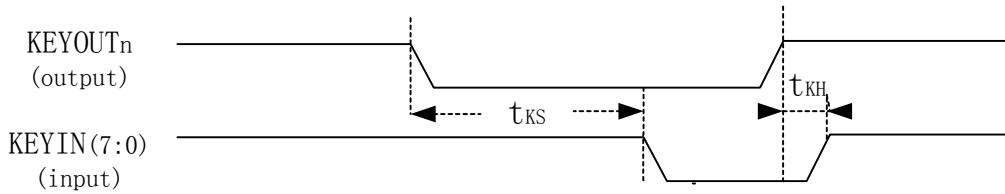


Remark n=0 to 6

(b) Keyboard scan parameter 2



(c) Keyboard port parameter



Remark n=0 to 7

(7) Serial interface parameter

Prescale Value	13		1.625		1	
Baud Rate	Divisor	%Error	Divisor	%Error	Divisor	%Error
600	192	0.16%	-	-	-	-
1200	96	0.16%	-	-	-	-
1800	64	0.16%	-	-	-	-
2000	58	0.53%	-	-	-	-
2400	48	0.16%	-	-	-	-
3600	32	0.16%	256	0.16%	-	-
4800	24	0.16%	192	0.16%	-	-
7200	16	0.16%	128	0.16%	208	0.16%
9600	12	0.16%	96	0.16%	156	0.16%
14400	8	0.16%	64	0.16%	104	0.16%
19200	6	0.16%	48	0.16%	78	0.16%
28800	4	0.16%	32	0.16%	52	0.16%
38400	3	0.16%	24	0.16%	39	0.16%
57600	2	0.16%	16	0.16%	26	0.16%
115200	1	0.16%	8	0.16%	13	0.16%
230400	-	-	4	0.16%	-	-
460800	-	-	2	0.16%	-	-
750000	-	-	-	-	2	0.00%
921600	-	-	1	0.16%	-	-
1500000	-	-	-	-	1	0.00%

Note :

Data transfer rate per bit, which is determined by the divisor of the baud-rate generator that is set with UART1/2 Baud Rate Registers and clock prescaler that is set with UART1/2 Control Registers.





## 9. Typical Performance Characteristics

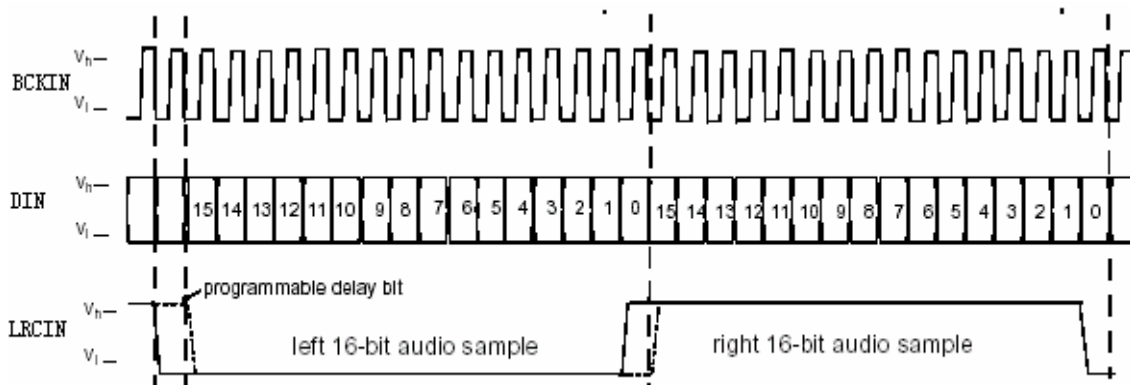
### 9.1 A/D Converter Characteristics

(TA = 25°C, VDD = 2.35 V, VCC = 3.3 V, Sample Rate=32KHz)

Parameter	Symbol	Min	Typ.	Max	Unit
Dynamic range	DR		60		dB
Total Harmonic Distortion + Noise	THD+N	50	53		dB
Frequency Response (20-13KHz)	FR			±1	dB
Full Scale Input Voltage(Gain=0dB)	Vifs		800		mVpp

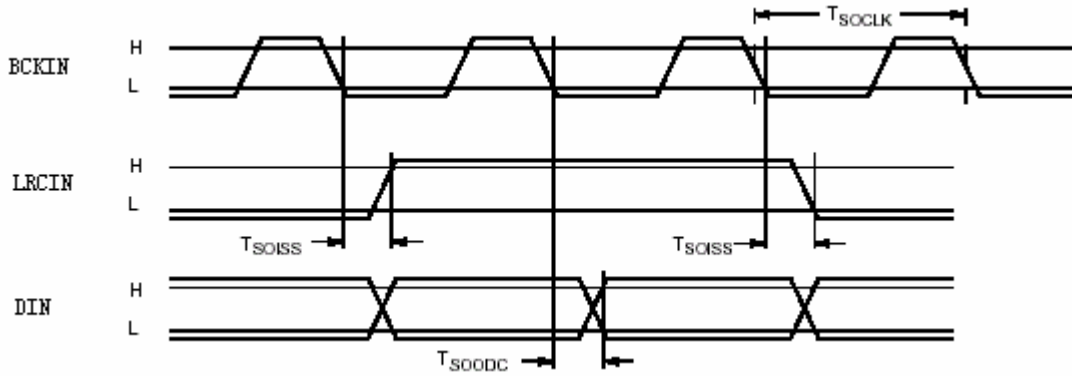
### 9.2 D/A Converter

I<sup>2</sup>S interface parameter



### Characteristics Table

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Clock Output Frequency	<sup>t</sup> SOCLK	48 kHz/s Stereo 16 bit/s		651		ns
Wordstrobe Hold Time after falling edge of clock	<sup>t</sup> SOISS		10		<sup>t</sup> SOCLK/2	ns
Data Hold Time after falling edge of clock	<sup>t</sup> SOODC		10		<sup>t</sup> SOCLK/2	ns



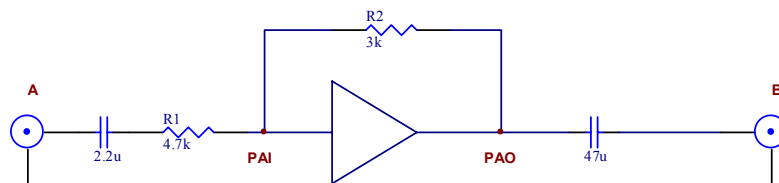
**D/A Converter Characteristics** (TA =25°C, VDD=2.35V, VCC=3.3V, Sample Rate=48KHz, Bias Current=8uA, Quantizer Level=0x05, Volume Level = 0x0D)

Parameter	Symbol	Min	Typ	Max	Unit
Signal / Noise Ratio	SNR		81		dB
Total Harmonic Distortion *	THD+N		0.05		%
Frequency Response 20-20KHz	FR			±0.6	dB
Output Common Mode Voltage	Vcm		1.5		V
Full Scale Output Voltage	Vofs		0.38		Vrms
Interchannel Isolation (1KHz)	Iso		75		dB
Interchannel Gain Mismatch(1KHz)	Mmg		0.025		dB

\* with 32 Ohm load.

### 9.3 Internal Power Amplifier (2 channels)

Test circuit:



Output Power:  
 > 2 x 4mW (32Ohm, use Avdd=2.15V )  
 > 2 x 10mW (32Ohm, use Avcc=3.00V )

**9.4 MCU/DSP Dissipation (I<sub>vdd</sub> VS. Frequency)****MCU Dissipation (V<sub>bat</sub>=3.0V,DSP under reset, MCU runs in internal SRAM)**

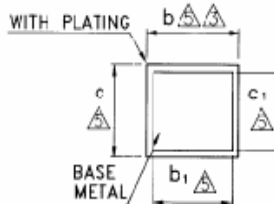
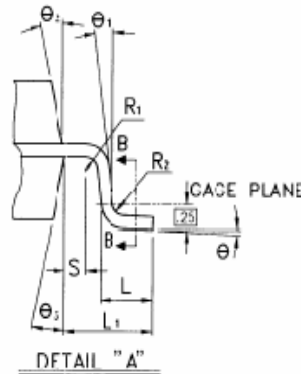
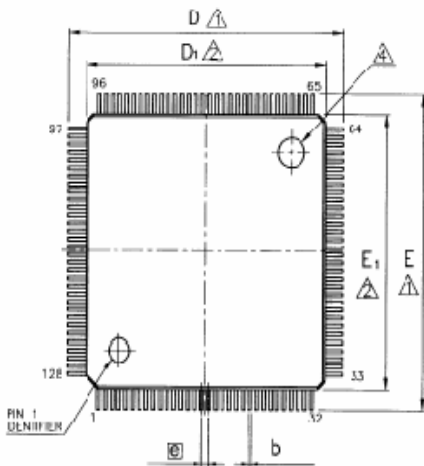
<b>Clock Source</b>	<b>Divisor factor</b>	<b>I<sub>vdd</sub>(Max)</b>
<b>32.768KHZ</b>	<b>/(1—1024)</b>	<b>350uA</b>
<b>24.576MHz</b>	<b>/1</b>	<b>8.5mA</b>
	<b>/2</b>	<b>4.7mA</b>
	<b>/4</b>	<b>2.9mA</b>
	<b>/8</b>	<b>1.8mA</b>
	<b>/16</b>	<b>1.4mA</b>
	<b>/32</b>	<b>1.1mA</b>
	<b>/64</b>	<b>0.96mA</b>
	<b>/128</b>	<b>0.88mA</b>
	<b>/256</b>	<b>0.85mA</b>
	<b>/512</b>	<b>0.84mA</b>
	<b>/1024</b>	<b>0.83mA</b>

**DSP Dissipation (V<sub>bat</sub>=3.0V,MCU in Debug mode)**

<b>DSP Speed (MIPS)</b>	<b>I<sub>vdd</sub> (Max)</b>
<b>6</b>	<b>11.7mA</b>
<b>12</b>	<b>18.8mA</b>
<b>24</b>	<b>30.7mA</b>
<b>36</b>	<b>43.2mA</b>
<b>48</b>	<b>55.9mA</b>



10. Outline Dimension



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	—	—	1.60	—	—	0.063
A <sub>1</sub>	0.05	—	—	0.002	—	—
A <sub>2</sub>	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b <sub>1</sub>	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c <sub>1</sub>	0.09	—	0.16	0.004	—	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636
D <sub>1</sub>	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E <sub>1</sub>	13.90	14.00	14.10	0.547	0.551	0.555
Ⓞ	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L <sub>1</sub>	1.00 REF			0.039 REF		
R <sub>1</sub>	0.08	—	—	0.003	—	—
R <sub>2</sub>	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	C	3.5°	7°	0°	3.5°	7°
θ <sub>1</sub>	C	—	—	0°	—	—
θ <sub>2</sub>	12° TYP			12° TYP		
θ <sub>3</sub>	12° TYP			12° TYP		

NOTE :

- △ TO BE DETERMINED AT SEATING PLANE  $\square\square$ .
- △ DIMENSIONS D<sub>1</sub> AND E<sub>1</sub> DO NOT INCLUDE MOLD PROTRUSION. D<sub>1</sub> AND E<sub>1</sub> ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
- △ DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADII OF THE FOOT.
- △ EXACT SHAPE OF EACH CORNER IS OPTIONAL.
- △ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
- △ A<sub>1</sub> IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
- 7. CONTROLLING DIMENSION : MILLIMETER.
- 8. REFERENCE DOCUMENT : JEDEC MS-026.

SECTION B-B



TIT.E: 128LD LQFP(14x14x1.4mm) PACKAGE OUTLINE -Cu L/F,FOOT/PRINT 2.0mm

L/F MATERIAL: C7025 1/2H

APPR.	<i>[Signature]</i>	DWG NO.	D128-SW1
R&D	<i>[Signature]</i>	REV NO.	A
Q.M	<i>[Signature]</i>	SCALE	
CHK.	<i>[Signature]</i>	DATE	JAN 20, '97
DEN.	J.F.C	SHT NO.	1/1

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