SP2000 Series Analog Array Macrocell Selection Guide

T-42-21

Amplifiers

	Description	V_{os} (mV)	I_b (nA)	E_n (nV/√Hz)	A_{VOL} (dB)	GBW (MHz)	Area (Tiles)	Page
OPA1	General Purpose OpAmp	3	150	10	70	34	0.5	33
OPA2	General Purpose OpAmp	3	150	10	90	23	1	35
OPA3	Precision OpAmp	3	2	20	90	14	1.5	37
OPA5	Clamped Output OpAmp	3	150	10	90	23	1	39
OPA6	Video OpAmp	3	3,000	3	80	300	1	41
OPA21	High Performance OpAmp	3	200	3	125	40	1.5	43

Multiplexing Amplifiers

	Description	V_{os} (mV)	I_b (nA)	E_n (nV/√Hz)	A_{VOL}	GBW (MHz)	Area (Tiles)	Page
MXA1	2-Channel MUX Amp	3.5	12	10	90	20	1.5	45

Low Voltage OpAmps

	Description	V_{cc} Min. (V)	Output Swing (V)	I_b (nA)	E_n (nV/√Hz)	A_{VOL} (dB)	Area (Tiles)	Page
LVA1	Wide CMR	2	V_{cc}-0.2/V_{EE}+0.2	150	10	85	2	47
LVA2	Reduced CMR	2	V_{cc}-0.2/V_{EE}+0.2	150	10	85	1	49

Buffers

	Description	V_{os} (mV)	I_b (nA)	A_{VOL} (dB)	Z_{out} (Ω)	GBW (MHz)	Area (Tiles)	Page
BUF1	Buffer/Opamp	2	150	60	10	50	0.3	51

Sample-and-Hold Amplifiers

	Description	V_{os} (mV)	I_b (nA)	E_n (nV/√Hz)	GBW (MHz)	Aperture (ns)	Acq. (µs)	Hold Step (mV)	Area (Tiles)	Page
SHA1	Voltage Out w/ Switch	2	100	9	8	25	4	1.6	2	53

Transimpedance Amplifiers

	Description	V_{os} (mV)	$+I_b$ (nA)	$-I_b$ (nA)	E_n (nV/√Hz)	A_{VOL} (dB)	R_{OL} (V/mA)	GBW (MHz)	Area (Tiles)	Page
TZA1	General Purpose	2	500	500	100	100	10M	100	2	57

Comparators

	Description	V_{os} (mV)	I_b (nA)	Gain (dB)	V_{OL} (V)	V_{OH} (V)	t_r (ns)	t_f (ns)	t_{pd} (ns)	Area (Tiles)	Page
CMP1	Single Supply, TTL Out	5	1,500	60	0.65	3.75	25	15	30	1	59
CMP2	Dual Supply, TTL Out	1.6	125	91	0.065	3.28	25	25	29	1.5	61
CMP4	Window Comparator	5	500	44	0.65	V_{cc}	—	—	30	1	63

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T-42-21

SP2000 Series Analog Array Macrocell Selection Guide

Multipliers

Description		V_{os} (mV)	I_b (nA)	BW (MHz; R_L=10KΩ)	BW (MHz; R_L=50Ω)	Area (Tiles)	Page
MLT1	Current Out, 4-Quad, VCA	2	100	20	100	2	65
MLT2	Current Out, 4-Quadrant	2	100	20	100	2	67
MLT3	Voltage Out, 4-Quadrant	2	100	20	100	2	69
MLT4	Current Out, TTL Input	2	100	20	100	2	71

Full-Wave Rectifiers

Description		V_{os} (mV)	I_b (nA)	Output Range (mA)	GBW (MHz)	Area (Tiles)	Page
FWR1	Current Source Output	2	200	0— ~2	10	1	73
FWR2	Current Sink Output	2	200	-2 — ~0	10	1	75

Bias Generator

Description		Low TC Current (µA)	PTAT Current (µA)	Number of Outputs	Area (Tiles)	Page
BAS1	I_b and I_{ptat} Cell Bias Source	100	100	as necessary	2	77

Logic Gates

Description		V_{ih} (V)	V_{il} (V)	I_{ih} (µA)	I_{il} (µA)	V_{oh} (V)	V_{ol} (V)	I_{oh} (µA)	I_{ol} (µA)	Area (Tiles)	Page
LBS1	CML Logic Bias Source	-	-	-	-	-	-	-	-	1	79
LBF1	CML Logic Input Buffer	-	-	-	-	1.25	1.5	3	3	0.3	81
NOR1	NOR/OR Gate, CML	1.25	1.5	0.1	2	1.25	1.5	5	7	0.25	83

Function Blocks

Description		V_{ih} (V)	V_{il} (V)	I_{oh} (µA)	I_{ol} (µA)	t_{pd} (ns)	Area (Tiles)	Page
CHP1	Charge Pump, Bipolar Out	0.4	2.8	+200	-200	5	1	85

Voltage References

Description		Output Voltage (V)	Stability (ppm/°C)	Area (Tiles)	Page
RBZ10	10V Buried-Zener	10	<10*	2	87
RBG10	10V Band-Gap	10	40	1	89

T-42-21

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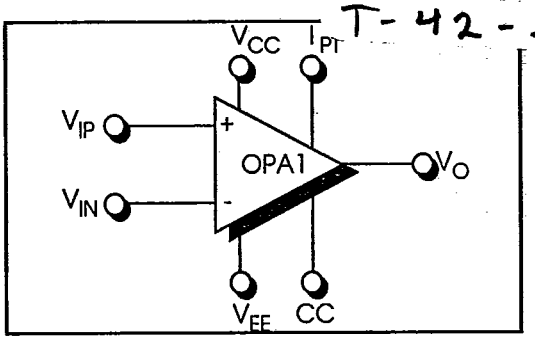
SP2000 Series Analog Array MacroCell
Operational Amplifier — OPA1

T-42-21

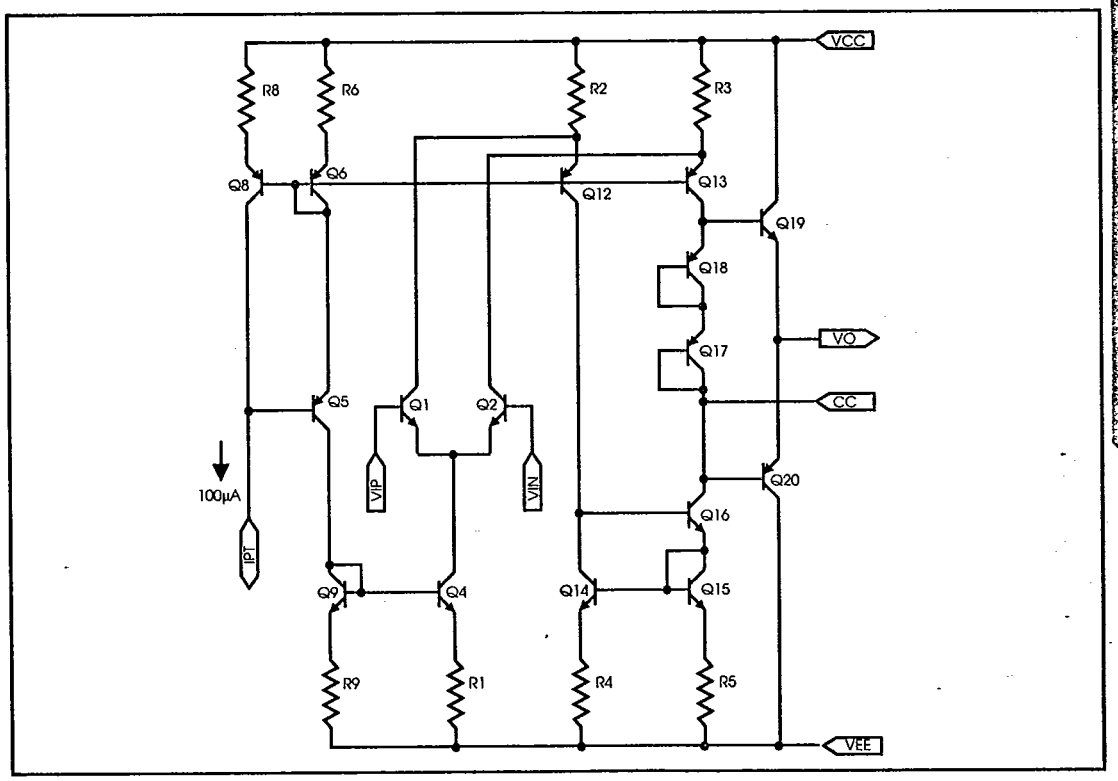
Features

- General Purpose
- 34MHz Gain-Bandwidth
- Unity Gain Compensated (with CC=3pF)
- 14V/µs Slew-Rate
- 0.5mA Supply Current
- Fits in 1/2 Tile
- Design/Layout Available in NiCr



Description

The **OPA1** is a simple opamp designed to fit within 1/2 tile. This opamp is well suited for buffers, gain cells and other applications where offset, drift and drive capability are not critical. The compensation required for **OPA1** is dependent on loading and closed-loop gain. For optimum layout flexibility, the compensation capacitor is added external to the macrocell. The **OPA1** has a bandwidth of 34MHz and a slew-rate of 14V/µs while using only 500µA of supply current.



T-42-21

SP2000 Series Analog Array MacroCell Operational Amplifier — OPA1

Specifications

All specifications at T_A=25°C, V_{CC} = +15V, V_{EE}=-15V, I_{PT}=100µA

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Characteristics						
Offset Voltage	V_{OS}		3	10	mV	
Drift	TCV_{OS}		10		µV/°C	
Bias Current	I_B		150		nA	
Offset Current	I_{OS}		15		nA	
Voltage Noise	e_n		10		nV/√Hz	F=10KHz
Current Noise	i_n		200		fA/√Hz	F=10KHz
Transfer Characteristics						
Common Mode Range	CMR	V_{EE}+2		V_{CC}-2	V	
Common Mode Rejection	CMRR		70		dB	DC
Open Loop Gain	A_{VOL}		70		dB	R_L=10KΩ
Gain-Bandwidth	GBW		34		MHz	R_L=10KΩ, C_L=5pF
Output Characteristics						
Current Sink/Source	I_O			3	mA	
Output Swing	V_O+			V_{CC}-1.5	V	R_L=10KΩ
	V_O-	V_{EE}+1.5			V	R_L=10KΩ
Load Capacitance	C_L			50	pF	C_C=7pF
Transient Response						
Slew Rate	S_r		16		V/µs	R_L=10KΩ, C_L=5pF
Settling Time	T_S		200		ns	to 1%
Power Supply						
Supply Voltage Range	V_{CC}-V_{EE}	8		30	V	
Supply Current	I_{CC}		0.5		mA	I_{PT}=100µA
Rejection	PSRR		70		dB	DC

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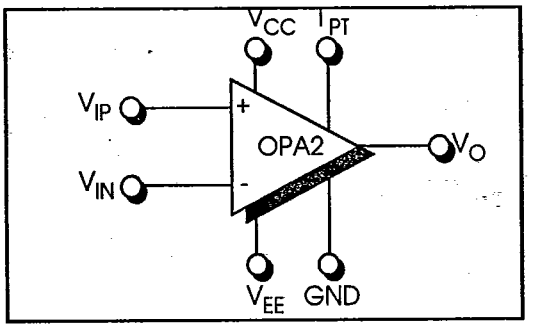
T-42-21

SP2000 Series Analog Array MacroCell
Operational Amplifier — OPA2

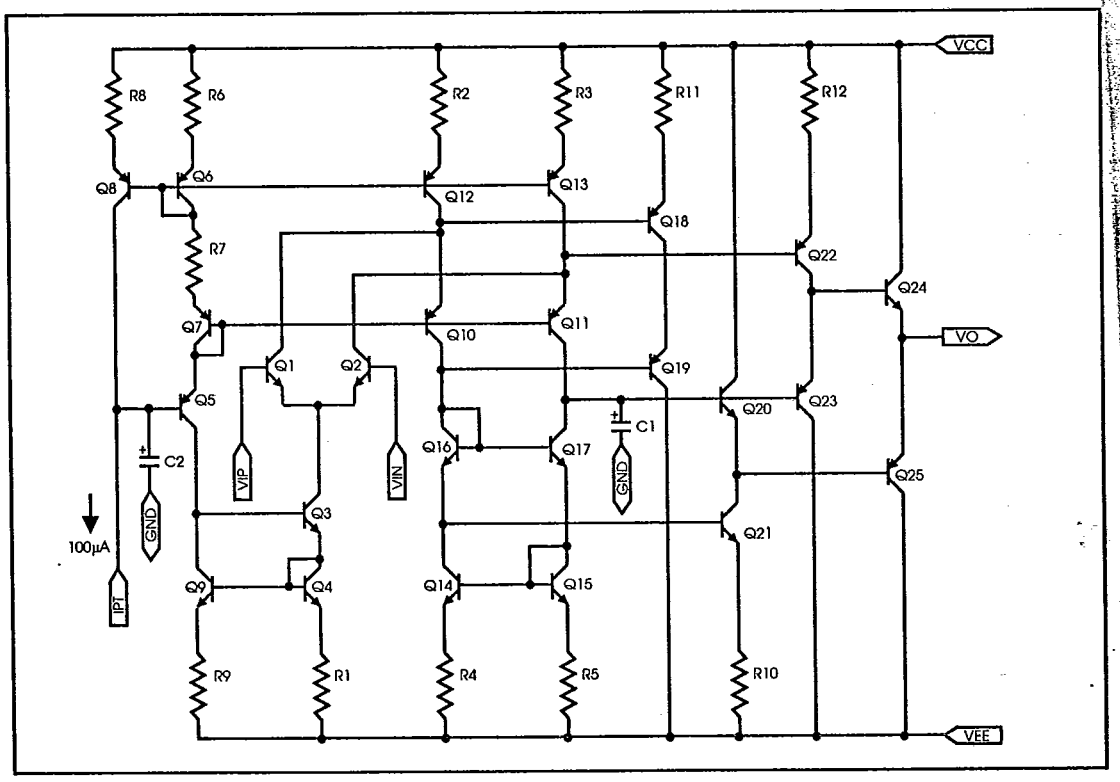
Features

- 25MHz Gain-Bandwidth
- 5mA Output Current Drive
- Compensated to Unity Gain With 5pF
- 1mA Supply Current
- 90dB Open Loop Gain
- Fits in 1 Tile
- Design/Layout Available in NiCr



Description

The **OPA2** is a general purpose opamp with a Class A/B output stage. The circuit has been designed to fit within one (1) tile. The **OPA2** has a bandwidth of 25MHz. It consumes only 1mA of supply current with a 100µA set current. The output stage is designed to drive 5mA loads with "D" devices. For higher output drive currents, larger output transistors can be substituted.



SP2000 Series Analog Array MacroCell Operational Amplifier — OPA2

T-42-21

Specifications

All specifications at T_A=25°C, V_{CC} = +15V, V_{EE}=-15V, I_{PT}=100µA

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Characteristics						
Offset Voltage	V_{OS}		2	5	mV	
Drift	TCV_{OS}		5		µV/°C	
Bias Current	I_B		150	300	nA	
Offset Current	I_{OS}		10	50	nA	
Voltage Noise	e_n		10		nV/√Hz	F=10KHz
Current Noise	I_n		200		fA/√Hz	F=10KHz
Transfer Characteristics						
Common Mode Range	CMR	V_{EE}+2		V_{CC}-2	V	
Common Mode Rejection	CMRR		104		dB	DC
Open Loop Gain	A_{VOL}		90		dB	R_L=10KΩ
Gain-Bandwidth	GBW		23		MHz	R_L=10KΩ, C_L=5pF
Phase Margin	Øm		58		degrees	C_L=10pF
			32		degrees	C_L=50pF
Output Characteristics						
Current Sink/Source	I_O			5	mA	
Output Swing	V_O+		V_{CC}-1.5		V	R_L=10KΩ
	V_O-		V_{EE}+1.5		V	R_L=10KΩ
Load Capacitance	C_L			50	pF	
Transient Response						
Slew Rate	S_r		7		V/µs	R_L=10KΩ, C_L=5pF
Settling Time	T_S		150		ns	to 1%
Power Supply						
Supply Voltage Range	V_{SUPPLY}	8		30	V	V_{CC}-V_{EE}
Supply Current	I_{CC}		1		mA	I_{PT}=100µA
Rejection	PSRR+		108		dB	DC
	PSRR-		92		dB	DC

Note: I_{PTAT} = -100µA for normal biasing and should be PTAT for optimum compensation.

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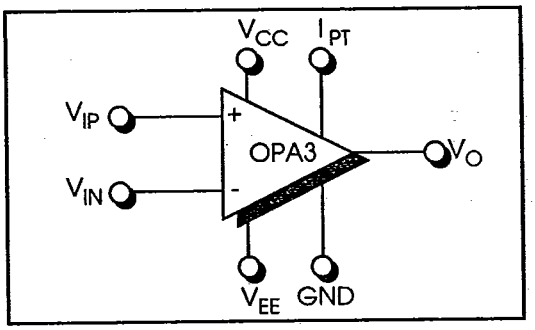
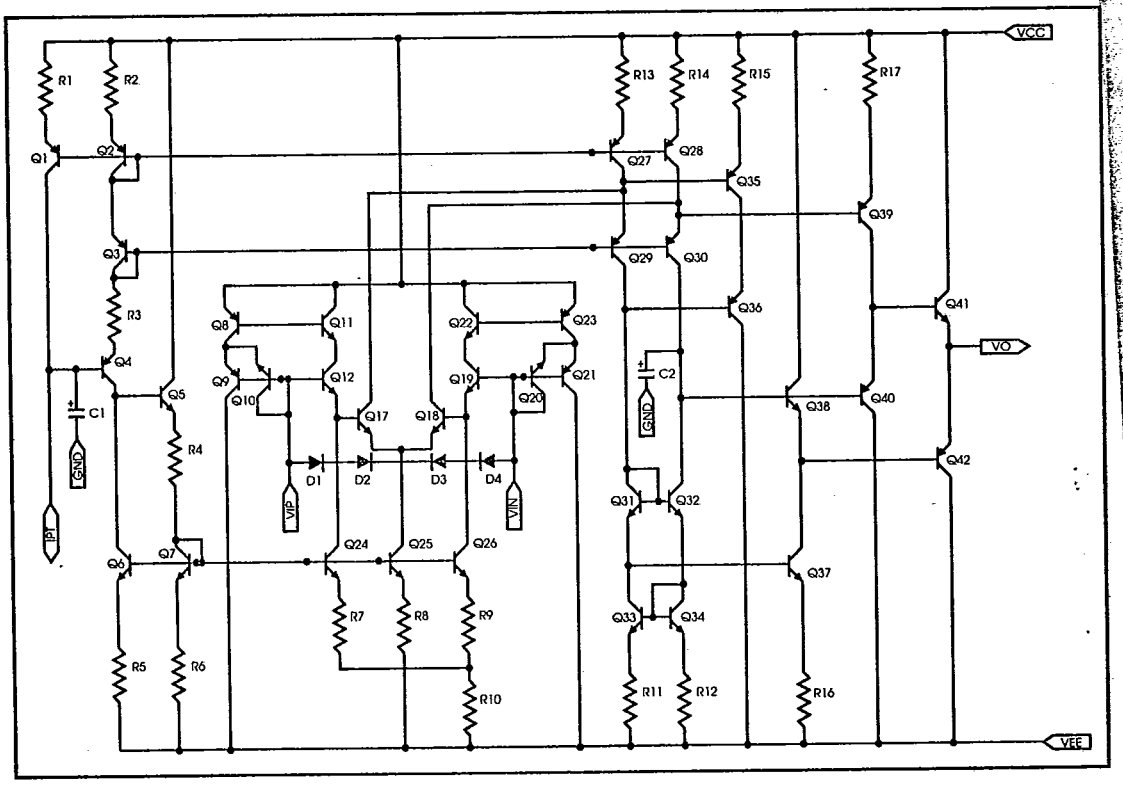
T-42-21

SP2000 Series Analog Array MacroCell
Precision OpAmp — OPA3



Features
- Precision OpAmp
- 14MHz Gain-Bandwidth
- 5mA Output Current Drive
- High Input Impedance
- Unity Gain Compensated
- Low Bias Current — 1nA
- Low Offset Current — 1nA
- 7V/µs Slew Rate
- 1mA Supply Current
- Fits in 1.5 Tiles
- Design/Layout Available in NiCr

Description
The **OPA3** is a precision opamp with a very low bias input stage. The input stage design has high input impedance, low offset current and high common-mode rejection. The amplifier is internally compensated to unity gain; however, it can be adjusted for higher closed-loop gains. The output stage has a driving capability of 5mA. Larger devices can be substituted for higher load current drives. The **OPA3** uses approximately 1.5 tiles and consumes 1mA supply current.



SP2000 Series Analog Array MacroCell Precision OpAmp — OPA3

T-42-21

Specifications

All specifications at T_A=25°C, V_{CC} = +15V, V_{EE}=-15V, I_{PT}=100µA

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Characteristics						
Offset Voltage	V_{OS}		2	7	mV	
Drift	TCV_{OS}		5		µV/°C	
Bias Current	I_B		2	15	nA	
Offset Current	I_{OS}		2		nA	
Voltage Noise	e_n		20		nV/√Hz	F=10KHz
Current Noise	I_n		300		fA/√Hz	F=10KHz
Transfer Characteristics						
Common Mode Range	V_{CM}	V_{EE}+2		V_{CC}-2	V	
Common Mode Rejection	CMRR		80		dB	DC
Open Loop Gain	A_{VOL}		90		dB	R_L=10KΩ
Gain-Bandwidth	GBW		14		MHz	R_L=10KΩ, C_L=20pF
Phase Margin	Øm		50		degrees	R_L= 10KΩ, C_L=20pF, unity gain
Output Characteristics						
Current Sink/Source	I_O			5	mA	
Output Swing	V_O+		V_{CC}-1.5		V	R_L=10KΩ
	V_O-		V_{EE}+1.5		V	R_L=10KΩ
Load Capacitance	C_L			50	pF	
Transient Response						
Slew Rate	S_r		6		V/µs	R_L=10KΩ, C_L=20pF
Settling Time	T_S		100		ns	R_L=10KΩ, C_L=20pF; to 1%
Power Supply						
Supply Voltage Range	V_{SUPPLY}	8		20	V	V_{CC}-V_{EE}
Supply Current	I_{CC}		1		mA	I_{PT}=100µA
Rejection	PSRR		90		dB	DC

Note: I_{PT} = -100µA for normal biasing and should be PTAT for optimum compensation.

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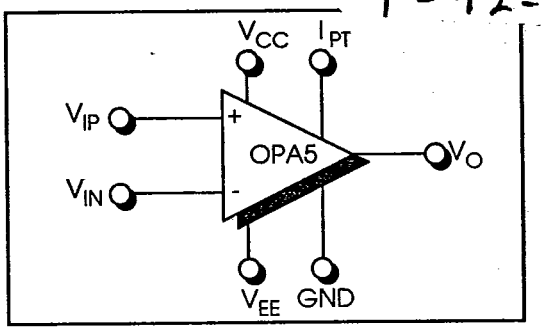
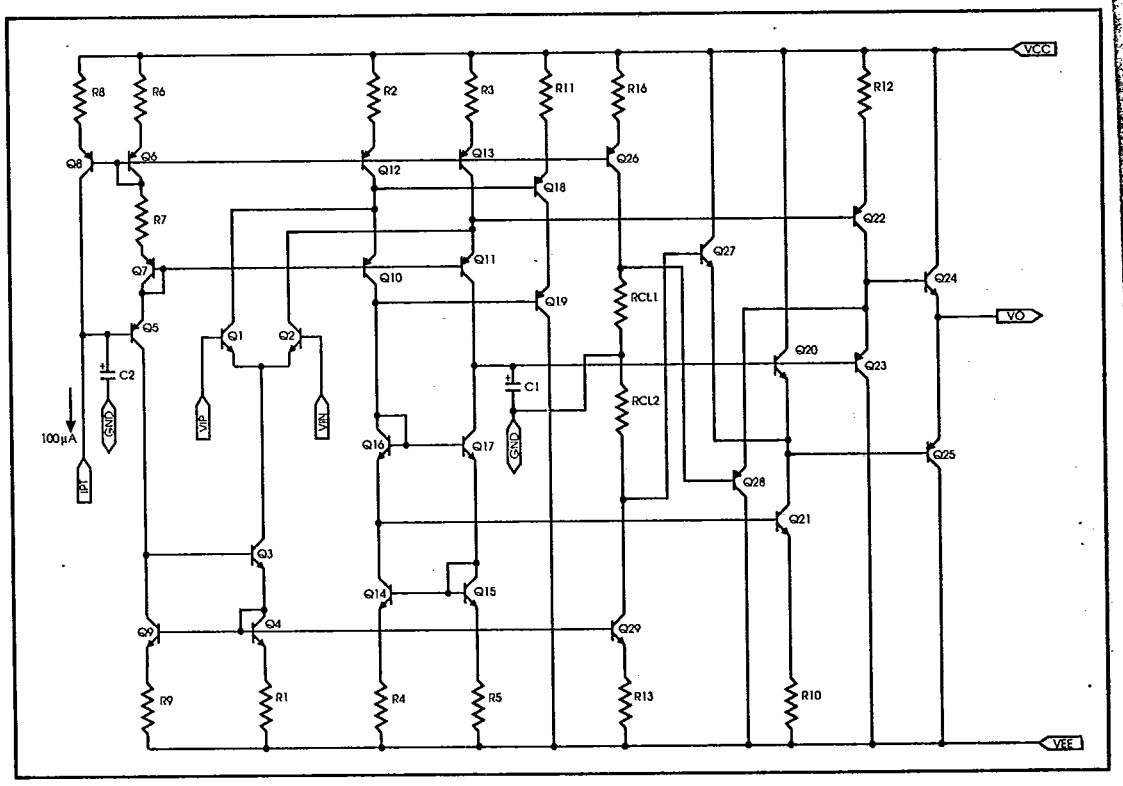
SP2000 Series Analog Array MacroCell
Clamped Output OpAmp — OPA5

T-42-21

Features
- Clamped Output Stage OpAmp
- 23MHz Gain-Bandwidth
- 5mA Output Current Drive
- Unity Gain Compensated
- Limiter
- 7V/μs Slew Rate
- 1mA Supply Current
- Fits in 1 Tile
- Design/Layout Available in NiCr



Description
The **OPA5** is essentially the same as the **OPA2** with the addition of a clamping circuit to the output stage. The output swing clamp voltages can be adjusted by setting the vaue of two resistors in the clamp circuit. The clamp voltages can be arbitrarily set for symetrical, asymetrical or unipolar values. The **OPA5** uses 1 tile and consumes 1mA supply current.



T-42-21

SP2000 Series Analog Array MacroCell Clamped Output OpAmp — OPA5

Specifications

All specifications at T_A=25°C, V_{CC} = +15V, V_{EE}=-15V, I_{PT}=100µA

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Characteristics						
Offset Voltage	V_{OS}		2	5	mV	
Drift	TCV_{OS}		5		µV/°C	
Bias Current	I_B		150	300	nA	
Offset Current	I_{OS}		10	50	nA	
Voltage Noise	e_n		10		nV/√Hz	F=10KHz
Current Noise	I_n		200		fA/√Hz	F=10KHz
Transfer Characteristics						
Common Mode Range	V_{CM}	V_{EE}+2		V_{CC}-2	V	
Common Mode Rejection	CMRR		104		dB	DC
Open Loop Gain	A_{VOL}		90		dB	R_L=10KΩ
Gain-Bandwidth	GBW		23		MHz	R_L=10KΩ, C_L=5pF
Output Characteristics						
Current Sink/Source	I_O			5	mA	
Output Swing	V_O+		V_{CC}-1.5		V	R_L=10KΩ
	V_O-		V_{EE}+1.5		V	R_L=10KΩ
Load Capacitance	C_L			50	pF	
Clamp Voltage	V_{CL}	V_{EE}+2		V_{CC}-2	V	See notes
Transient Response						
Slew Rate	S_r		7		V/µs	R_L=10KΩ, C_L=20pF
Settling Time	T_S		150		ns	R_L=10KΩ, C_L=20pF; to 1%
Power Supply						
Supply Voltage Range	V_{SUPPLY}	8		30	V	V_{CC}-V_{EE}
Supply Current	I_{CC}		1		mA	I_{PT}=100µA
Rejection	PSRR+		108		dB	
	PSRR-		92		dB	

Notes:
1) I_{PT} = -100µA for normal biasing and should be PTAT for optimum compensation.
2) Clamp voltages are set by: $+V_{CL} = (0.2mA)R_{CL1}$
$-V_{CL} = (0.2mA)R_{CL2}$

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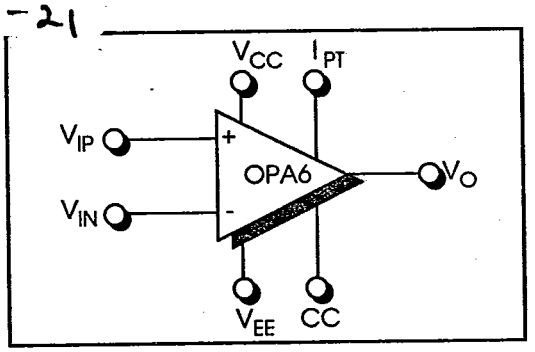
SP2000 Series Analog Array MacroCell
Video OpAmp — OPA6

T-42-21

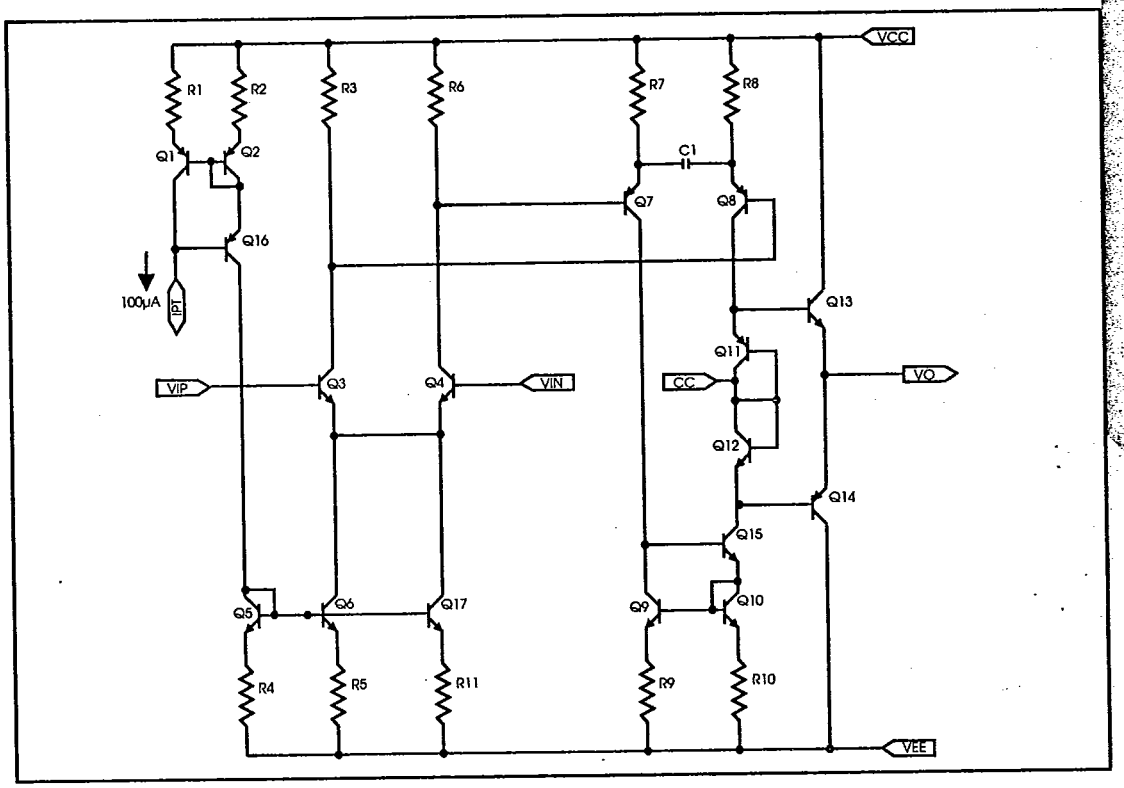
Features

- 300MHz Bandwidth
- 200V/µs Slew Rate
- 30ns Settling Time to 1%
- 2.5mA Supply Current
- Fits in <1 Tile
- Design/Layout Available in NiCr



Description

The **OPA6** is a very high-speed operational amplifier suitable for video applications with closed-loop gains greater than 35dB. For lower closed-loop gain settings, a compensation capacitor to ground at CC should be used. Compensation might also be required for capacitive loading at the output.



SP2000 Series Analog Array MacroCell
Video OpAmp — OPA6

T-42-21

Specifications

All specifications at T_A=25°C, V_{CC} = +15V, V_{EE}=-15V, I_{PT}=100µA

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Characteristics						
Offset Voltage	V_{OS}		3	5	mV	
Drift	TCV_{OS}		10		µV/°C	
Bias Current	I_B		3		µA	
Offset Current	I_{OS}		300		nA	
Voltage Noise	e_n		3		nV/√Hz	F=10KHz
Current Noise	i_n		600		fA/√Hz	F=10KHz
Transfer Characteristics						
Common Mode Range	V_{CM}	V_{EE}+2.5		V_{CC}-2	V	
Common Mode Rejection	CMRR		55		dB	DC
Open Loop Gain	A_{VOL}		80		dB	R_L=10KΩ
Gain-Bandwidth	GBW		300		MHz	R_L=10KΩ, C_L=5pF
Output Characteristics						
Current Sink/Source	I_O			5	mA	
Output Swing	V_O+		V_{CC}-2		V	R_L=10KΩ
	V_O-		V_{EE}+2		V	R_L=10KΩ
Load Capacitance	C_L			20	pF	
Transient Response						
Slew Rate	S_r		200		V/µs	R_L=10KΩ, C_L=5pF
Settling Time	T_S		30		ns	R_L=10KΩ, C_L=5pF; to 1%
Power Supply						
Supply Voltage Range	V_{SUPPLY}	8		30	V	V_{CC}-V_{EE}
Supply Current	I_{CC}		1		mA	I_{PT}=100µA
Rejection	PSRR+		40		dB	
	PSRR-		55		dB	DC

Notes:
1) I_{PT} = -100µA for normal biasing and should be PTAT for optimum compensation.
2) For higher than 5pF load capacitance, series resistance and/or increased compensation might be required

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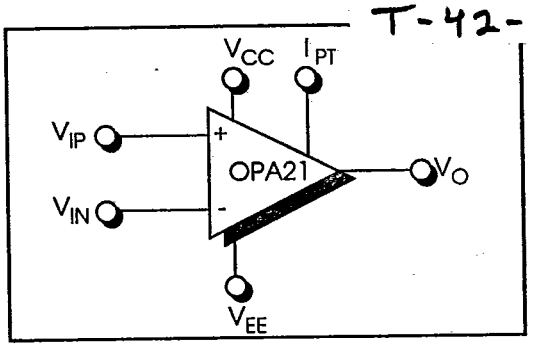
SP2000 Series Analog Array MacroCell
High Performance OpAmp — OPA21

T-42-21

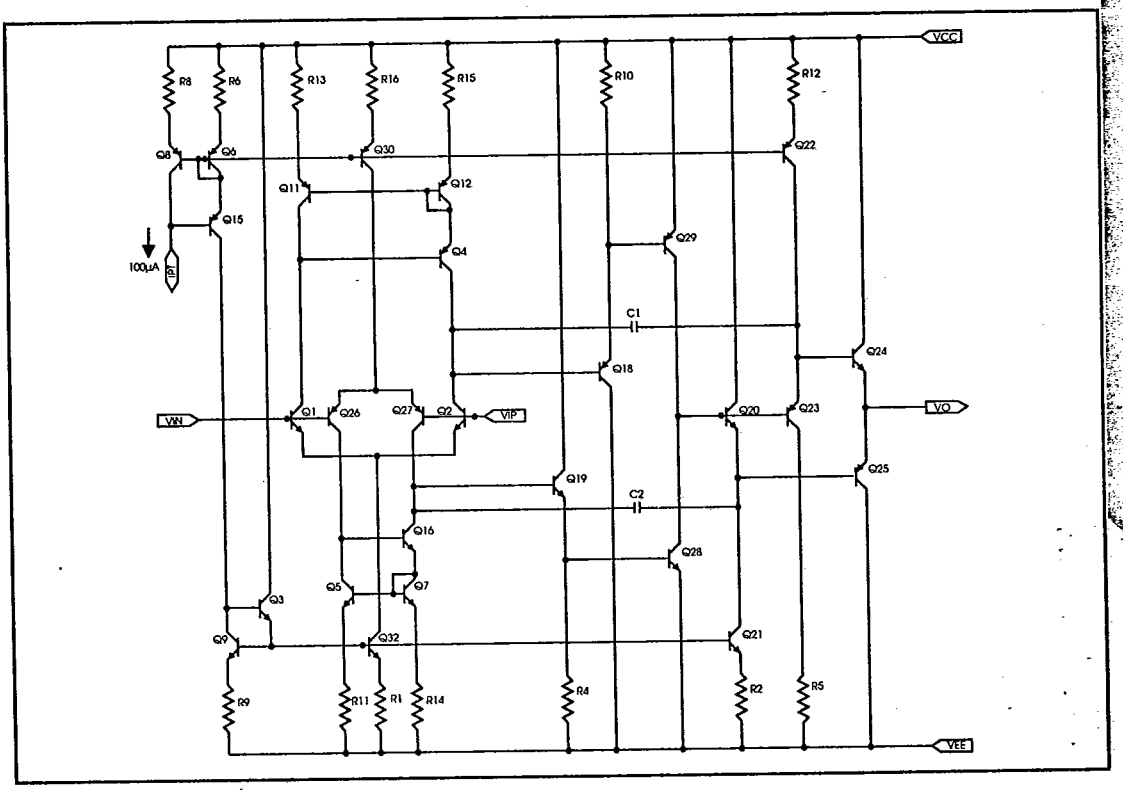
Features

- Low Noise — 3nV/√Hz
- High Open-Loop Gain — 125dB
- Low Input Bias Current — 200nA
- Wide Bandwidth — 40MHz
- High Slew Rate — 20V/μs
- Low DC Offset — 3mV (untrimmed)
- Fits in 1.5 Tile
- Design/Layout Available in NiCr



Description

The **OPA21** provides a new measure of performance for general-purpose op-amps. It has operating specifications that generally equal or exceed those of the HA-5104-type amplifier in all categories of performance. The **OPA21** is well-suited to accurate signal processing applications by virtue of its low input offset voltage, input bias current and input voltage noise. It features a 40MHz bandwidth and very high open-loop gain. The mirror image design of this cell is very suitable for applications where low distortion and symmetrical slewing are desired. It is internally compensated for gains greater than 2.



SP2000 Series Analog Array MacroCell
High Performance OpAmp — OPA21

T-42-21

Specifications

All specifications at T_A=25°C, V_{CC} = +15V, V_{EE}=-15V, I_{PT}=100µA

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Characteristics						
Offset Voltage	V_{OS}		3		mV	
Drift	TCV_{OS}		10		µV/°C	
Bias Current	I_B		1200		nA	
Offset Current	I_{OS}		20		nA	
Voltage Noise	e_n		3		nV/√Hz	F=1KHz
Transfer Characteristics						
Common Mode Range	V_{CM}	V_{EE}+2		V_{CC}-2	V	
Common Mode Rejection	CMRR		130		dB	DC
Open Loop Gain	A_{VOL}		125		dB	R_L=10KΩ
Gain-Bandwidth	GBW		40		MHz	R_L=10KΩ, C_L=20pF
Output Characteristics						
Current Sink/Source	I_O		5		mA	
Output Swing	V_{OUT}	V_{EE}+1.5		V_{CC}-1.5	V	R_L=10KΩ
Load Capacitance	C_L			50	pF	
Transient Response						
Slew Rate	S_r		20		V/µs	R_L=10KΩ, C_L=20pF
Settling Time	T_S		250		ns	V_O=10V_{P-P}, R_L=10KΩ, C_L=20pF; to 1%
Power Supply						
Supply Voltage Range	V_{SUPPLY}	8		30	V	V_{CC}-V_{EE}
Supply Current	I_{CC}		2.5		mA	
Rejection	PSRR		130		dB	DC

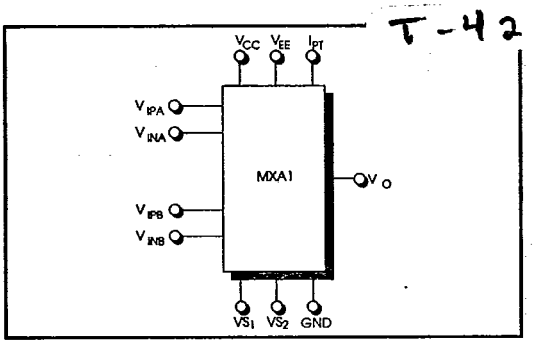
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP2000 Series Analog Array MacroCell
2-Channel Multiplexing Amplifier — MXA1

T-42-21

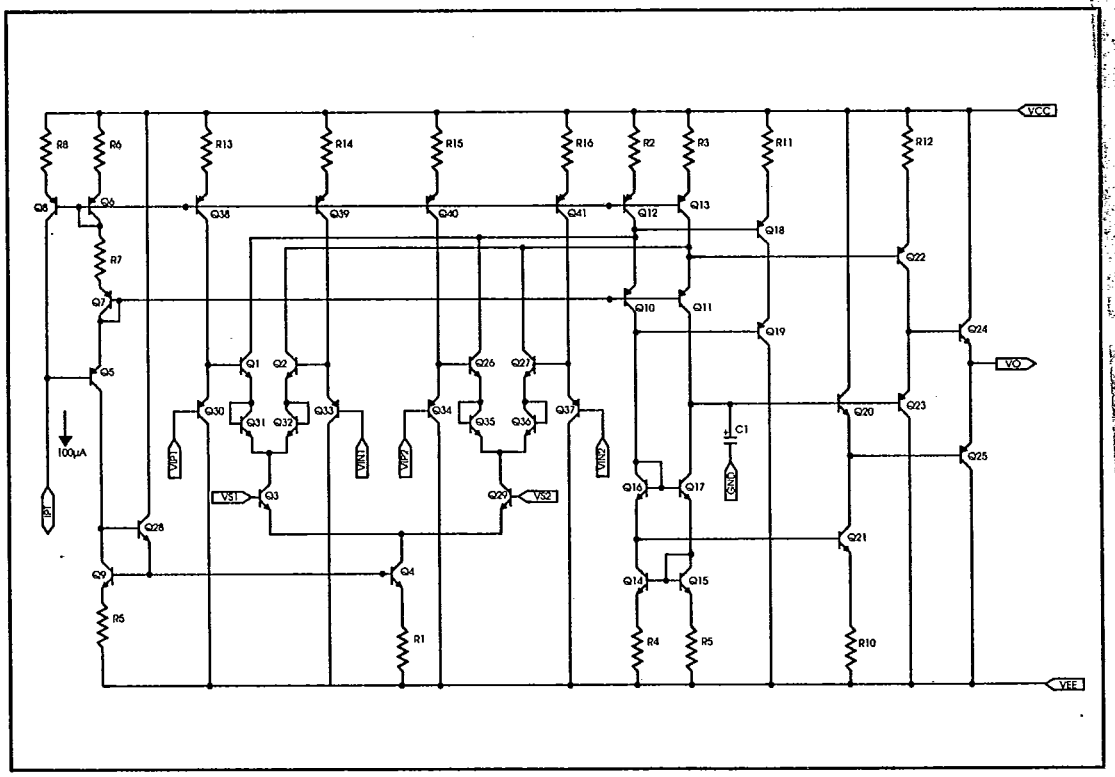
Features

- SPDT Operation, Expandable
- 20MHz Gain-Bandwidth
- Unity Gain Stable
- 11V/µs Slew Rate
- 10ns Delay Time
- -110dB Crosstalk (DC)
- 20V Maximum Input Differential
- 1.5mA Supply Current
- Fits in 1.5 Tiles
- Design/Layout Available in NiCr



Description

The **MXA1** is a 2-channel, input stage multiplexing opamp. The operation of the amplifier is that of an SPDT switch. The switching inputs (VS1 and VS2) can be switched from a differential driver similar to the **LBF1** logic buffer macrocell. The **MXA1** can be expanded to additional switched inputs by adding parallel input stages. The inputs have emitter-follower buffers to reduce bias current and to increase the maximum differential input voltage



2-Channel MUX Amplifier — MXA1

SP2000 Series Analog Array MacroCell
2-Channel Multiplexing Amplifier — MXA1

T-42-21

Specifications

All specifications at T_A=25°C, V_{CC} = +15V, V_{EE}=-15V, I_{PT}=100µA

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Characteristics						
Offset Voltage	V_{OS}		3.5	10	mV	
Drift	TCV_{OS}		12		µV/°C	
Bias Current	I_B		200	600	nA	
Offset Current	I_{OS}		10	60	nA	
Voltage Noise	E_n		10		nV/√Hz	F=10KHz
Current Noise	I_n		200		fA/√Hz	F-10KHz
Transfer Characteristics						
Common Mode Range	V_{CM}	V_{EE}+2		V_{CC}-2	V	
Common Mode Rejection	CMRR		90		dB	DC
Open Loop Gain	A_{VOL}		90		dB	R_L=10KΩ
Gain-Bandwidth	GBW		20		MHz	R_L=10KΩ, C_L=5pF
Phase Margin	θ_m		58		degrees	C_L=10pF
			32		degrees	C_L=50pF
Output Characteristics						
Current Sink/Source	I_O			5	mA	
Output Swing	V_{OUT}	V_{EE}+1.5		V_{CC}-1.5	V	R_L=10KΩ
Load Capacitance	C_L			50	pF	
Transient Response						
Slew Rate	S_r		11		V/µs	R_L=10KΩ, C_L=5pF
Settling Time	T_s		200		ns	R_L=10KΩ, C_L=5pF; to 1%
Power Supply						
Supply Voltage Range	V_{SUPPLY}	8		30	V	V_{CC}-V_{EE}
Supply Current	I_{CC}		1.5		mA	I_{PT} = -100µA
Rejection	PSRR+		90		dB	DC
	PSRR-		90		dB	DC

Notes:

I_{PTAT} = -100µA for normal biasing, and should be PTAT for optimum compensation

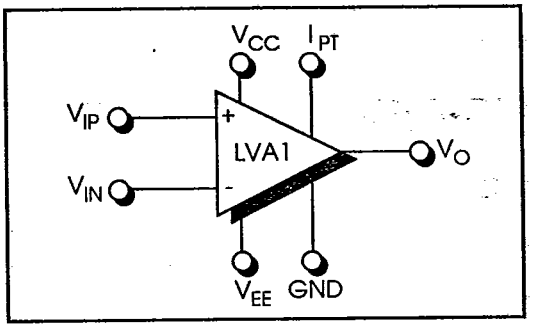
T-42-21

SIGNAL PROCESSING EXCELLENCE

SP2000 Series Analog Array MacroCell
Low Voltage OpAmp — LVA1

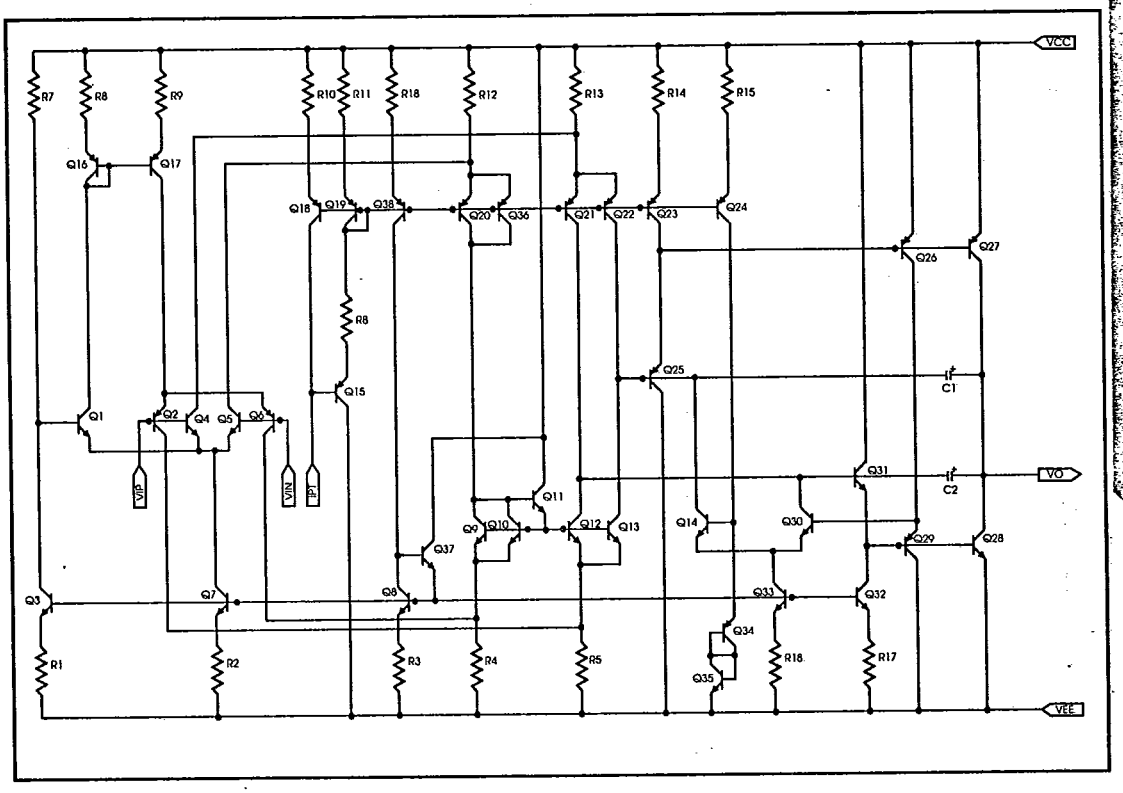
Features

- Low Voltage Operation — 2V Minimum Supply
- Operation From Single or Split Supply Voltages
- Output Voltage Swing to Within 0.1V of Supplies
- 10MHz Gain-Bandwidth
- Unit-Gain Compensated
- 7V/µs Slew Rate
- 20mA Output Drive
- 1mA Supply Current
- Fits in 1.5 Tiles
- Design/Layout Available in NiCr



Description

The **LVA1** is designed to operate with a supply voltage as low as 2.0V. The input common-mode rejection of the **LVA1** is from rail to rail. The output stage can swing to within 0.1V of the rails, which is accomplished by using common emitter output stages. The open-loop gain of the amplifier therefore, is affected by the load impedance.



SP2000 Series Analog Array MacroCell
Low Voltage OpAmp — LVA1

T-42-21

Specifications

All specifications at T_A=25°C, V_{CC} = +5V, V_{EE}=-5V, I_{PT}=100µA

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Characteristics						
Offset Voltage	V_{OS}		2	5	mV	
Drift	TCV_{OS}		10		µV/°C	
Bias Current	I_B		150		nA	
Offset Current	I_{OS}		15		nA	
Voltage Noise	e_n		10		nV/√Hz	F=10KHz
Transfer Characteristics						
Common Mode Range	V_{CM}	V_{EE}		V_{CC}	V	
Common Mode Rejection	CMRR		80		dB	DC
Open Loop Gain	A_{VOL}		85		dB	R_L=10KΩ
Gain-Bandwidth	GBW		10		MHz	R_L=10KΩ
Phase Margin	Øm		60		degrees	
Output Characteristics						
Current Sink/Source	I_O		5		mA	Note 1
Output Swing	V_O+		V_{CC}-0.2		V	R_L=10KΩ
	V_O-		V_{EE}+0.2		V	R_L=10KΩ
Load Capacitance	C_L			100	pF	
Transient Response						
Slew Rate	S_r		7		V/µs	R_L=10KΩ, C_L=10pF
Settling Time	T_S		200		ns	R_L=10KΩ, C_L=10pF; to 1%
Power Supply						
Supply Voltage Range	V_{SUPPLY}	2		10	V	V_{CC}-V_{EE}
Supply Current	I_{CC}		1		mA	I_{PT}=100µA
Rejection	PSRR+		80		dB	DC
	PSRR-		80		dB	DC

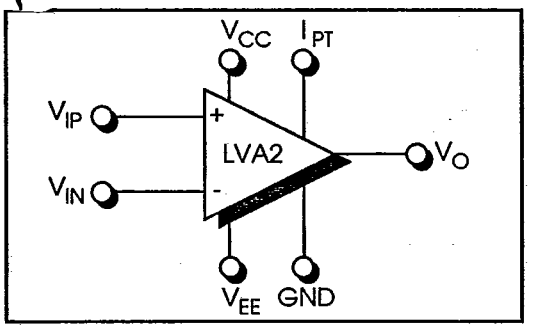
Note:
1. Output current drive can be increased by increasing the size of the output transistors.

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

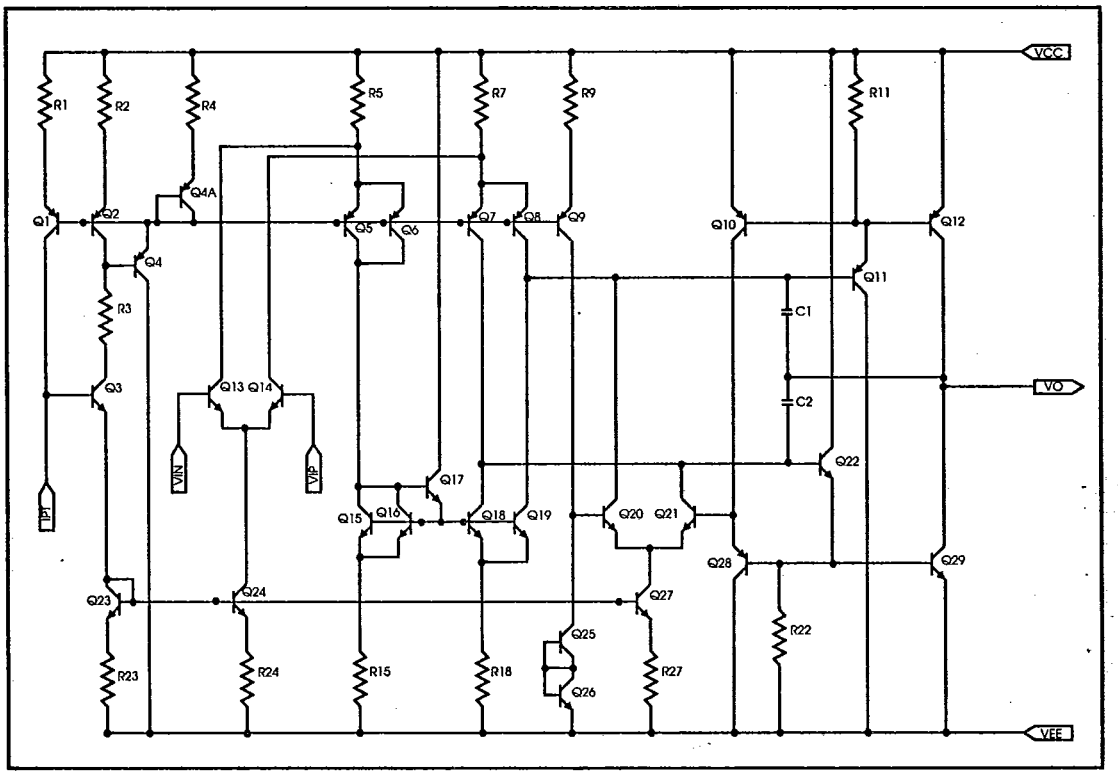
T-42-21

SP2000 Series Analog Array MacroCell
Low Voltage OpAmp — LVA2

Features
- Low Voltage Operation — 2V Minimum Supply
- Single or Split Supply Operation
- Output Voltage Swing to Within 0.2V of Supplies
- 10MHz Gain-Bandwidth
- Unit-Gain Compensated
- 7V/µs Slew Rate
- 20mA Output Drive
- 1mA Supply Current
- Fits in 1.5 Tiles
- Design/Layout Available in NiCr



Description
The **LVA2** is a low-voltage opamp similar to the **LVA1**. It is designed to operate with a supply voltage as low as 2.0V. The output stage is designed to provide wide (near rail-to-rail) output swing. The **LVA2** has a simplified input stage for applications which do not require a CMR to the negative rail (i.e. ground-referenced input signals in single-supply systems). The reduced component count allows the **LVA2** to be implemented in one tile.



T-42-21

SP2000 Series Analog Array MacroCell
Low Voltage OpAmp — LVA2

Specifications

All specifications at T_A=25°C, V_{CC} = +5V, V_{EE}=-5V, I_{PT}=-100µA

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Characteristics						
Offset Voltage	V_{OS}		2	5	mV	
Drift	TCV_{OS}		10		µV/°C	
Bias Current	I_B		150		nA	
Offset Current	I_{OS}		15		nA	
Voltage Noise	e_n		10		nV/√Hz	F=10KHz
Transfer Characteristics						
Common Mode Range	V_{CM}	V_{EE}+2		V_{CC}	V	
Common Mode Rejection	CMRR		80		dB	DC
Open Loop Gain	A_{VOL}		85		dB	R_L=10KΩ
Gain-Bandwidth	GBW		10		MHz	R_L=10KΩ
Phase Margin	Øm		60		degrees	
Output Characteristics						
Current Sink/Source	I_O		5		mA	Note 1
Output Swing	V_O+		V_{CC}-0.2		V	R_L=10KΩ
	V_O-		V_{EE}+0.2		V	R_L=10KΩ
Load Capacitance	C_L			100	pF	
Transient Response						
Slew Rate	S_r		7		V/µs	R_L=10KΩ, C_L=10pF
Settling Time	T_S		200		ns	R_L=10KΩ, C_L=10pF; to 1%
Power Supply						
Supply Voltage Range	V_{SUPPLY}	2		30	V	V_{CC}-V_{EE}
Supply Current	I_{CC}		1		mA	I_{PT}=100µA
Rejection	PSRR+		80		dB	DC
	PSRR-		80		dB	DC

Note:
1. Output current drive can be increased by increasing the size of the output transistors.

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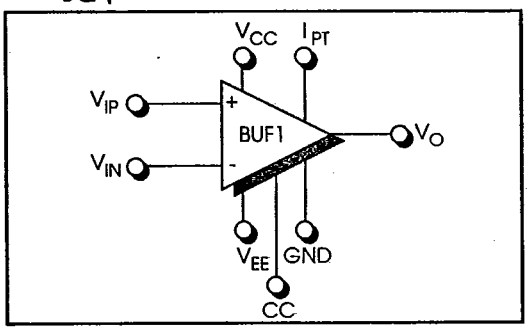
SIGNAL PROCESSING EXCELLENCE

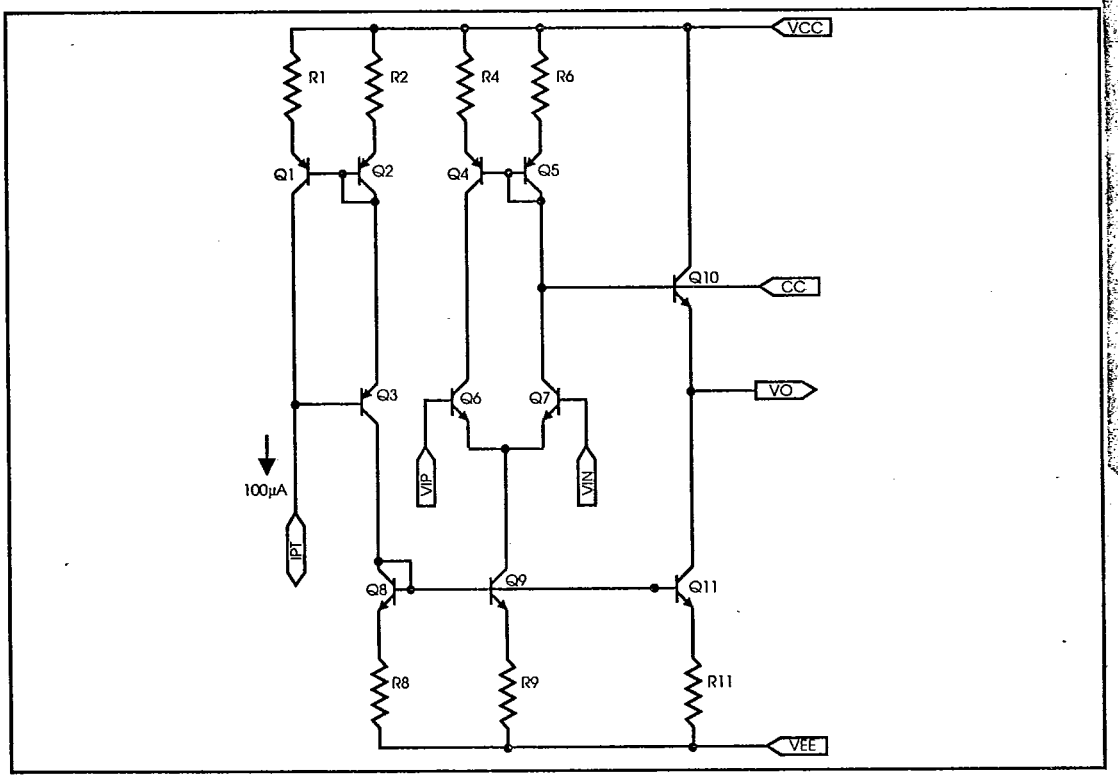
T-42-21

SP2000 Series Analog Array MacroCell
Buffer Amplifier —BUF1

Features
- General-Purpose Buffer or Gain Block
- 25MHz Gain-Bandwidth
- Unity-Gain Compensated (with CC=3pF)
- 12V/µs Slew Rate
- 0.7mA Supply Current
- Fits in <0.5 Tile
- Design/Layout Available in NiCr



Description
The **BUF1** is a simple opamp suitable for use as a buffer stage or gain block. The output drive of the **BUF1** is very limited and should be used only to drive fairly high impedances. The **BUF1** should normally be used only in a non-inverting configuration. The amount of compensation depends on the closed-loop gain setting and capacitive loading. A 3pF compensation capacitor is sufficient for unity-gain and less than 10pF loading.



SP2000 Series Analog Array MacroCell
Buffer Amplifier — BUF1

T-42-21

Specifications

All specifications at T_A=25°C, V_{CC} = +15V, V_{EE}=-15V, I_{PT}=-100µA

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Characteristics						
Offset Voltage	V_{OS}		5	15	mV	
Drift	TCV_{OS}		10		µV/°C	
Bias Current	I_B		150		nA	
Offset Current	I_{OS}			50	nA	
Voltage Noise	e_n		10		nV/√Hz	F=10KHz
Current Noise	i_n		200		fA/√Hz	F=10KHz
Transfer Characteristics						
Common Mode Range	V_{CM}	V_{EE}+2		V_{CC}-2	V	
Common Mode Rejection	CMRR		50		dB	DC
Open Loop Gain	A_{VOL}		60		dB	R_L=10KΩ
Gain-Bandwidth	GBW		25		MHz	R_L=10KΩ, C_L=5pF
Phase Margin	Øm		45		degrees	C_L=10pF
Output Characteristics						
Current Sink/Source	I_O			0.3	mA	
Output Swing	V_O+		V_{CC}-1.5		V	R_L=10KΩ
	V_O-		V_{EE}+1.5		V	R_L=10KΩ
Load Capacitance	C_L			10	pF	
Transient Response						
Slew Rate	S_r		7		V/µs	R_L=10KΩ, C_L=10pF, C_C=3pF
Settling Time	T_S		150		ns	R_L=10KΩ, C_L=10pF, C_C=3pF;1%
Power Supply						
Supply Voltage Range	V_{SUPPLY}	8		30	V	V_{CC}-V_{EE}
Supply Current	I_{CC}		0.7		mA	I_{PT}=100µA
Rejection	PSRR+		50		dB	DC
	PSRR-		50		dB	DC

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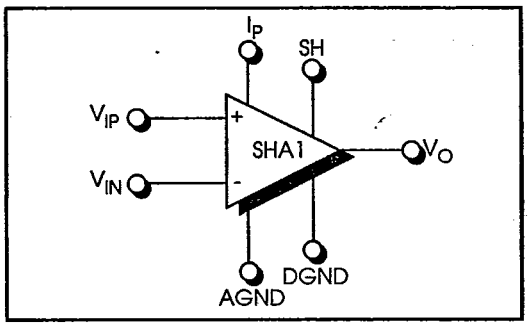
SIGNAL PROCESSING EXCELLENCE

SP2000 Series Analog Array MacroCell
Sample-and Hold Amplifier & Switch — SHA1

T-42-21

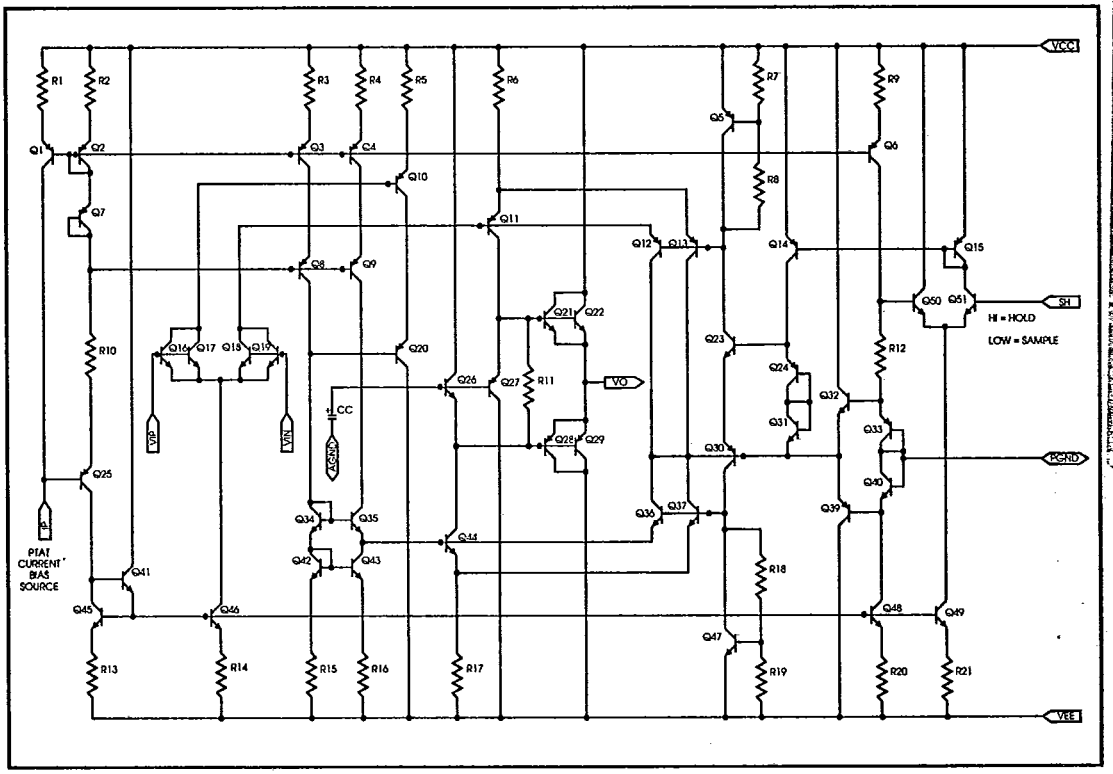
Features

- Switched (Tri-Stated) Amplifier
- Shunt-capacitor S/H Amplifier
- 8MHz Gain-Bandwidth
- 2.5V/µs Slew-Rate
- 4µs Acquisition Time
- 25ns Aperture Time
- 1.6mV Hold Step Error
- Fits in 2 Tiles
- Design/Layout Available in NiCr



Description

The **SHA1** macrocell is a sample-and-hold (S/H) amplifier and switch. When the switch is activated, the output stage of the amplifier is disabled, causing it to go into a high-impedance state. The normal application of the **SHA1** would be in driving a shunt hold capacitor in a S/H loop. To complete the loop, a high-impedance buffer amplifier would be connected to the hold capacitor. The output stage of the **SHA1** does not use replicate feedback, which minimizes hold step error.



SP2000 Series Analog Array MacroCell
Sample-and Hold Amplifier & Switch — SHA1

T-42-21

Specifications

All specifications at -55°C≤T_A≤+125°C; V_{CC} = +15V, V_{EE}=-15V; I_P=100µA; C_{HOLD} = 1000pF; R_L = 10KΩ ; Unity–Gain Configuration; Mode Input: V_{LO}=0.0V, V_{HI}=3.0V; Rise/Fall Time = 20ns

Parameters	Min.	Typ.	Max.	Units	Conditions
Analog Input Characteristics					
Offset Voltage		1.0	4.0	mV	25°C
Offset Voltage Drift		3		µV/°C	Full temperature range
Bias Current		100	300	nA	25°C
		130	400	nA	Full temperature range
Offset Current		5	30	nA	25°C
		10		nA	Full temperature range
Differential Input Resistance		200	500	KΩ	25°C
Common Mode Range		±13	±14	V	V_{OUT}=0V; full temperature range
Input Noise Density					At 100KHz; 25°C
Voltage		9		µV/√Hz	Track mode
Current		360		fA/√Hz	
Transfer Characteristics					
DC Gain		90		dB	V_{OUT}=±10V
Gain-Bandwidth		8		MHz	C_{HOLD}=1000pF; 25°C
Common Mode Rejection		115		dB	DC; 25°C
Rejection		90		dB	DC; 1V_{p-p} ripple on either supply
Output Characteristics					
Current Current					R_{LOAD}=250Ω; full temperature range
Source		26		mA	
Sink		21		mA	
Output Swing		±14		V	Full temperature range
Output Resistance		1000		Ω	25°C; I_{LOAD}=1mA; open-loop config.
Maximum C_{HOLD} for Stability		2000		pF	Phase margin = 30°; full temp. range
Transient Response					
Slew Rate		2.5		V/µs	25°C; ±10V step input
Rise Time		70		ms	25°C; C_{HOLD}=1000pF, V_{OUT}=200mV_{p-p}
Overshoot		3.5		%	25°C; C_{HOLD}=1000pF, V_{OUT}=200mV_{p-p}
Digital Input Characteristics					
Low Input Voltage			0.8	V	Full temperature range
High Input Voltage	2.0			V	Full temperature range
Low Input Current		10		pA	V_{SH}=0V; full temperature range
High Input Current		1.5		µA	V_{SH}=5V; full temperature range
Hold-To-Sample Characteristics					
Acquisition Time					
10V Step, ±0.1% FS		4.0		µs	±10mV; 25°C
10V Step, ±0.01% FS		4.3		µs	±1mV; 25°C
Sample-To-Hold Characteristics					
Aperture Time		25		ns	Note 1; 25°C
Effective Aperture Delay		±5		ns	25°C
Aperture Uncertainty				ps	25°C
Settling Time to ±0.01%		25		ns	±1mV; 25°C
Transient Amplitude		0.7		mV	25°C
Hold Step		1.6		mV	C_{HOLD}=1000pF; 25°C
Hold Step Drift		25		µV/°C	Full temperature range

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP2000 Series Analog Array MacroCell
Sample-and Hold Amplifier & Switch — SHA1

T-42-21

Specifications (continued)

All specifications at -55°C≤T_A≤+125°C; V_{CC} = +15V, V_{EE}=-15V; I_P=100µA; C_{HOLD} = 1000pF; R_L = 10KΩ ; Unity-Gain Configuration; Mode Input: V_{LO}=0.0V, V_{HI}=3.0V; Rise/Fall Time = 20ns

Parameters	Min.	Typ.	Max.	Units	Conditions
Sample-To-Hold Characteristics					
Charge Transfer		1.6		pC	= Hold Step * C_{HOLD}; 25°C
Hold Mode Characteristics					
Droop Rate					V_{OUT}=0.0V, C_{HOLD}=1000pF
		10		µV/ms	25°C
		1700		µV/ms	125°C
Drift Current					= Droop Rate * C_{HOLD}
		10		pA	25°C
		1700		pA	125°C
Feedthrough Attenuation		96		dB	V_{IN}=20V_{p-p} at 100kHz; ±3dB over 10Hz-10MHz
Power Supply					
I_{SUPPLY}^+					V_{IN}=0V, V_{OUT}=0V; track/hold modes
		3.6		mA	25°C
		4.0		mA	125°C
I_{SUPPLY}^-					V_{IN}=0V, V_{OUT}=0V; track/hold modes
		3.6		mA	25°C
		4.0		mA	125°C

Notes:

T-42-21

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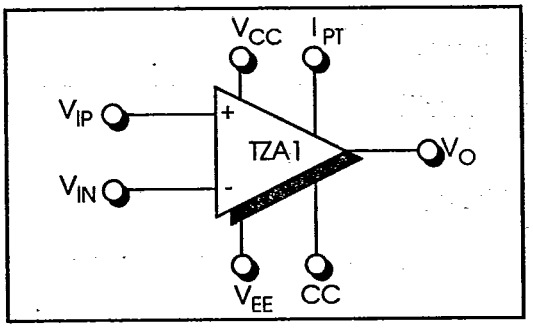
SIGNAL PROCESSING EXCELLENCE

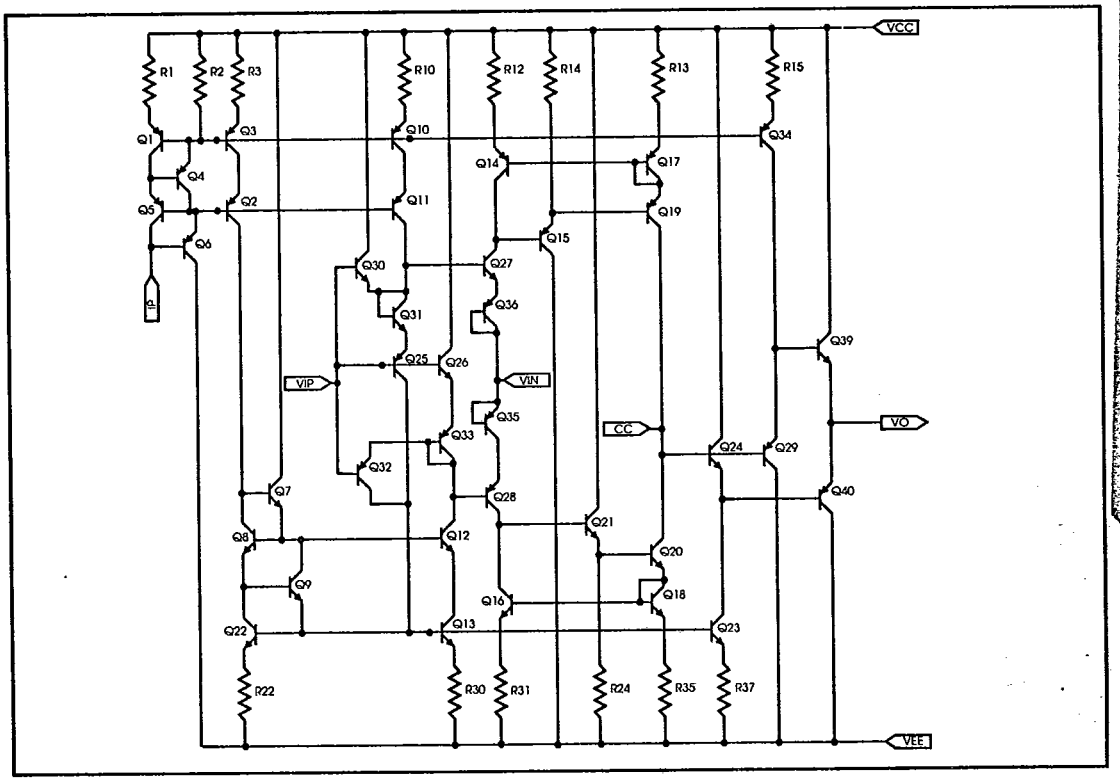
T-42-21

SP2000 Series Analog Array MacroCell
TransImpedance Amplifier — TZA1

Features
- 50MHz Bandwidth
- 400V/µs Slew Rate
- 110ns Settling Time
- 2.7mA Supply Current
- Fits in 1.5 Tiles
- Design/Layout Available in NiCr



Description
The **TZA1** is a transimpedance amplifier. The inverting input is designed for low impedance, current-mode operation. The non-inverting input is high impedance. The input signal is therefore a current applied to V_{IN}. Feedback between V_{IN} and V_O converts the input current to a voltage. Due to the low impedance nature of V_{IN}, the transimpedance configuration is insensitive to input shunt capacitance, and provides high-speed transimpedance (I/V) conversion. The **TZA1** can also be configured as a high-speed buffer by driving the non-invertng input (V_{IP}) and connecting a feedback resistor.



SP2000 Series Analog Array MacroCell TransImpedance Amplifier — TZA1

T-42-21

Specifications

All specifications at 0°C≤T_A≤70°C, V_{CC} = +15V, GND=0V,

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Characteristics						
Input Offset Voltage	V_{OS}		2	8	mV	
Drift	TCV_{OS}		13	25	µV/°C	
Input Bias Current (V_{IP})	I_B		0.5		µA	
Voltage Noise	E_N		100		nV/√Hz	F=10kHz
Transfer Characteristics						
Transimpedance	Z_{OL}		140		dB	R_L=10kΩ, C_L=20pF, $Z_{OL}=V_O/I_{IN}$ open loop
Voltage Gain	A_{VOL}		100		dB	R_L=10KΩ
Bandwidth	BW		50		MHz	
Output Characteristics						
Output Swing	V_{OUT}	V_{EE}+1.5		V_{CC}-1.5	V	
Output Current	I_O		15		mA	Sink or source, R_L=10K Ω
Transient Response						
Slew Rate	S_r		400		V/µs	R_L=10KΩ
Settling Time	T_S		110		ns	to 1%, R_L=10KΩ
Power Supply						
Supply Voltage Range	V_{CC}-V_{EE}	10		30	V	
Supply Current	I_{CC}		2.7		mA	
Power Supply Rejection	PSRR		60		dB	

Note:
For capacitive loads exceeding 10pF, compensation (CC) may be required depending on the value of the feedback resistor.

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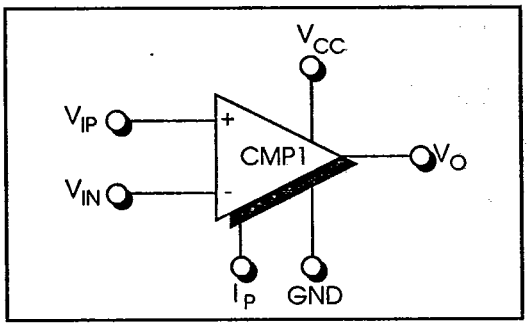
SIGNAL PROCESSING EXCELLENCE

SP2000 Series Analog Array MacroCell
Single-Supply TTL Comparator — CMP1

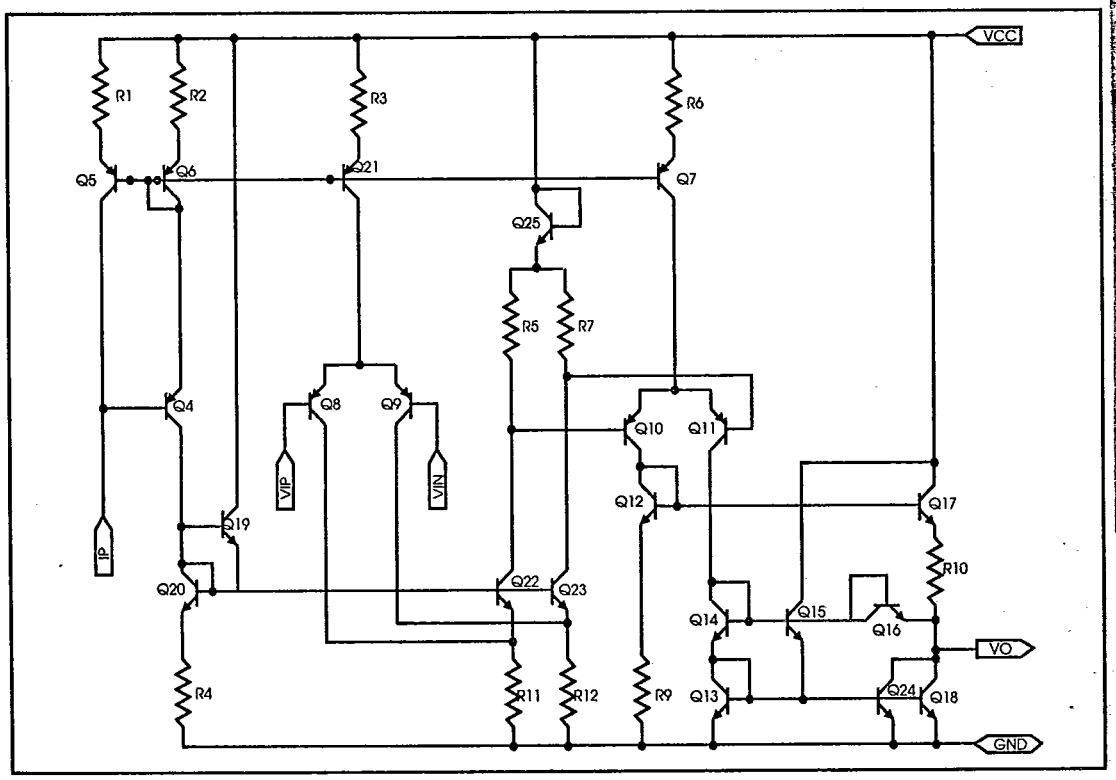
Features

- Single-Supply Operation
- TTL Output Levels
- 25ns Response Time
- Input CMR Includes Ground
- Fits in 1 Tile
- Design/Layout Available in NiCr



Description

The **CMP1** is a TTL-output comparator configured to operate with either single or split supply voltages. The V_{OL} of the comparator is achieved with a saturated output stage so that V_{OL} will be relative to the negative supply voltage. The input common mode range includes ground (or V_{EE} when powered by a split supply). Due to the long recovery time associated with a saturated output stage implemented in a DI process, a relatively high V_{OL} of 0.6V has been implemented. A lower V_{OL} can be traded-off for longer recovery time.



T-42-21

SP2000 Series Analog Array MacroCell Single-Supply TTL Comparator — CMP1

Specifications

All specifications at 0°C≤T_A≤70°C, V_{CC} = +15V, GND=0V,

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Characteristics						
Input Offset Voltage	V_{OS}		5	20	mV	
Input Bias Current	I_B		1.5		µA	
Transfer Characteristics						
Gain			60		dB	
Common Mode Range	V_{CM}	GND		V_{CC}-3	V	
Common Mode Rejection	CMRR		70	90	dB	
Output Characteristics						
Output Current						
Source	$-I_{OUT}$		2		mA	
Sink	$+I_{OUT}$		2		mA	
Output Low Voltage	V_{OL}		600		mV	$+I_{OUT}$=1mA
Output High Voltage	V_{OH}		3.2		V	
Transient Response						
Response Time	T_D					C_L=20pF
Low-to-High			25		ns	
High-to-Low			15		ns	
Power Supply						
Supply Voltage Range	V_{SUPPLY}	5		20	V	V_{CC}-GND
Supply Current	I_{SUPPLY}		2		mA	V_{CC}=+15V, I_{OUT}=0
Power Supply Rejection	PSRR	70	96		dB	
Output Voltage Swing	V_O		5		V	

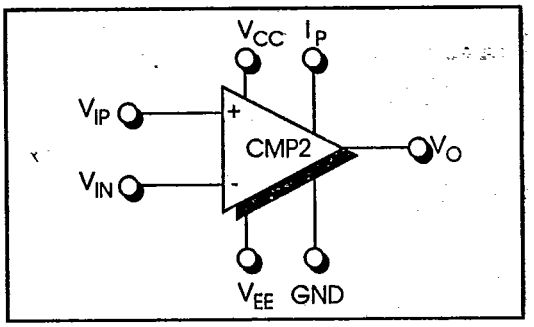
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

T-42-21

SP2000 Series Analog Array MacroCell
Split-Supply TTL Comparator — CMP2

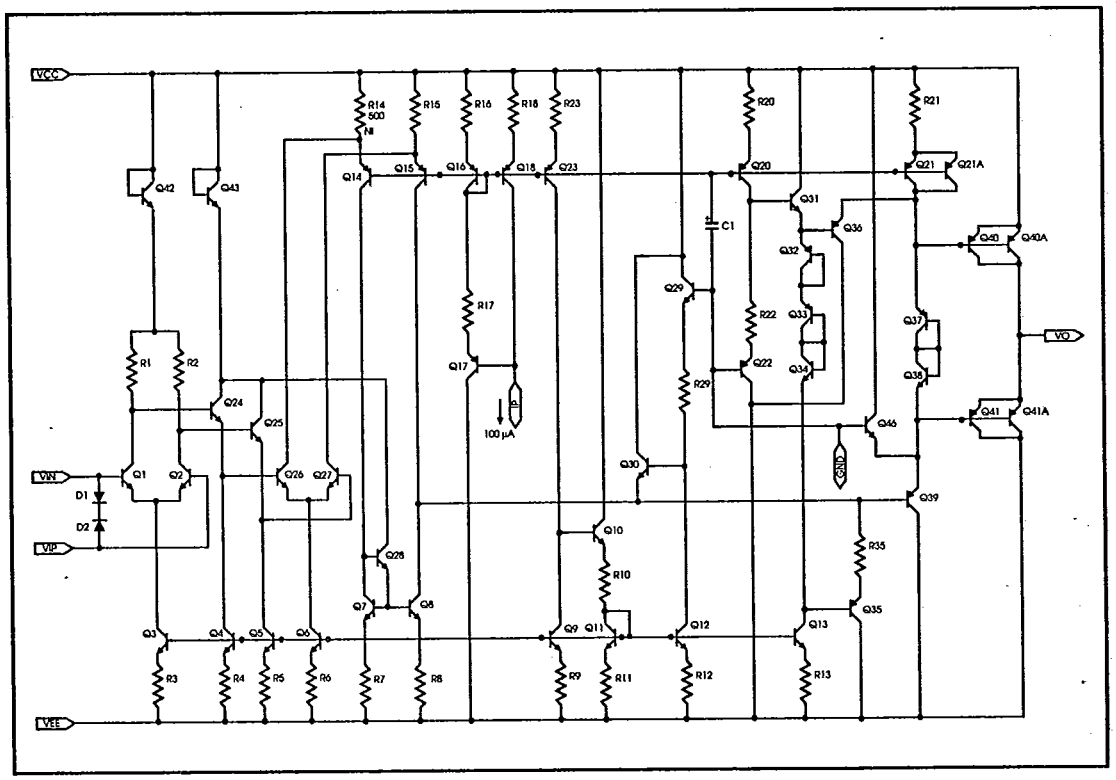
Features

- Split-Supply Operation
- TTL Output Levels
- High Output Drive Current — 30mA
- 29ns Response Time
- High Gain — 90dB
- Fits in 1.5 Tile
- Design/Layout Available in NiCr



Description

The **CMP2** is a TTL-output comparator that operates from split supply voltages. It is a precision comparator that features high gain, low offset and drift. The output stage is non-saturating, and is designed to clamp at typical TTL levels. Other clamp levels can be choosen, including bipolar levels, depending on the supply voltages.



SP2000 Series Analog Array MacroCell
Split-Supply TTL Comparator — CMP2

Specifications

All specifications at T_A=25°C, V_{CC} = +15V, V_{EE} = -15V, Ip=100µA

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Characteristics						
Input Offset Voltage	V_{OS}		1.6	5	mV	
Input Bias Current	I_B		125	300	nA	
Input Ofset Curent	I_{OS}		10	50	nA	
Common Mode Voltage	V_{CM}			V_{CC}-1.5	V	
Transfer Characteristics						
Voltage Gain	A_{OL}		91		dB	
Output Characteristics						
Output Current						
Source	$-I_{OUT}$		30		mA	
Sink	$+I_{OUT}$		30		mA	
Output Low Voltage	V_{OL}		65	300	mV	I_{OL}=1mA
			0.27	0.5	V	I_{OL}=40mA; Note 1
Output High Voltage	V_{OH}		3.28	2.8	V	I_{OH}=-1mA
			3.11	2.8	V	I_{OH}=-30mA; Note 1
Capacitive Load	C_P			50	pF	
Transient Response						
Rise/Fall Time	$T_r T_f$		25		ns	Overdrive = 50mV, C_L=50pF
Settling Time	T_s		125		ns	Overdrive = 50mV, C_L=50pF; to 0.01%
Propagation Delay	T_{pd}		29		ns	Overdrive = 50mV, C_L=50pF
Overshoot	OS		13		%	Overdrive = 50mV, C_L=50pF
Power Supply						
Supply Voltage Range	V_{SUPPLY}	10		30	V	V_{CC}-V_{EE}
Supply Current	I_{CC}		2.0		mA	I_{PT}=100µA, V_O=H
			3.0		mA	I_{PT}=100µA, V_O=L
			1.9		mA	I_{PT}=100µA, V_O=H, V_{CC}=±5V
			2.7		mA	I_{PT}=100µA, V_O=L, V_{CC}=±5V

Notes:
1) If V_{CC}-V_{EE}=10V, then I_{OL} and I_{OH} for V_{OL} and V_{OH} are +15mA and 10mA respectively.

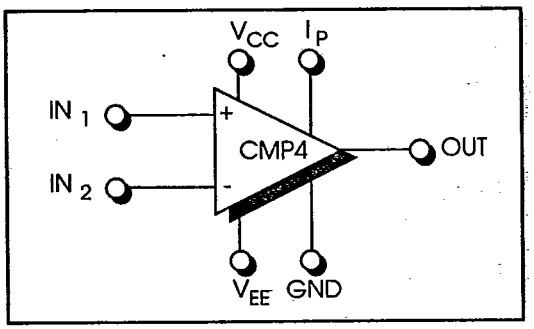
T-42-21

SIGNAL PROCESSING EXCELLENCE

SP2000 Series Analog Array MacroCell
Two-Input Window Comparator — CMP4

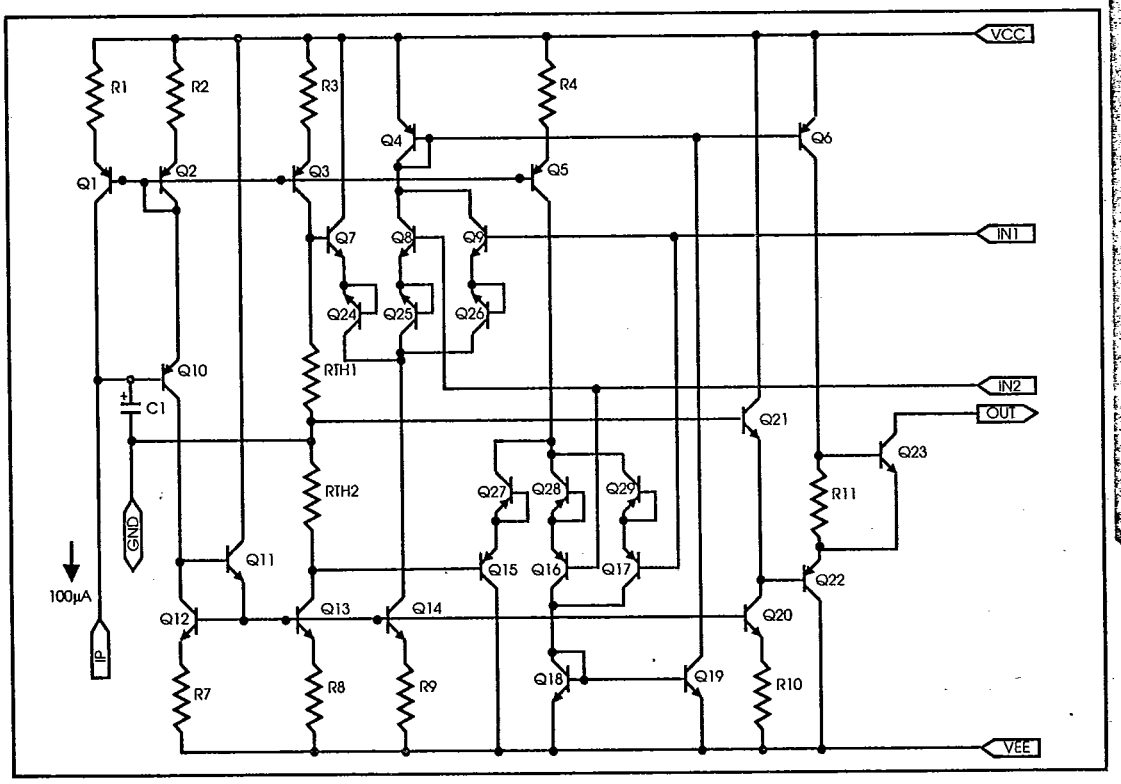
Features

- Open–Collector Output
- High Impedance Inputs
- Arbitrarily Set Thresholds Equal to 0.2mA (RTH)
- Fits in 1 Tile
- Design/Layout Available in NiCr



Description

The **CMP4** is a two-input window comparator with high impedance inputs and a TTL-level, open-collector output. The output will be active (pull-down) when either input exceeds the internal thresholds set by RTH_1 and RTH_2. RTH_1 sets the positive threshold voltage, and RTH_2 sets the negative threshold voltage. In a typical application, IN_1 or IN_2 would be connected to a point to be monitored in a system. A digital flag would then be set (output low) by the comparator when that signal point exceeded the plus or minus threshold voltage.



SP2000 Series Analog Array MacroCell
Two-Input Window Comparator — CMP4

T-42-21

Specifications

All specifications at T_A=25°C, V_{CC} = +15V, V_{EE} = -15V, Ip=100µA

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Characteristics						
Input Offset Voltage	V_{OS}		5	10	mV	Relative to V_{TH}, Note1
Input Bias Current	I_B		0.1	10	µA	IN_1 and $IN_2 < V_{TH}$
			0.5	5	µA	IN_1 and $IN_2 > V_{TH}$
Common Mode Range	CMR	V_{EE}+1		V_{CC}-1	V	
Transfer Characteristics						
Voltage Gain	A_V		44		dB	R_L=10KΩ to 5V (pull up)
Overdrive	V_{OD}		0.15		V	Note 2
Output Characteristics						
Output Current						
Sink	$+I_{OUT}$		5		mA	
Output Low Voltage	V_{OL}		0.5	0.7	V	
Output High Voltage	V_{OH}		V_{CC}		V	R_L to V_{CC}
Transient Response						
Response Time	T_{pd}		30		ns	High to low output, R_L=10KΩ to 5V
			1		µs	Low to high output
Power Supply						
Supply Voltage Range	V_{SUPPLY}	8		30	V	V_{CC}-V_{EE}
Supply Current	I_{CC}		0.5		mA	Output high

Notes:
1) V_{TH} = Threshold Voltage (absolute value) = (0.2mA)($RTH_{1,2}$)
2) V_{OD} = Input voltage overdrive required to switch output from V_{TH}.

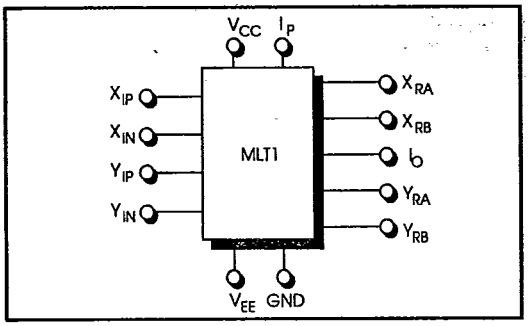
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP2000 Series Analog Array MacroCell Multiplier — MLT1

T-42-21

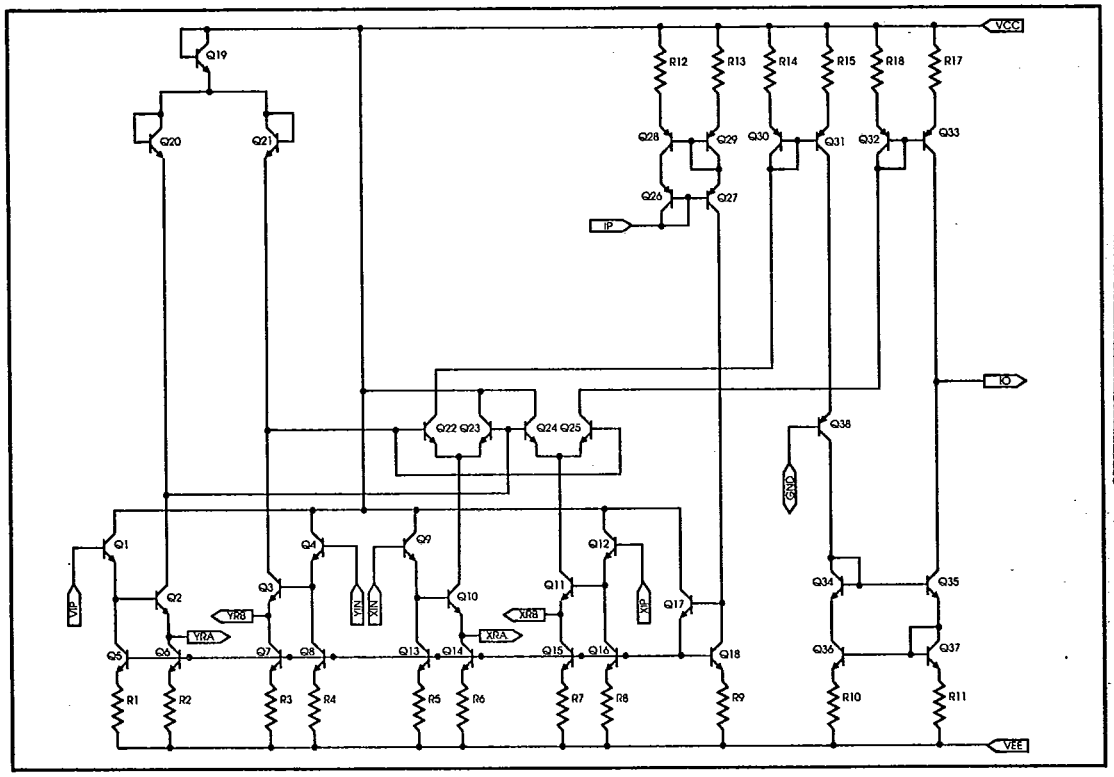
Features

- Voltage-Controlled Amplifier Operation
- Bipolar Output
- I_o = VX/RX(1+VY/(IB*RY))
- 100MHz Bandwidth with 50Ω Load
- 0.02% THD
- 1.6mA Supply Current
- Fits in 2 Tile
- Design/Layout Available in NiCr



Description

The **MLT1** is a Gilbert Cell multiplier configured as a voltage-controlled amplifier. The output stage contains differential conversion and level-shifting to a bipolar current output. Typically, an input signal is applied to the VX inputs. A DC control voltage applied to the VY input would control the gain or attenuation of the VX signal. The inputs to either VX or VY can be bipolar. The output is a sum of the inverting and non-inverting currents (bipolar output) with near rail-to-rail compliance. The output current can be converted to a voltage through a resistor connected to ground, or with an I-to-V converter (transimpedance) amplifier.



SP2000 Series Analog Array MacroCell Multiplier — MLT1

T-42-21

Specifications

All specifications at T_A=25°C, V_{CC} = +15V, V_{EE} = -15V, Ip=100µA

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Characteristics						
Offset Voltage	V_{OS}		2	7	mV	
Offset Current	I_{OS}		10		nA	V_X or V_Y inputs
Input Bias Current	I_B		100		nA	V_X or V_Y inputs
Common Mode Range	CMR	V_{EE}+3		V_{CC}-2	V	Note 2
Input Resistance	R_{IN}		200		MΩ	$R_X = R_Y$ = 10KΩ
Transfer Characteristics						
Reference Current	I_R		250		µA	Note 1
Scale Factor						$I_O = V_Y/R_X (1+(V_Y/(I_R{*}R_Y))$
Distortion	THD		0.02		%	$R_X = R_Y = R_L$ = 10KΩ, F = 10kHz
Output Characteristics						
Offset Current	I_{OS}		2.5		µA	At I_O
Transient Response						
Bandwidth	BW		20		MHz	$R_X = R_Y = R_L$ =10KΩ
			100		MHz	R_L = 50Ω
Power Supply						
Supply Voltage Range	V_{SUPPLY}	8		30	V	V_{CC}-V_{EE}
Supply Current	I_{CC}		1.6		mA	

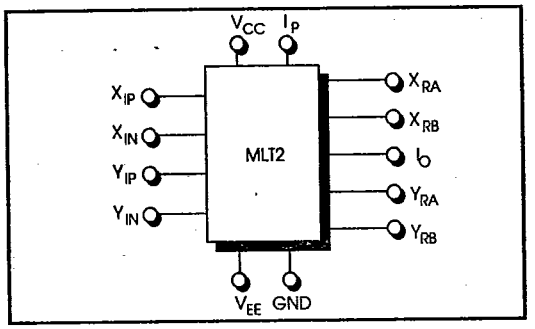
Notes:
1) The reference current I_R, can be scaled linearly with I_P.
2) Maximum input voltage, ($V_{(XIP-XIN)}$, $V_{(YIP-YIN)}$ is equal to (R_X,R_Y)(I_B)

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP2000 Series Analog Array MacroCell
Current Output, 4-Quadrant Multiplier — MLT2

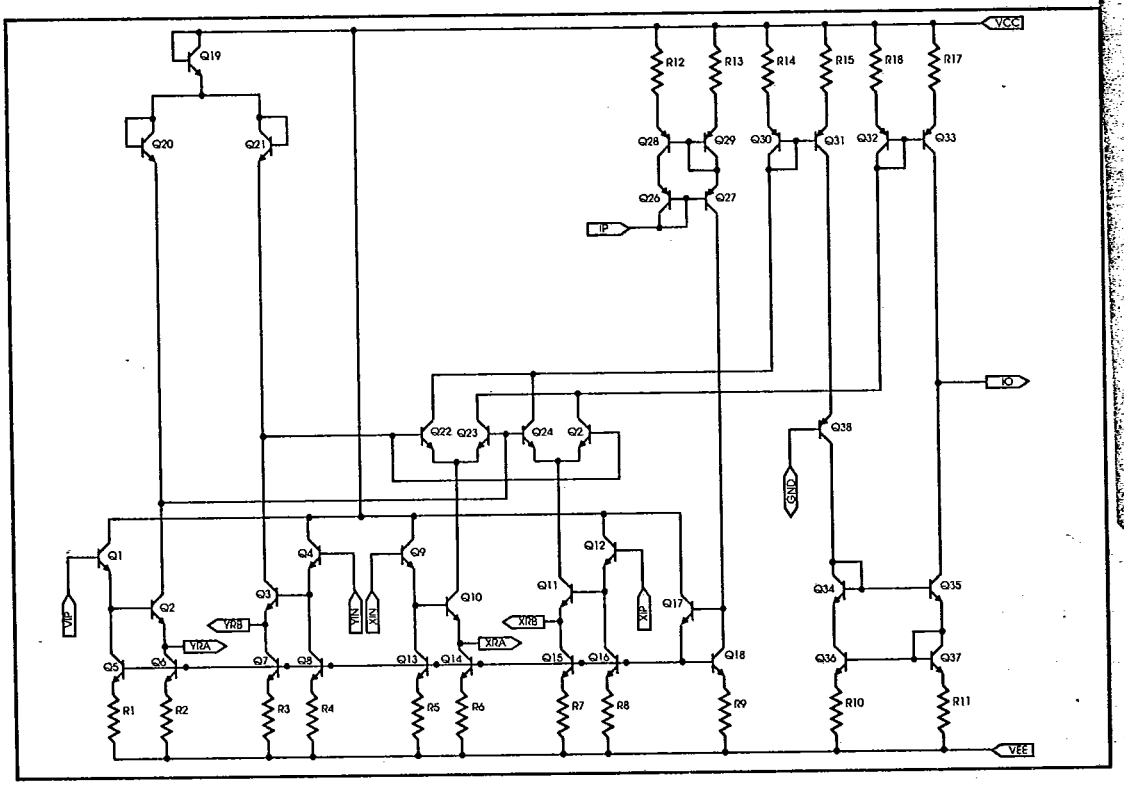
Features

- 4-Quadrant Multiplier
- Bipolar Current Output
- $I_o = K(V_X)(V_Y)$
- 100MHz Bandwidth with 50Ω Load
- Thin-Film Resistors for Temperature Stability and Very Low Voltage Coefficients
- 1.6mA Supply Current
- Fits in 2 Tiles
- Design/Layout Available in NiCr



Description

The **MLT1** is a 4-quadrant Gilbert Cell type multiplier, with a bipolar current output stage. Internal level-shifting circuits eliminate the need for a differential-to-single-ended stage following the multiplier. This simplifies the complete multiplier implementation. The output current can be converted to a voltage by a load resistor, or fed directly into an integrator, depending on the application.



SP2000 Series Analog Array MacroCell
Current Output, 4-Quadrant Multiplier — MLT2

T-42-21

Specifications

All specifications at T_A=25°C, V_{CC} = +15V, V_{EE} = -15V, Ip=100µA

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Characteristics						
Offset Voltage	V_{OS}		2	7	mV	
Offset Current	I_{OS}		10		nA	V_X or V_Y Inputs
Input Bias Current	I_B		100		nA	V_X or V_Y Inputs
Common Mode Range	CMR	V_{EE}+3		V_{CC}-2	V	Note 2
Input Resistance	R_{IN}		200		MΩ	$R_X = R_Y$ = 10KΩ
Transfer Characteristics						
Reference Current	I_R		250		µA	Note 1
Scale Factor	K					K= $R_L/(R_X R_Y I_B)$
Distortion	THD		0.02		%	$R_X = R_Y = R_L$ = 10KΩ, F = 10kHz
Output Characteristics						
Offset Current	I_{OS}		2.5		µA	At I_O
Transient Response						
Bandwidth	BW		20		MHz	$R_X = R_Y = R_L$ =10KΩ
			100		MHz	R_L = 50Ω
Power Supply						
Supply Voltage Range	V_{SUPPLY}	8		30	V	V_{CC}-V_{EE}
Supply Current	I_{CC}		1.6		mA	

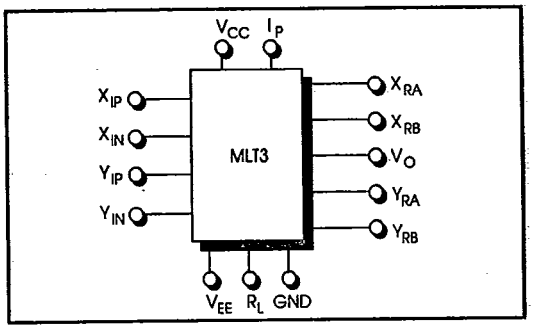
Notes:
1) The reference current I_R, can be scaled linearly with I_P.
2) Maximum input voltage, ($V_{(XIP-XIN)}$, $V_{(YIP-YIN)}$ is equal to (R_X,R_Y)(I_B)
3) Transfer function: I_O=K($V_X$$V_Y$), where K = scale factor as above.

T-42-21

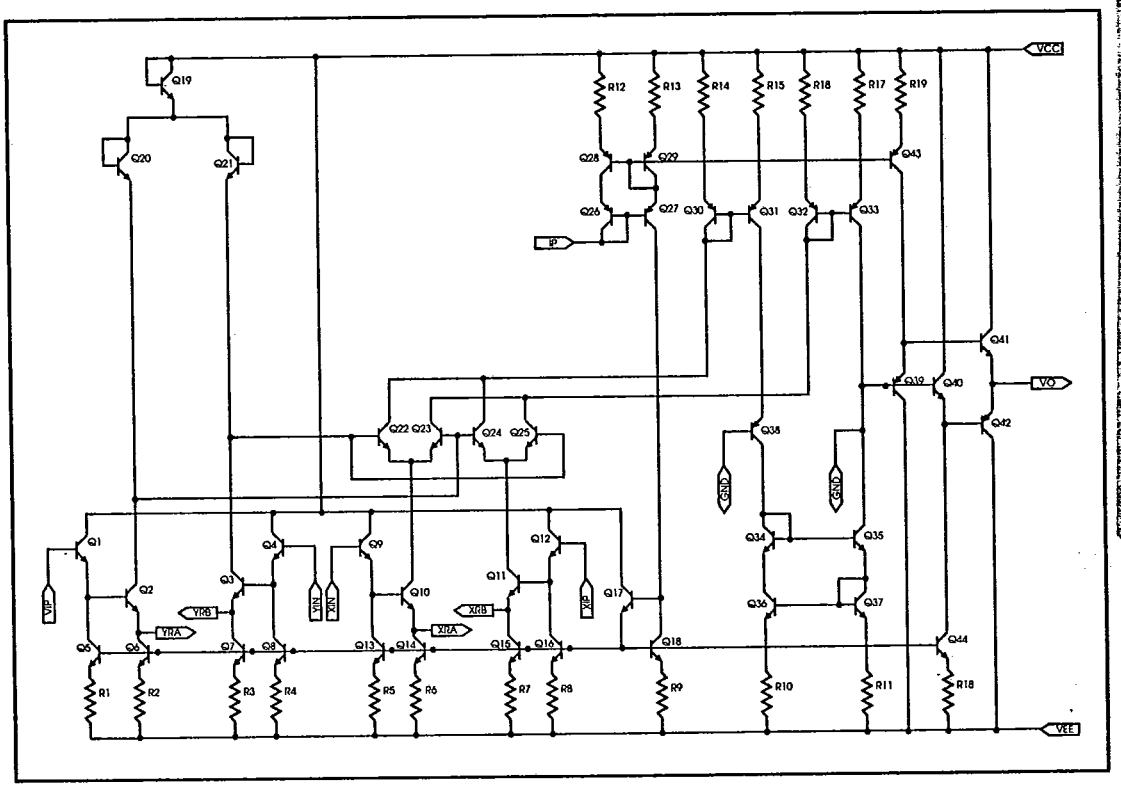
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP2000 Series Analog Array MacroCell
Voltage Output, 4-Quadrant Multiplier — MLT3

Features
- 4-Quadrant Multiplier
- Voltage Output
- $V_O = K(R_L)(V_X)(V_Y)$
- 100MHz Bandwidth with 50Ω Load
- Thin-Film Resistors for Temperature Stability and Very Low Voltage Coefficients
- 2mA Supply Current
- Fits in 2 Tiles
- Design/Layout Available in NiCr



Description
The **MLT3** is a 4-quadrant Gilbert Cell type multiplier, similar to the **MLT2** multiplier, except that a unity-gain buffer has been added to the output stage. All differential conversion and level-shifting is done internally. A resistor is required at R_L to set the I-to-V conversion.



T-42-21

SP2000 Series Analog Array MacroCell
Voltage Output, 4-Quadrant Multiplier — MLT3

Specifications

All specifications at T_A=25°C, V_{CC} = +15V, V_{EE} = -15V, Ip=100µA

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Characteristics						
Offset Voltage	V_{OS}		2	7	mV	
Offset Current	I_{OS}		10		nA	V_X or V_Y Inputs
Input Bias Current	I_B		100		nA	V_X or V_Y Inputs
Common Mode Range	CMR	V_{EE}+3		V_{CC}-2	V	Note 2
Input Resistance	R_{IN}		200		MΩ	$R_X = R_Y$ = 10KΩ
Transfer Characteristics						
Reference Current	I_R		250		µA	Note 1
Scale Factor	K					K= $R_L/(R_X R_Y I_B)$
Distortion	THD		0.02		%	$R_X = R_Y = R_L$ = 10KΩ, F = 10kHz
Output Characteristics						
Offset Voltage	V_{OS}		25		mV	R_L = 10KΩ
Transient Response						
Bandwidth	BW		20		MHz	$R_X = R_Y = R_L$ =10KΩ
			100		MHz	R_L = 50Ω
Power Supply						
Supply Voltage Range	V_{SUPPLY}	8		30	V	V_{CC}-V_{EE}
Supply Current	I_{CC}		2		mA	I_P=100µA

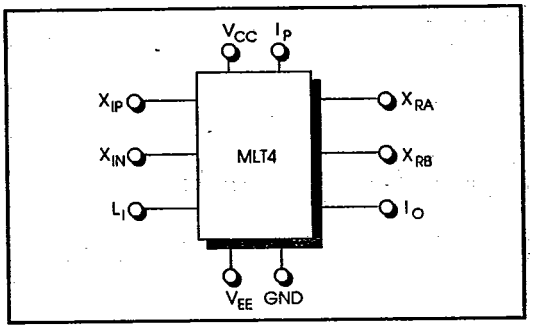
Notes:
1) The reference current I_R, can be scaled linearly with I_P.
2) Maximum input voltage, ($V_{(XIP-XIN)}$, $V_{(YIP-YIN)}$ is equal to (R_X,R_Y)(I_B)
3) Transfer function: V_O=K($V_X V_Y$), where K = scale factor as above.

T-42-21

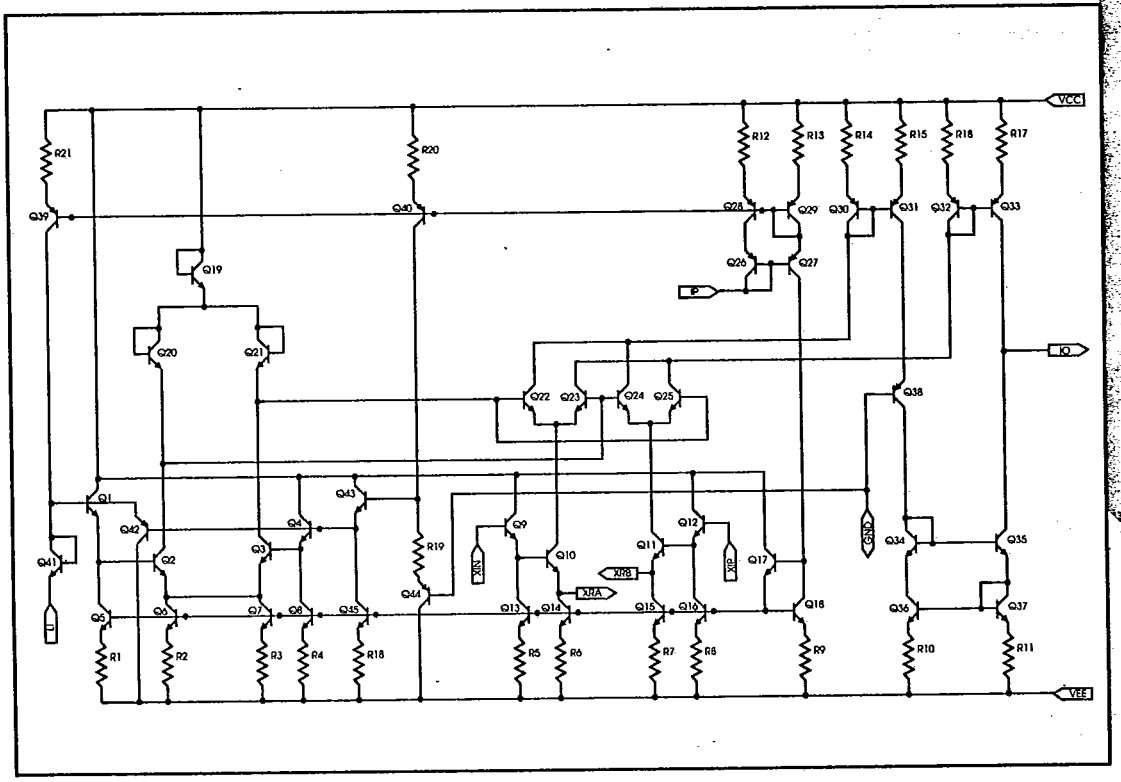
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP2000 Series Analog Array MacroCell
Current Output, TTL Input, 4-Quadrant Multiplier — MLT4

Features
- 4-Quadrant Multiplier
- Bipolar Current Output
- Y Input Accepts TTL Logic Levels
- 100MHz Bandwidth with 50Ω Load
- Thin-Film Resistors for Temperature Stability and Very Low Voltage Coefficients
- 2mA Supply Current
- Fits in 2 Tiles
- Design/Layout Available in NiCr



Description
The **MLT4** is a 4-quadrant Gilbert Cell type multiplier, similar in several respects to the **MLT1** and **MLT2** multipliers. Like the **MLT1** and **MLT2**, the **MLT4** has a bipolar current output stage, and the X input stage is the same. However, the Y input stage has been configured to accept a ground-referenced TTL logic signal. The **MLT4** therefore will, for example, multiply a linear signal by a digital clock for demodulation. Like the other **SP2000 Series** multipliers, the **MLT4** also has internal level-shifting and differential conversion to simplify its application.



SP2000 Series Analog Array MacroCell
Current Output, TTL Input, 4-Quadrant Multiplier — MLT4

T-42-21

Specifications

All specifications at T_A=25°C, V_{CC} = +15V, V_{EE} = -15V, Ip=100µA

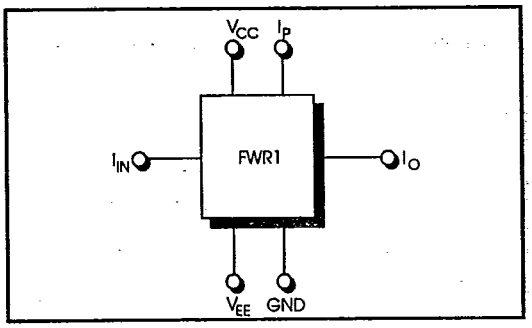
Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Characteristics						
Bias Current	I_B		100		nA	V_X inputs
Input High Current	I_{IH}		1	10	µA	I_I=5V
Input Low Current	I_{IL}		50	100	µA	I_I=0V
Logic High	V_{IH}	2.8		7	V	
Logic Low	V_{IL}	0		0.8	V	
Common Mode Range	CMR				V	Note 2
Transfer Characteristics						
Reference Current	I_R		250		µA	Note 1
Output Characteristics						
Offset Current	I_{OS}		2.5		µA	At I_O, DC average
Transient Response						
Bandwidth	BW		20		MHz	$R_X = R_Y = R_L$ =10KΩ
			100		MHz	R_L = 50Ω
Power Supply						
Supply Voltage Range	V_{SUPPLY}	8		30	V	V_{CC}-V_{EE}
Supply Current	I_{CC}		2		mA	

Notes:
1) The reference current I_R, can be scaled linearly with I_P.
2) Maximum Input voltage, $V_{(XIP-XIN)} = R_X I_B$.

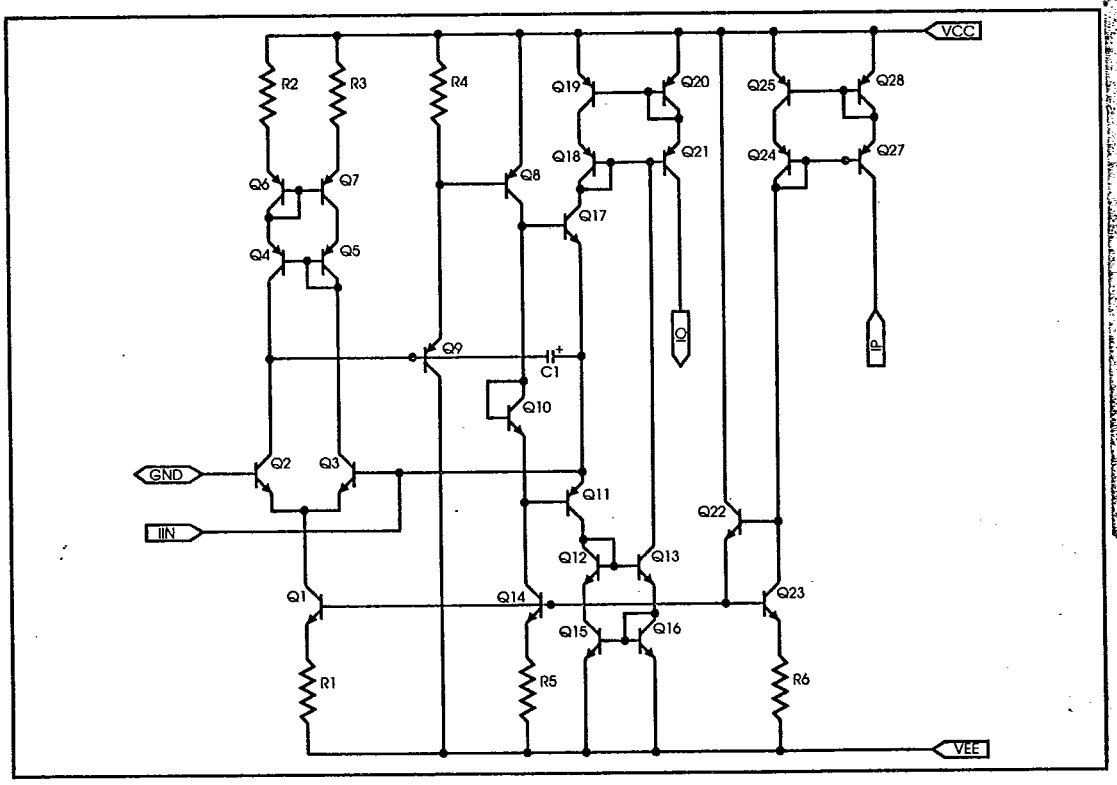
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP2000 Series Analog Array MacroCell
Current Source Output, Full-Wave Rectifier — FWR1

Features
- Precision Full-Wave Rectification
- Current Source Operation
- 0.5mA Supply Current
- Fits in 1 Tile
- Design/Layout Available in NiCr



Description
The **FWR1** is a precision full-wave rectifier. The I_{IN} input is a virtual ground. An external resistor connected to I_{IN} converts the input voltage to a current. The rectified input current is available at the output, I_O, which is a current source for both halves of the input waveform.



SP2000 Series Analog Array MacroCell
Current Source Output, Full-Wave Rectifier — FWR1

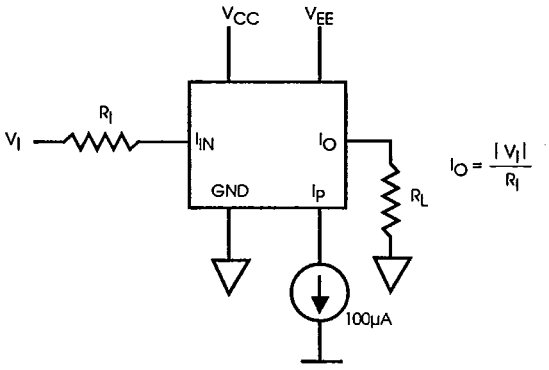
T-42-21

Specifications

All specifications at T_A=25°C, V_{CC} = +15V, V_{EE} = -15V, Ip=100µA

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Characteristics						
Bias Current	I_B		200	500	nA	
Offset Voltage	V_{OS}		1	5	mV	$R_I = R_L$ = 10KΩ
Output Characteristics						
Current Range	I_O	0		2.0	mA	
Voltage Range	V_O	V_{EE}		V_{CC}-1.5	V	Voltage compliance
Transient Response						
Small Signal Bandwidth	BW		10		MHz	R_L =1KΩ
Slew Rate	S_r		3		V/µs	R_L = 1KΩ
Power Supply						
Supply Voltage Range	V_{SUPPLY}	8		30	V	V_{CC}-V_{EE}
Supply Current	I_{CC}		0.5		mA	I_{IN}=0V

Typical Application:

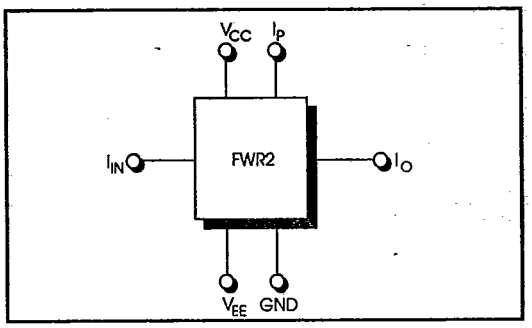


T-42-21

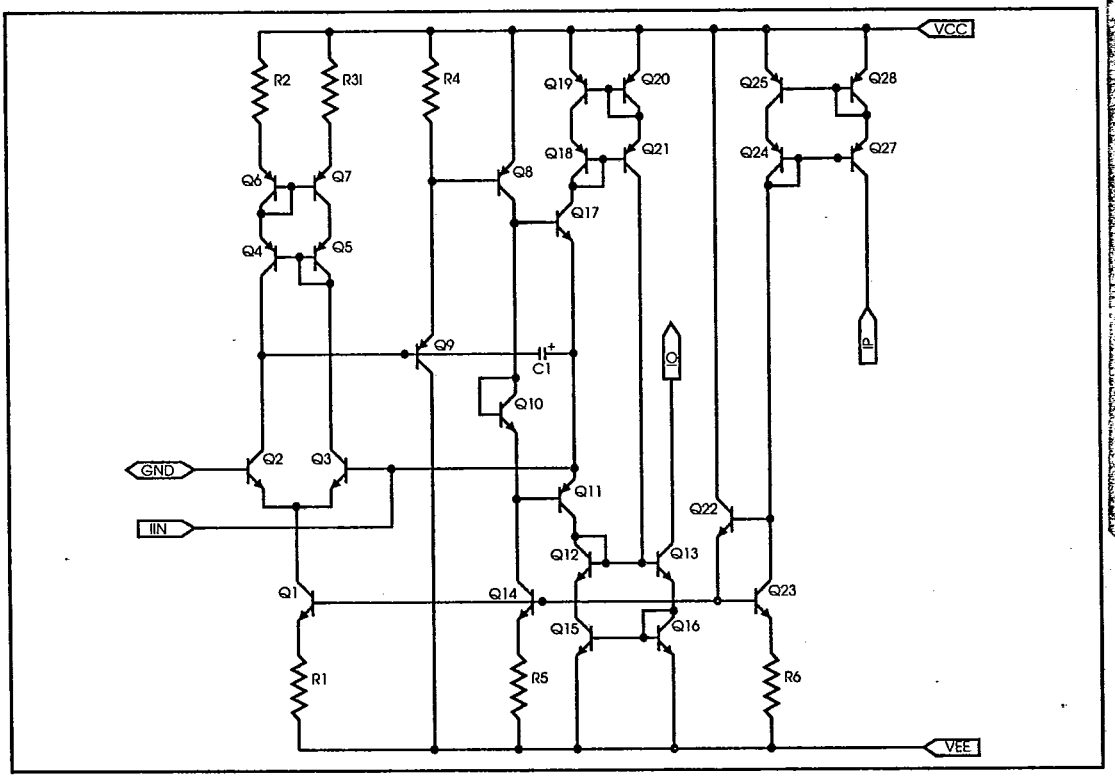
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP2000 Series Analog Array MacroCell
Current Sink Output, Full Wave Rectifier — FWR2

Features
- Precision Full Wave Rectification
- Current Sink Operation
- 0.5mA Supply Current
- Fits in 1 Tile
- Design/Layout Available in NiCr



Description
The **FWR2** is a precision full-wave rectifier. The I_{IN} input is a virtual ground. An external resistor connected to I_{IN} converts the input voltage to a current. The rectified input current is available at the output, I_O, which is a current sink for both halves of the input waveform.



T-42-21

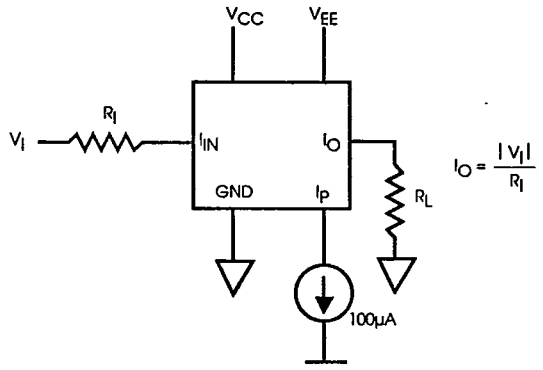
SP2000 Series Analog Array MacroCell
Current Sink Output, Full-Wave Rectifier — FWR2

Specifications

All specifications at T_A=25°C, V_{CC} = +15V, V_{EE} = -15V, Ip=100µA

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Characteristics						
Bias Current	I_B		200	500	nA	
Offset Voltage	V_{OS}		1	5	mV	$R_I = R_L$ = 10KΩ
Output Characteristics						
Current Range	I_O	-2.0		0	mA	
Voltage Range	V_O	V_{EE}+1.5		V_{CC}	V	Voltage compliance
Transient Response						
Small Signal Bandwidth	BW		10		MHz	R_L =1KΩ
Slew Rate	S_r		3		V/µs	R_L = 1KΩ
Power Supply						
Supply Voltage Range	V_{SUPPLY}	8		30	V	V_{CC}-V_{EE}
Supply Current	I_{CC}		0.5		mA	I_{IN}=0V

Typical Application:



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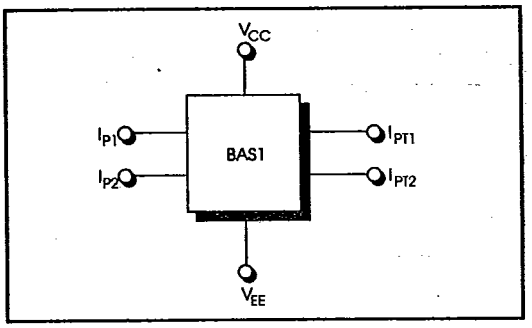
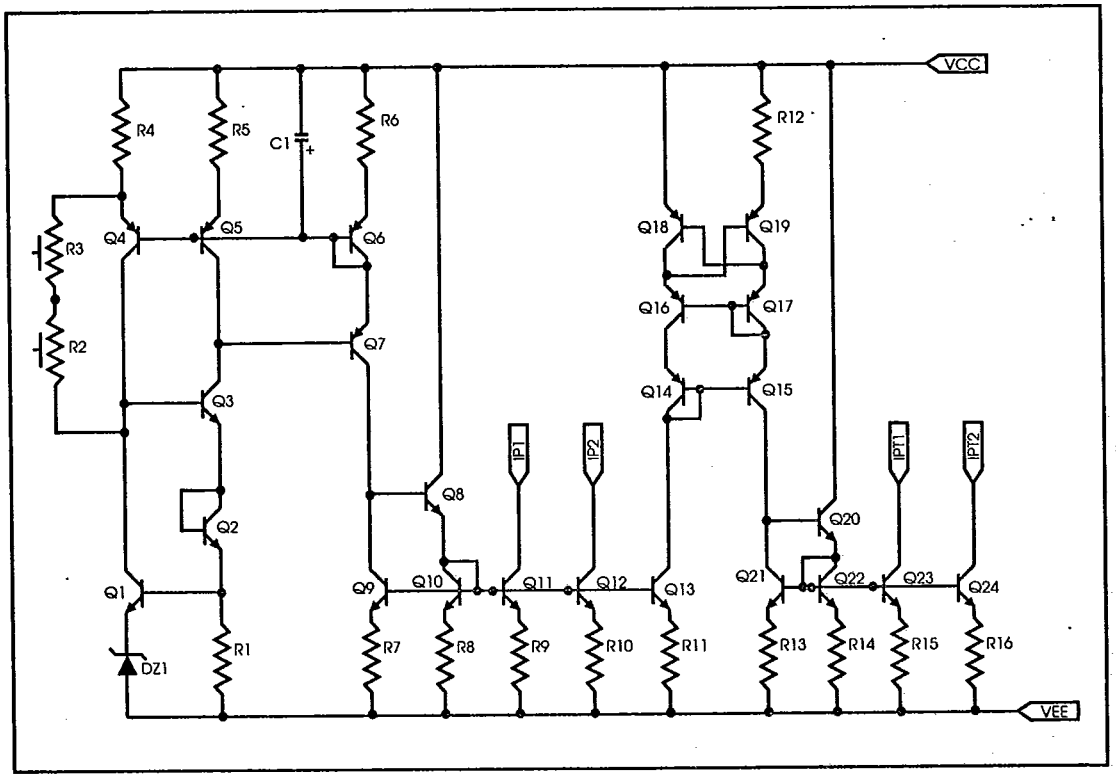
SP2000 Series Analog Array MacroCell
I_P and I_{PT} Bias Generator — BAS1

Features
- I_P (low TC) Current Sources
- I_{PT} (PTAT) Current Sources
- 1.4mA Supply Current
- Fits in 1 Tile
- Design/Layout Available in NiCr



Description
The **BAS1** cell is a biasing block that generates both I_P and I_{PT} bias currents. The I_P circuits are based on a zener voltage (divided by R) and therefore have a fairly low temperature coefficient. When an I_P current is converted to a voltage through a resistor, the absolute tolerance of thin-film sheet rho is cancelled. The I_{PT} current is developed by a PTAT (proportional to absolute temperature) current generator. This current source is usually used to bias the op-amps for optimum compensation over temperature.



SP2000 Series Analog Array MacroCell
I_P and I_{PT} Bias Generator —BAS1

T-42-21

Specifications

All specifications at T_A=25°C, V_{CC} = +15V, V_{EE} = -15V

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Characteristics						
Low TC Current	I_P	70	100	130	µA	
PTAT Current	I_{PT}	70	100	130	µA	At 25°C
			73		µA	At -55°C
			133		µA	At 125°C
Power Supply						
Supply Voltage Range	V_{SUPPLY}	10		30	V	V_{CC}-V_{EE}
Supply Current	I_{EE}		1.4		mA	$2I_P$ and $2I_{PT}$

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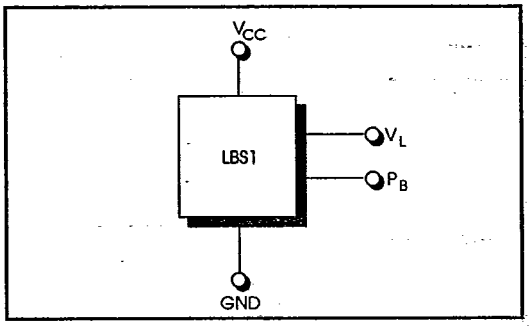
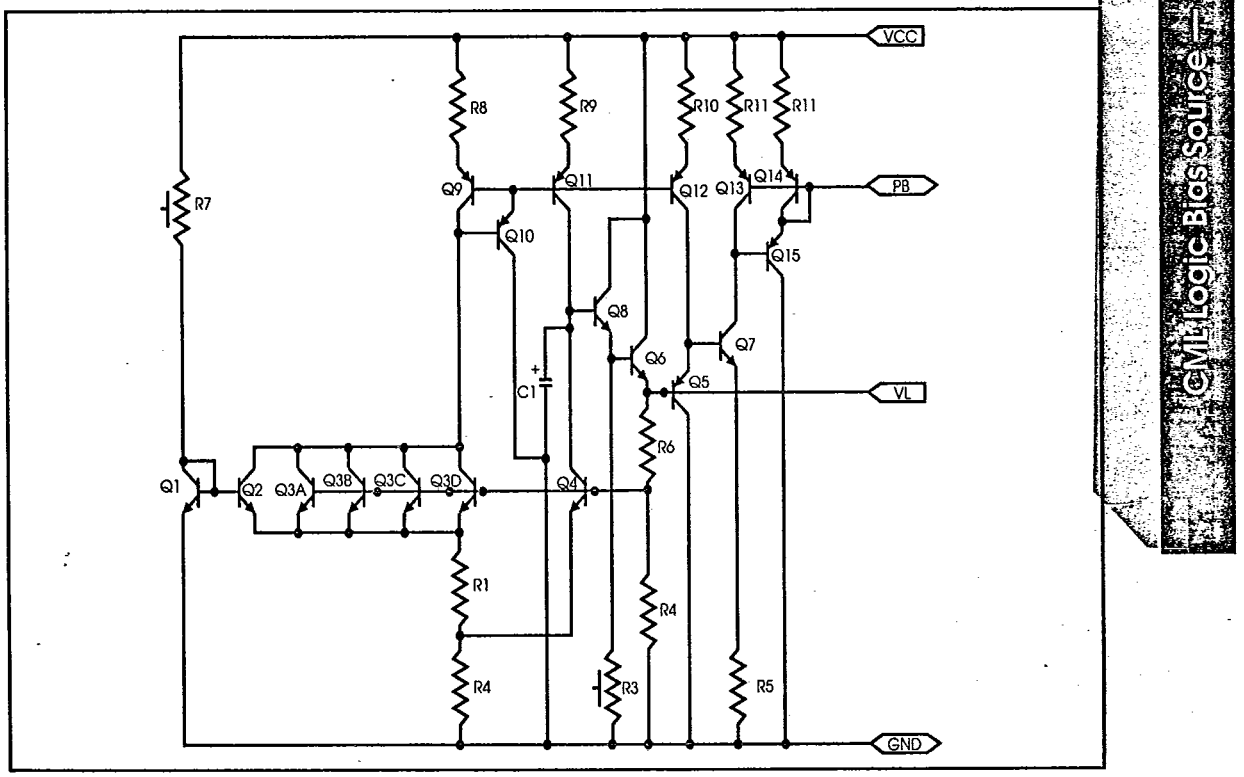
T-42-21

SP2000 Series Analog Array MacroCell
CML Logic Bias Source — LBS1

Features
- CML Logic Bias Current Source
- Band-gap Voltage Reference
- 0.5mA Supply Current
- Fits in 1 Tile
- Design/Layout Available in NiCr



Description
The **LBS1** cell is a biasing block for the CML logic family. The circuit is a band-gap voltage reference that provides the CML voltage level (1.5V). It also sets up a bias voltage for PNP current sources. The circuit can operate from a single 5V supply.



CML Logic Bias Source — LBS1

SP2000 Series Analog Array MacroCell
CML Logic Bias Source —LBS1

T-42-21

Specifications

All specifications at T_A=25°C, V_{CC} = +15V

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Characteristics						
CML Output Voltage	V_L		1.5		V	
Tempco	TC		40	100	ppm/°C	
Output Load Current	I_L			5	mA	
Power Supply						
Supply Voltage	V_{CC}	4		30	V	
Supply Current	I_{CC}		0.5		mA	

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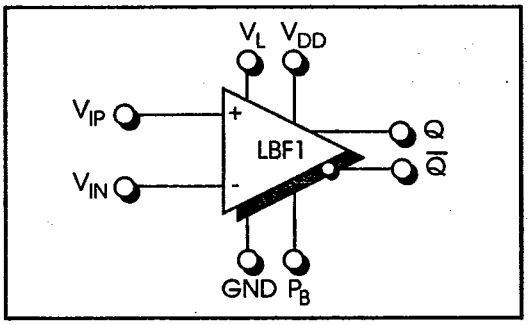
T-42-21

SP2000 Series Analog Array MacroCell
CML Logic Input Buffer —LBF1

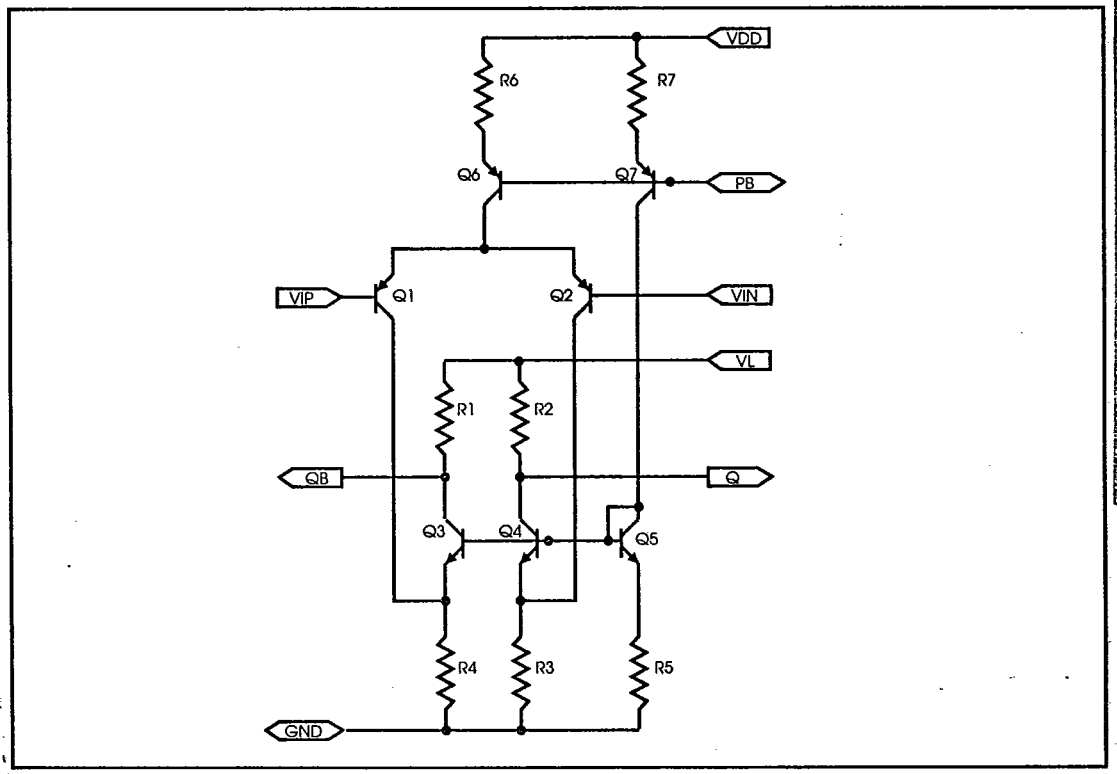
Features

- Buffered Input to CML Logic
- Differential Inputs and Outputs
- Input Common-Mode Range to Ground
- 3ns Rise Time
- 3ns Response Time
- 0.6mA Supply Current
- Fits in <1 Tile
- Design/Layout Available in NiCr



Description

The **LBF1** is an input logic buffer that has been designed to drive the CML logic gate. The **LBF1** is in essence a comparator with input common-mode range to ground. An inverted output is provided. One of the inputs is normally tied to a logic threshold (e.g. 1.4V for TTL). Biasing for the **LBF1** is provided by the logic bias block **LBS1**. The **LBF1** can also be used for general-purpose comparator/level-shifting operations.



T-42-21

SP2000 Series Analog Array MacroCell
CML Logic Input Buffer — LBF1

Specifications

All specifications at T_A=25°C, V_{CC} = +15V

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Characteristics						
Common Mode Range	CMR	0		V_{CC}-2	V	V_{IP}, V_{IN}
CML Logic Voltage	V_L		1.5		V	
Output Characteristics						
CML Output Low			1.25		V	Q or $\overline{Q}$
CML Output High			1.5		V	Q or $\overline{Q}$
Transient Response						
Rise Time	T_r		3		ns	
Response Time	T_d		3		ns	
Power Supply						
Supply Voltage	V_{CC}	4		30	V	
Supply Current	I_{CC}		0.6		mA	

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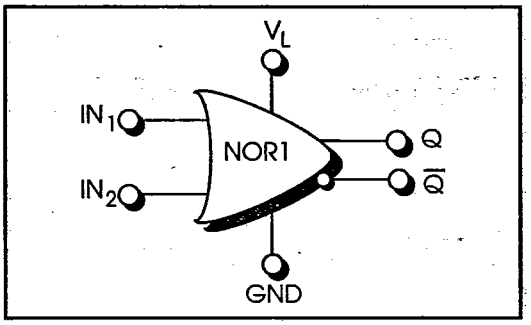
SIGNAL PROCESSING EXCELLENCE

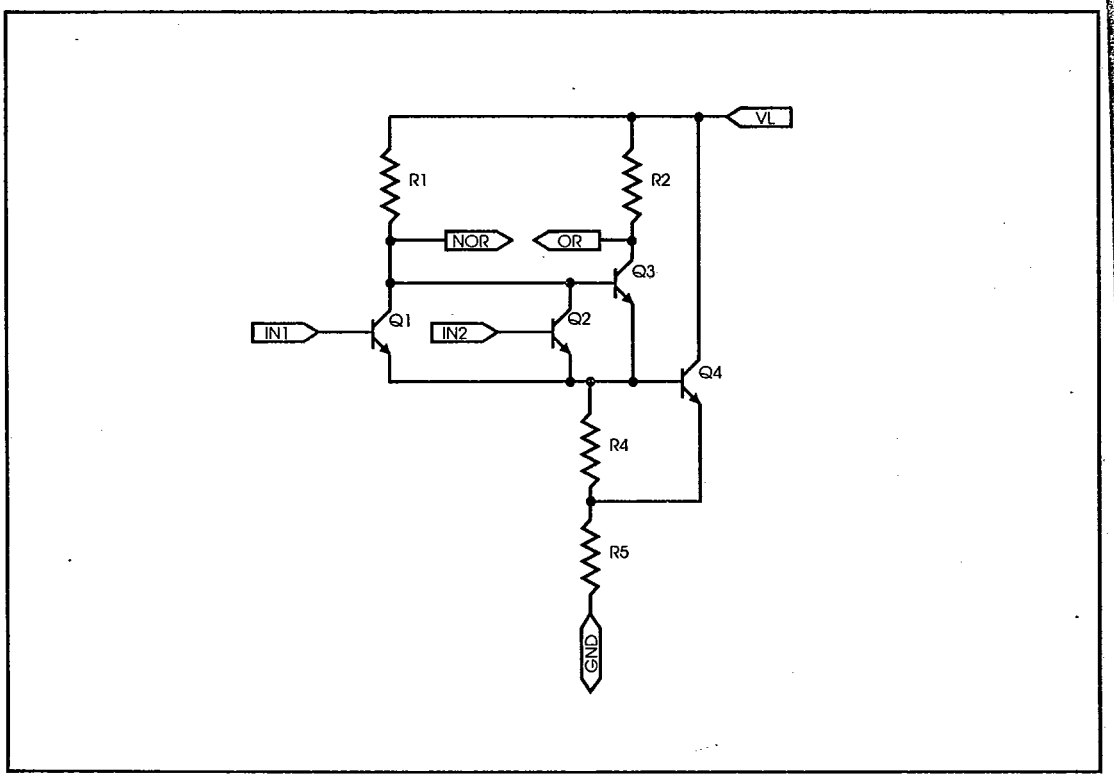
T-42-21

SP2000 Series Analog Array MacroCell
NOR Gate — NOR1

Features
- Two Input OR/NOR Function
- Built-in Hysteresis
- High Noise Immunity
- 5ns Rise Time
- 7ns Response Time
- 300μA Supply Current
- Fits in <0.5 Tile
- Design/Layout Available in NiCr



Description
The **NOR1** is a two-input OR/NOR logic gate. The logic topology is essentially that of current-mode logic (CML), similar to ECL. This CML logic design has built-in hysteresis. The logic swing is 250mV, referenced to a 1.5V supply rail. The built-in hysteresis gives the gate high noise immunity, even with the small voltage swing. The V_{OH} is 1.5V and the V_{OL} is 1.25V. These levels and their differential nature are well-suited for directly driving other analog macrocells such as comparators, multipliers and switched amplifiers.



SP2000 Series Analog Array MacroCell
NOR Gate —NOR1

T-42-21

Specifications

All specifications at T_A=25°C, V_L = 1.5V; 20V process

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Characteristics						
Input Logic Low	V_{IL}		1.25		V	
Input Logic High	V_{IH}		1.5		V	
Bias Current Low	I_{IL}		0.1		µA	
Bias Current High	I_{IH}		2	5	µA	
Output Characteristics						
Output Logic Low	V_{OL}		1.25		V	
Output Logic High	V_{OH}		1.5		V	
Transient Response						
Rise Time	T_r		5		ns	
Response Time	T_d		7		ns	25°C
			15		ns	125°C
Power Supply						
Supply Voltage	V_L		1.5		V	
Supply Current	I_{CC}		300		µA	

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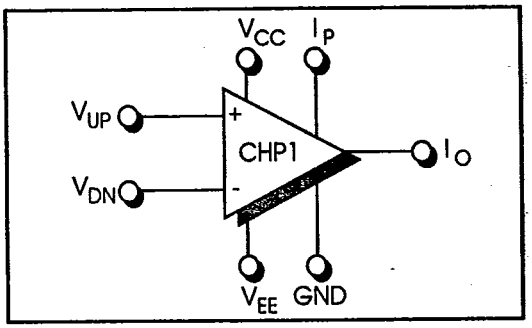
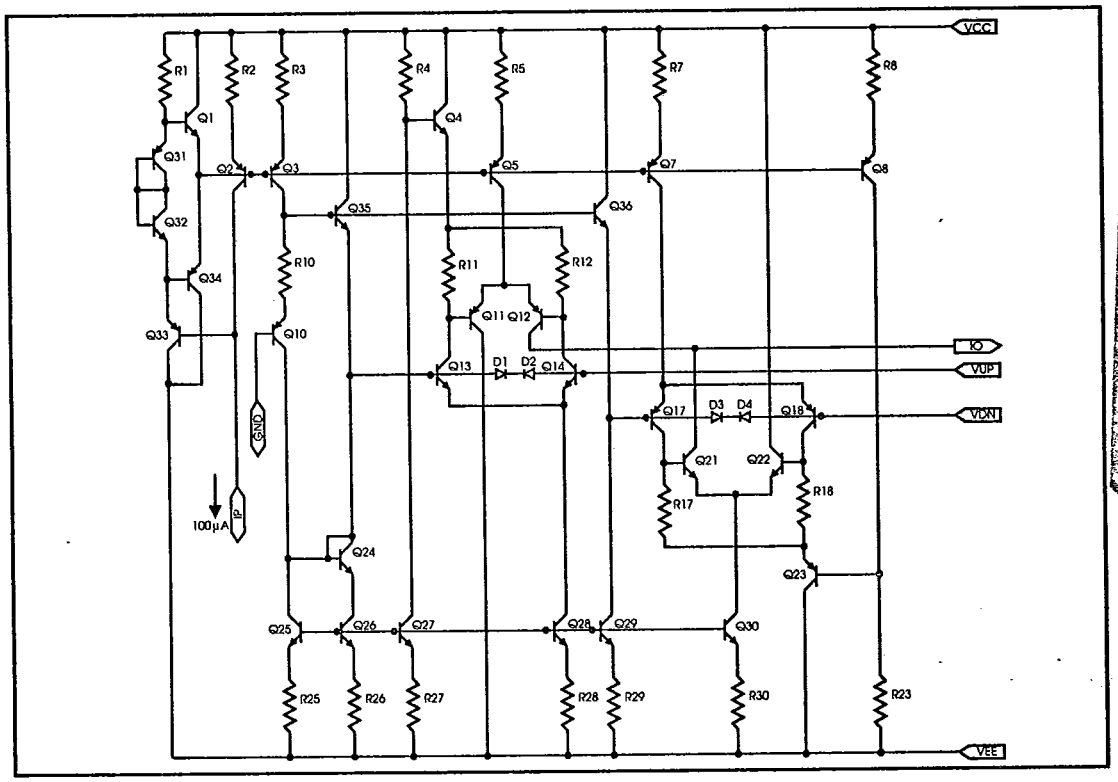
T-42-21

SP2000 Series Analog Array MacroCell
Charge Pump — CHP1

Features
- TTL Input Logic
- Bipolar Output Current (Sink/Source)
- 5ns Response Time
- 2.1mA Supply Current
- Fits in 1.5 Tiles
- Design/Layout Available in NiCr



Description
The **CHP1** is a precision charge pump that delivers fixed, bipolar output currents. The inputs accept TTL logic levels and are active high. The V_{UP} input will cause the output to source current into a load, whereas the V_{DN} input causes the output to sink current. When both inputs are low, the currents will be off; when both inputs are high, the source and sink currents will be balanced. The output current will have same tolerance and TC as the I_p bias current. The **CHP1** fits within 1.5 tiles.



SP2000 Series Analog Array MacroCell Charge Pump — CHP1

T-42-21

Specifications

All specifications at T_A=25°C, V_{CC} = +15V, V_{EE} = -15V

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Characteristics						
Input High Current	I_{IH}		0	-0.5	µA	V_{IH} = 5V
Input Low Current	I_{IL}		1.5	5	µA	V_{IL} = 0V
Threshold Voltage	V_{TH}		1.4		V	
Output Characteristics						
Output Current	I_{OUT}	175	200	225	µA	V_{UP} = H, V_{DN} = L
		-225	-200	-175	µA	V_{UP} = L, V_{DN} = H
			±7	±25	µA	Both = H or both = L
Output Voltage Range			±13	±13.6	V	V_{CC} = ±15V
			±3	±3.6	V	V_{CC} = ±5V; Note 1
Transient Response						
Rise Time	T_r		5	30	ns	R_L =1KΩ, C_L = 1pF (from 50% input to 50% output)
Fall Time	T_f		5	30	ns	R_L =1KΩ, C_L = 1pF (from 90% to 10%)
Propagation Delay	T_d		5	30	ns	R_L =1KΩ, C_L = 1pF (from 50% input to 50% output)
Power Supply						
Supply Voltage Range		10		30	V	V_{CC} - V_{EE}
Supply Current	I_{CC}		2.1		mA	I_p = 100µA

Note:
1) For V_{CC} = ±15V, R30 should be 880Ω for better matching of source and sink current.

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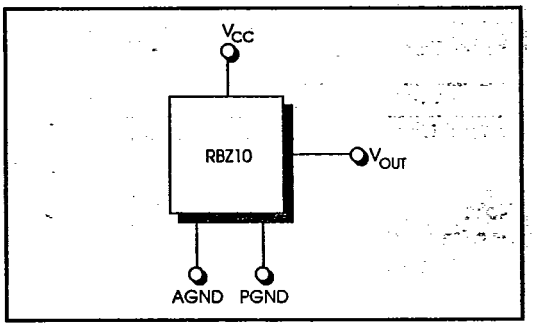
SP2000 Series Analog Array MacroCell
Buried-Zener Reference — RBZ10

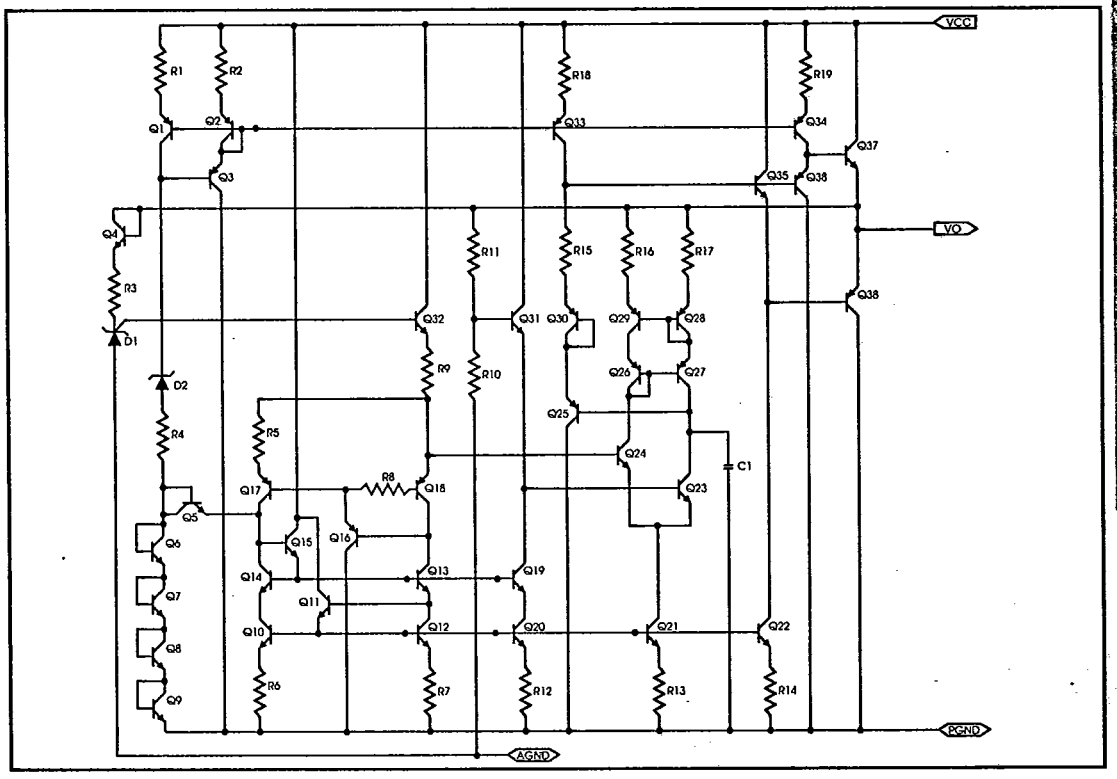
Features

- Precision 10V Reference Voltage
- 3ppm/°C Tempco
- 5mV Output Tolerance
- 4μV Noise (10Hz BW)
- 75mV/V Line Regulation
- 100mV/V Load Regulation
- 2mA Supply Current
- Fits in 2 Tiles
- Design/Layout Available in NiCr



Description

The **RBZ10** is a 10V precision reference based on a Kelvined buried-zener diode, which eliminates the error caused by parasitic cathode resistance, which improves the tempco of the reference. The zener is compensated by a precision PTAT (proportional-to-absolute-temperature) generator. An amplifier is provided to boost the compensated zener voltage (about 5V) to a 10V output level. The combination of a Kelvined buried-zener, a specially-designed output amplifier, and PTAT compensation form a reference of outstanding performance. Two trims are required for maximum performance, one for TC and another for output level.



SP2000 Series Analog Array MacroCell
Buried-Zener Reference —RBZ10

T-42-21

Specifications

All specifications at T_A=25°C, V_{CC} = +15V

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Characteristics						
Output Voltage	V_O		10		V	Note 1
Drift	TC		3		ppm/°C	Note 1
Noise	e_{NO}		4		µV	0.1-10Hz
Line Regulation			100		µV/V	
Load Regulation			100		µV/mA	
Output Current Drive	I_L		5		mA	
Power Supply						
Supply Voltage Range	V_{CC}	13		30	V	
Supply Current	I_{CC}		2		mA	

Note:
1) Requires trimming for maximum performance

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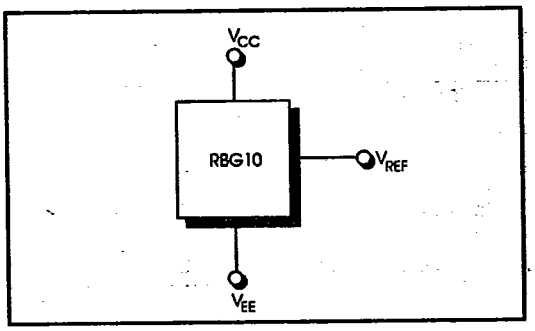
T-42-21

SP2000 Series Analog Array MacroCell
10V Band-Gap Reference — RBG10

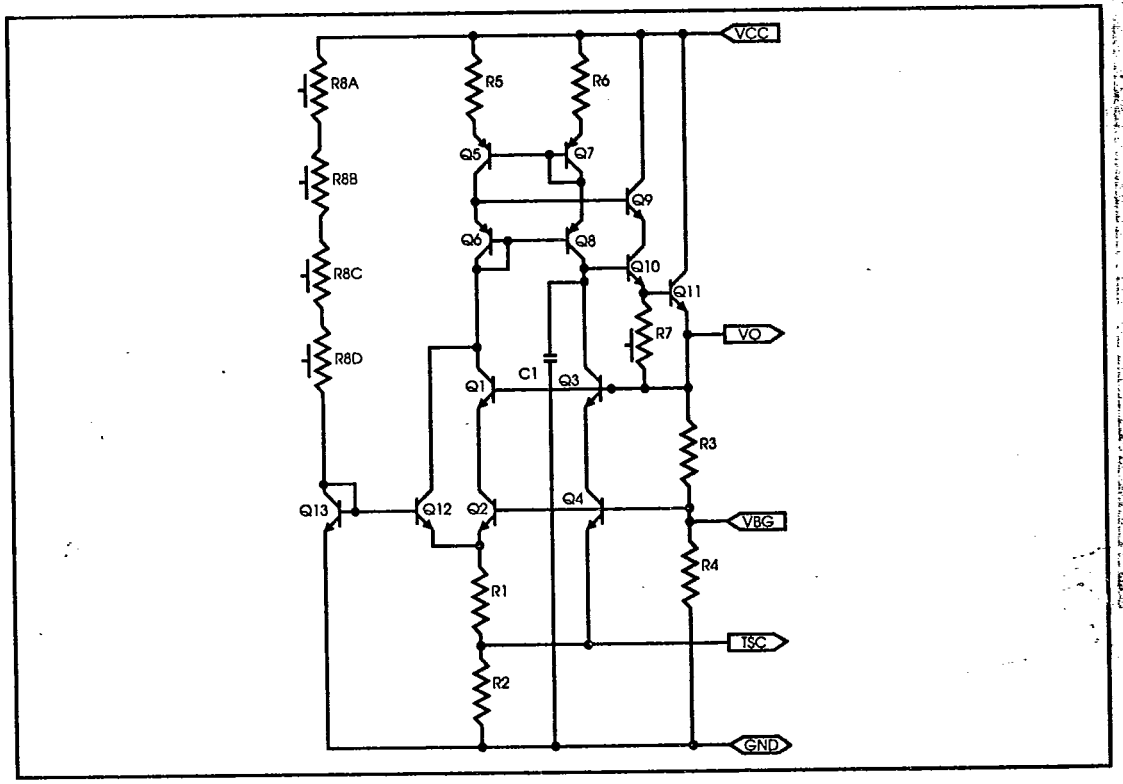
Features

- 50ppm/°C Untrimmed Tempco
- Laser-Trimmable Output Voltage
- Laser-Trimmable Tempco
- 5mA Output Current Capability
- 0.5mA Supply Current
- Fits in 1 Tile
- Design/Layout Available in NiCr



Description

The **RBG10** is a voltage reference macrocell featuring a 10 volt output. The basic reference element is a "band gap" with first-order temperature compensation. To achieve optimum temperature performance, the **RBG10** employs NiCr resistors with appropriate matching to minimize temperature effects, which provide a 50ppm/°C untrimmed temperature coefficient. The **RBG10** can be trimmed, both for output voltage and reduced temperature coefficient. It can source 5mA of output current. It fits within one tile.



SP2000 Series Analog Array MacroCell
10V Band-Gap Reference —RBG10

T-42-21

Specifications

All specifications at T_A=25°C, V_{CC} =+15V, V_{EE} =0V

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Characteristics						
Output Voltage	V_O		10		V	
Output Current						
Sourcing	$-I_{OUT}$		5		mA	
Sinking	$+I_{OUT}$		0.25		mA	
V_O Temperature Coefficient	TC_{VO}		50	150	ppm/°C	
Power Supply						
Supply Voltage Range	V_{SUPPLY}	14		35	V	V_{CC} - V_{EE}
Supply Current	I_{CC}		0.5		mA	Quiescent; V_{CC}=+15V, I_{OUT}=0mA
V_O Load Regulation	$\Delta V_O/\Delta I_O$		1	10	mV/mA	
V_O Line Regulation	$\Delta V_O/\Delta V_S$		5	20	mV/mA	

Note:
1) Design limits account for process and temperature variations and should be used for worst-case design analysis.