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Advance Information

DSP56ADC16 16-Bit Sigma-Delta Analog-to-Digital Converter

The DSP56ADC16 is a single-chip, linear, 16-bit, oversampling, analog-to-digital (A/D) converter, providing output sample rates up to 100 kHz. Third-order noise-shaping sigma-delta technology is employed utilizing 64 times oversampling, which yields 96-dB dynamic range and 90-dB signal-to-noise ratio for the signal bandwidths from 0–45.5 kHz with an in-band ripple of less than 0.001 dB. The DSP56ADC16 is an ideal choice for high-performance digital audio systems, such as digital audio disk, tapes, and processors as well as voice-bandwidth communication and control applications. It does not require antialiasing filters and sample-and-hold (S/H) circuitry because they are an inherent part of the sigma-delta technology. The DSP56ADC16 can easily be interfaced to the DSP56001 and other host processors using its flexible serial interface. Output is also provided before the final finite impulse response (FIR) decimation filter for applications requiring higher speed, lower group delay, and 12-bit accuracy for AC levels. The DSP56ACD16 can also be used with an input multiplexer at a minimum output sampling interval (15 μsec) in the comb filter output mode.

Key features of the DSP56ADC16 include the following:

- 16-Bit Output Resolution at 100 kHz from FIR Filter
- 12-Bit Output Resolution at 400 kHz from Comb Filter
- 96-dB Dynamic Range
- 90-dB Signal-to-THD Ratio
- 90-dB Signal-to-Noise Ratio
- In-Band Ripple: <0.001 dB
- Maximum Output Sample Rates (FIR Filter: 100 kHz; Comb Filter: 400 kHz)
- Maximum Input Sample Rate: 6.4 MHz
- Maximum Internal Clock Rate: 12.8 MHz
- DC Stability: 10 Bits
- Supply Voltage: Single +5 V ±10%
- Supply Current: <100 mA
- 20-Pin CERDIP, Plastic, and Surface Mount Packages
- Single Chip
- Linear-Phase Analog Front End and Internal Digital Filters
- Simple Serial Interface to Host Microprocessors
- No-Glue Interface to DSP56001/7720/320XX Processors
- Fully Differential Inputs

This document contains information on a new product. Specifications and information herein are subject to change without notice.

INTERNAL ARCHITECTURE

The A/D converter is a key component in data acquisition systems, such as those found in digital audio systems, high-accuracy measurement systems, communications, and digital signal processing (DSP) systems in general. High-resolution A/D converters have typically used successive-approximation techniques with complicated trimming/calibration or dual-ramp conversion techniques, which require accurate comparators and expensive S/H circuits to yield over 15 bits of accuracy. In addition, the antialiasing filter for these A/D converters generally sets severe limitations on the attainable signal-to-noise ratio and phase linearity.

The DSP56ADC16 uses an advanced third-order sigma-delta quantizer to implement an oversampled noise-shaping A/D converter system on a single chip. By oversampling the input signal, the overall quantization noise spectrum expands well beyond the frequency band of interest. Third-order noise shaping insures that this expanded noise spectrum contains very little noise power in the pass band. The oversampled signal is low-pass filtered, effectively rêmoving the out-of-band quantization noise. The low-pass filtering is then followed by decimation to reduce the output sample rate commensurate with the frequency band of interest and to increase the resolution. In the DSP56ADC16, the filtering and decimation are performed in two steps to reduce digital filter complexity. Since the input signal is oversampled by a factor of 64, the need for a high-order antialiasing filter can be eliminated

The DSP56ADC16 consists of three major sections: 1) analog front end (AFE), 2) compensated decimation digital filters, and 3) serial interface (see Figure 1). The AFE consists primarily of three differential, switched-capacitor, linear integrators. These highly stable, fully differential integrators perform the noise-shaping function. The decimation digital filter section consists of a 16:1 decimation comb filter stage followed by a 4:1 decimation low-pass/compensation FIR filter stage, resulting in a total decimation ratio of 64:1. The frequency response of the decimation digital filters is described in **FIRST- AND SECOND-STAGE DECIMATION**. The serial interface provides serial communication to a host processor. This interface uses three dedicated pins: serial data output (SDO), frame sync output (FSO), and serial clock output (SCO). The serial interface format of operation in pin selectable. The timing diagrams for the serial interface are described in **AC ELECTRICAL SPECIFICATIONS**.

SIGNAL DESCRIPTIONS

The DSP56ADC16 is available in 20-pin CERDIP, plastic, and surface mount packages. The functional pin definitions (see Figure 2) and their mnemonics are explained in the following paragraphs:

Clock Input (CLKIN)

This pin accepts the input clock for the DSP56ADC16. This TTL-level compatible input accepts clock frequencies in the range from 1.0–12.8 MHz. The output sample rate is equal to the CLKIN requency divided by 128.

Frame Sync Input (FSI)

This active-high input is used to start or reset the serial data output and synchronize internal circuits. It is not a start convert pulse since the DSP56ADC16 is always converting at a rate of CLKIN/128. FSI is sampled on the falling edge of CLKIN (see the timing diagram shown in Figure 14). When this signal goes high, the DSP56ADC16 will begin transmitting bits via the serial data

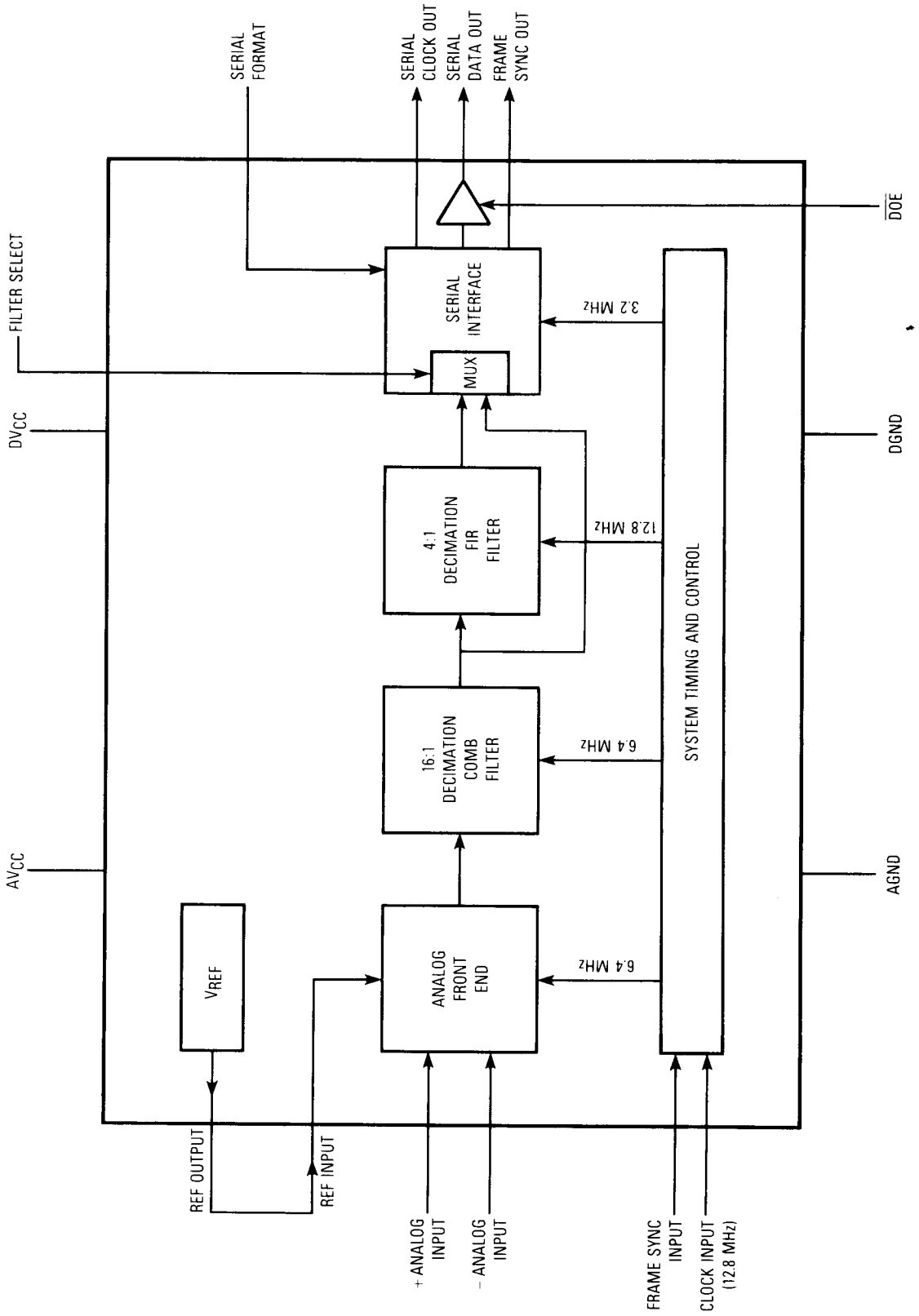


Figure 1. Internal Block Diagram

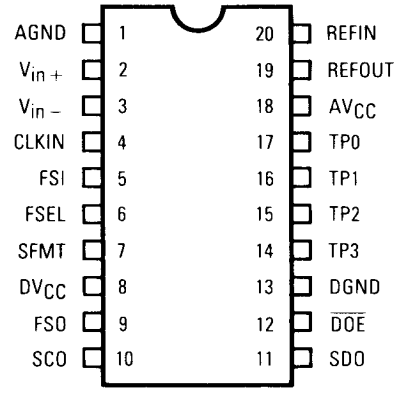


Figure 2. Pin Assignment

out (SDO) pin. FSI is an optional input signal. If the FSI pin is grounded, frame syncs will be internally generated automatically. The purpose of FSI is to allow external control of the phasing of the A/D conversion process. FSI should be a periodic signal occurring every 16 SCO clock periods in the comb filer output mode and every 32 SCO clock periods in the FIR filter output mode. In all cases, FSI must be synchronized to CLKIN as defined in the timing specification. FSI allows multiple DSP56ADC16s to be synchronized using a common frame sync source. When using a common frame sync signal with multiple DSP56ADC16s, a common CLKIN signal is required.

Analog + Input (V_{in+})

This pin is the A/D converter analog noninverting input. If an input sample rate antialiasing filter is used prior to the V_{in} inputs, high-quality polystyrene or equivalent capacitors must be used to meet the published THD specification. See the connection diagram example in Figure 7 for a typical single-pole input filter.

Analog − Input (V_{in-})

This A/D converter analog inverting input has the same characteristics as V_{in+}.

Reference Input (REFIN)

The analog reference voltage applied to this pin sets the analog input range. Its magnitude sets both positive and negative full scale. The maximum input is +2.0 V. The maximum peak-to-peak input signal is 2 × REFIN. Since this input is extremely sensitive to induced noise, reference input decoupling is recommended to achieve the maximum performance (see Figures 7 and 12). Failure to do so may result in a degradation of SNR. The output of the DSP56ADC16 is

$$\frac{(V_{in+}) - (V_{in-})}{V_{refin}}$$

Reference Output (REFOUT)

This pin has an on-board reference voltage output of +2.0 V given a +5.0 V supply. This pin should be connected to REFIN when an external reference input is not used.

Serial Clock Output (SCO)

This pin provides the serial bit clock for the SDO port. When the FIR filter output is selected by setting FSEL = 0, the rate of this output is CLKIN divided by four; when the comb filter output

is selected by setting FSEL = 1, the rate of this output is CLKIN divided by two. See Figures 15 and 16 for timing details.

Serial Data Output (SDO)

A 16-bit serial data stream is output on the SDO pin once per frame sync output cycle. This data changes synchronously to the SCO pin. Format is twos complement transmitted most significant bit (MSB) first. See Figures 15 and 16 for timing details.

Serial Format (SFMT)

This pin selects the formats of the FSO and SCO when the FIR filter output is selected by FSEL = 0. The two formats of operation are shown in Figure 15.

Frame Sync Output (FSO)

This output is used to indicate the beginning of serial word transmission on the SDO pin. The shape and timing of the FSO pulse are controlled by the SFMT pin. Refer to Figures 15 and 16 for timing details of FSO.

Analog V_{CC} Supply (AV_{CC})

This pin is the positive analog power supply (+5 V ±10%) for the analog integrator section.

NOTE

Analog V_{CC} and digital V_{CC} should be decoupled with respect to AGND and DGND, respectively, to obtain published specifications. The decoupling is intended to isolate digital noise from the analog section. Decoupling capacitors should be as close as possible to their respective analog and digital supply pins.

Digital V_{CC} Supply (DV_{CC})

This pin is the positive digital power supply (+5 V ±10%) for digital internal circuitry and pad drivers (see **Analog V_{CC} Supply (AV_{CC})**).

Analog Ground (AGND)

This pin, which is the analog ground return for the analog front end, is **not** internally connected to digital ground (DGND).

Digital Ground (DGND)

This pin is the ground connection for digital internal circuitry and pad drivers.

Filter Select (FSEL)

This input allows selection of the final FIR filter output or the comb filter output. When FSEL is low, the SDO pin will deliver the final low-pass/compensation FIR filter output. When FSEL is high, the SDO will deliver the comb filter output at a four-times-faster output sample rate with two-times-faster clock rate than the FIR filter output, and the SFMT pin is disabled (SFMT = 0) as shown in Figure 16 (see **Serial Clock Output (SCO)** and Figure 15).

Data Output Enable ($\overline{DOE}$)

This pin is the SDO three-state control pin. When $\overline{DOE}$ is asserted (low), the SDO is active. When $\overline{DOE}$ is deasserted (high), the SDO is in a high-impedance state. $\overline{DOE}$ can be used for multiplexing several A/D converters into one host serial input. This pin, an asynchronous input, operates independently of input or output clocks (see Figure 17).

Test Pins (TP0–TP3)

These test pins are reserved for factory use. In normal operation, these pins should be connected to DGND.

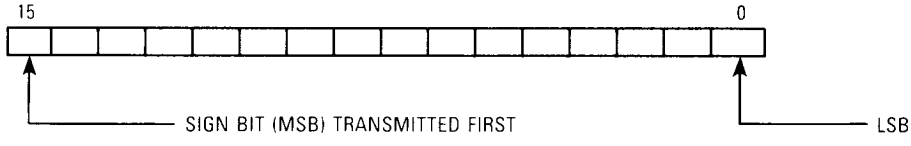
INPUT/OUTPUT CLOCKS AND CONTROL

The DSP56ADC16 output sample rate is defined by a combination of the CLKIN frequency and the output filter selected (determined by the FSEL pin). When FSEL = 0, the FIR filter is selected, and the output sample rate is equal to CLKIN divided by 128. When FSEL = 1, the comb filter is selected, the decimation ratio is changed to 16:1, and the output sample rate is equal to CLKIN divided by 32. The input sample rate is always the CLKIN frequency divided by two.

In normal mode (FSEL = 0), the clock rate of the SCO is defined as the CLKIN frequency divided by four, giving a maximum serial clock output of 3.2 MHz (see Figure 15). However, when the comb filter output is selected (FSEL = 1), the rate is changed to the CLKIN frequency divided by two, giving a maximum rate of 6.4 MHz (see Figure 16). The timing relationship between CLKIN, FSI, and SCO when the FSEL pin is set to zero for FIR filter output is presented in **AC ELECTRICAL SPECIFICATIONS** (also see **Filter Select (FSEL)**).

SERIAL INTERFACE

The DSP56ADC16 has three output pins for the serial interface: 1) serial data out (SDO), 2) frame sync out (FSO), and 3) serial clock out (SCO). The corresponding internal block diagram is shown in Figure 3. The serial port can interface with general-purpose DSPs such as the DSP56001, NEC7720, and TMS320XX without additional "glue" circuitry. The format of the fractional data output from the A/D converter is MSB first 16-bit serial twos complement. The serial data format for interfaces is defined as follows:



The SFMT pin selects between one clock-wide active-high frame sync pulse and one data-word-wide active-low frame sync pulse (see Figure 15).

FIRST- AND SECOND-STAGE DECIMATION

The first-stage comb filter provides initial filtering of the quantized output from the analog front end as well as decimation of the input sample rate by a factor of 16:1. The z-domain transfer function of the stage can be expressed as

$$H(z) = \frac{(1 - z^{-16})^4}{(1 - z^{-1})^4}$$

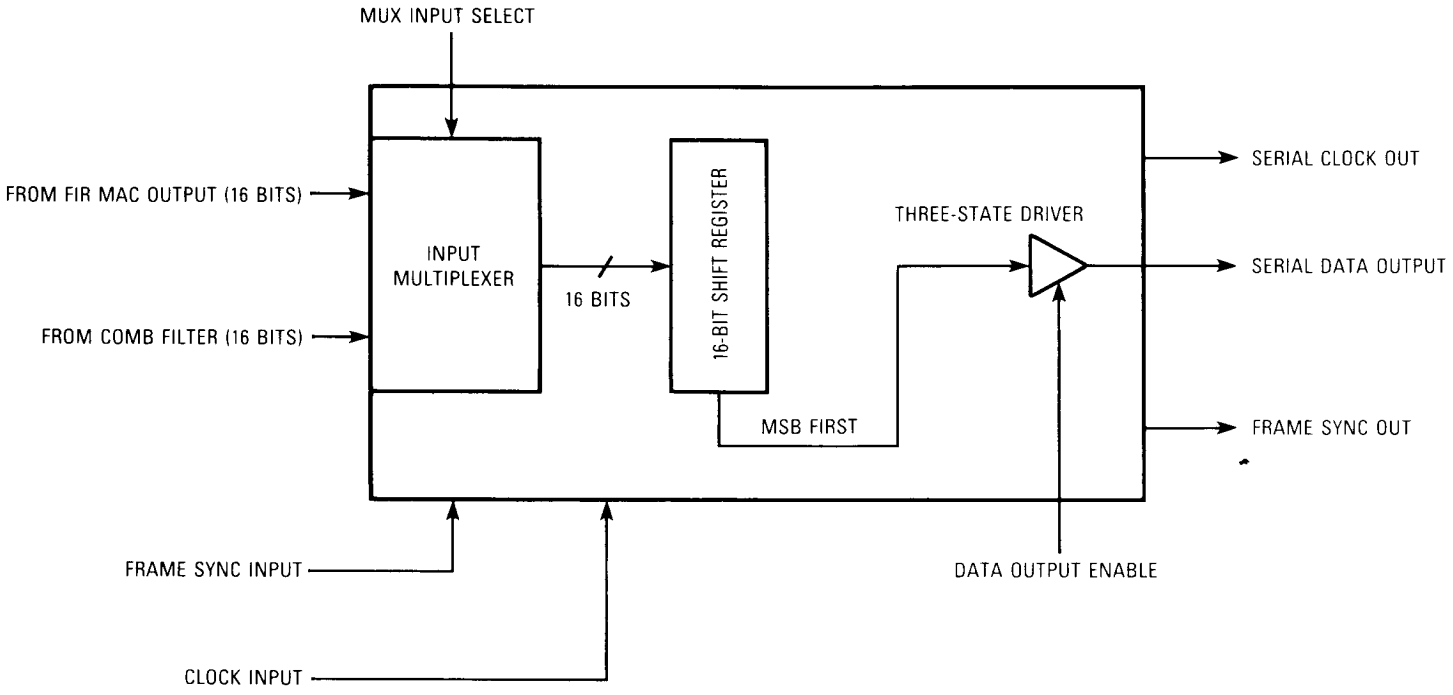


Figure 3. Block Diagram of Serial Interface

The frequency domain (in Hz) equaivalent of the transfer function is

$$\overline{H}(f) = \left[\frac{1}{16}\,\frac{\sin(16\pi fT)}{\sin(\pi fT)}\right]^4$$

where

$$T = \frac{1}{f_S}$$

f_S = the input sample rate for the AFE (maximum 6.4 MHz)

Figure 4 shows the magnitude response of the comb filter section. Since the comb filter has a nonflat low pass-like frequency response in the pass-band region, the following second-stage FIR filter should compensate for the pass-band droop as well as providing the final sharp cutoff required for 16 bits of dynamic range. Figures 5 and 6 illustrate the frequency reponses of the low-pass FIR filter and the compensation filter, respectively. The 255-tap FIR filter coefficients are designed for a low-pass filter with nine-percent transition-band and the following pass-band amplitude compensation characteristics: pass-band cutoff frequency, 45.5 kHz; stop-band cutoff frequency, 50 kHz; pass-band ripple, 0.0003 dB; and a stop-band ripple, −96 dB when the chip is operated at a CLKIN frequency of 12.8 MHz. The 16-bit output of the first-stage comb filter is used as input to the second-stage FIR filter. This filter removes the out-of-band noise components and also acts as the system antialiasing filter. Since the in-band signal has been shaped by the third-order noise-shaping integrators, the signal-to-noise ratio achieved is more than 90 dB. Note that the pass-band and stop-band frequencies of both the comb and FIR filters scale linearly with the CLKIN frequency.

The 38-bit accumulator of the FIR filter is convergently rounded for 16-bit output to the serial interface section. This output provides 90-dB signal-to-THD ratio and 96-dB dynamic range in the 0–45.5 kHz band, which makes this device suitable for high-performance digital audio applications.

TECHNOLOGY COMPARISONS

Three techniques have traditionally been used in A/D converter implementation: successive approximation, integrating, and flash. These techniques are implemented under Nyquist-sampled criterion (set to be about twice a signal frequency bandwidth) compared to the oversampled method for the sigma-delta technology.

Successive-approximation A/D converters compare the unknown input with sums of accurately known fractions of full scale in the successive-approximation register (SAR), starting with the largest fraction and rejecting any fraction that causes the sum to become greater than the unknown input. The on-chip D/A converter used to generate the sum of fractions must be very accurate and may require external trimming. The settling time for 16 approximations in succession for 16-bit performance must be less than 10 μs for a 100-kHz sample rate. Allowing 5 μs to acquire the signal to the specified linear error, 5 μs is left for 16-bit digitization process that yields ≈0.3 μs for each bit.

Integrating A/D converters count pulses for a period proportional to the input. Dual-slope integrating converters count the period required for the integral of the reference to equal the average

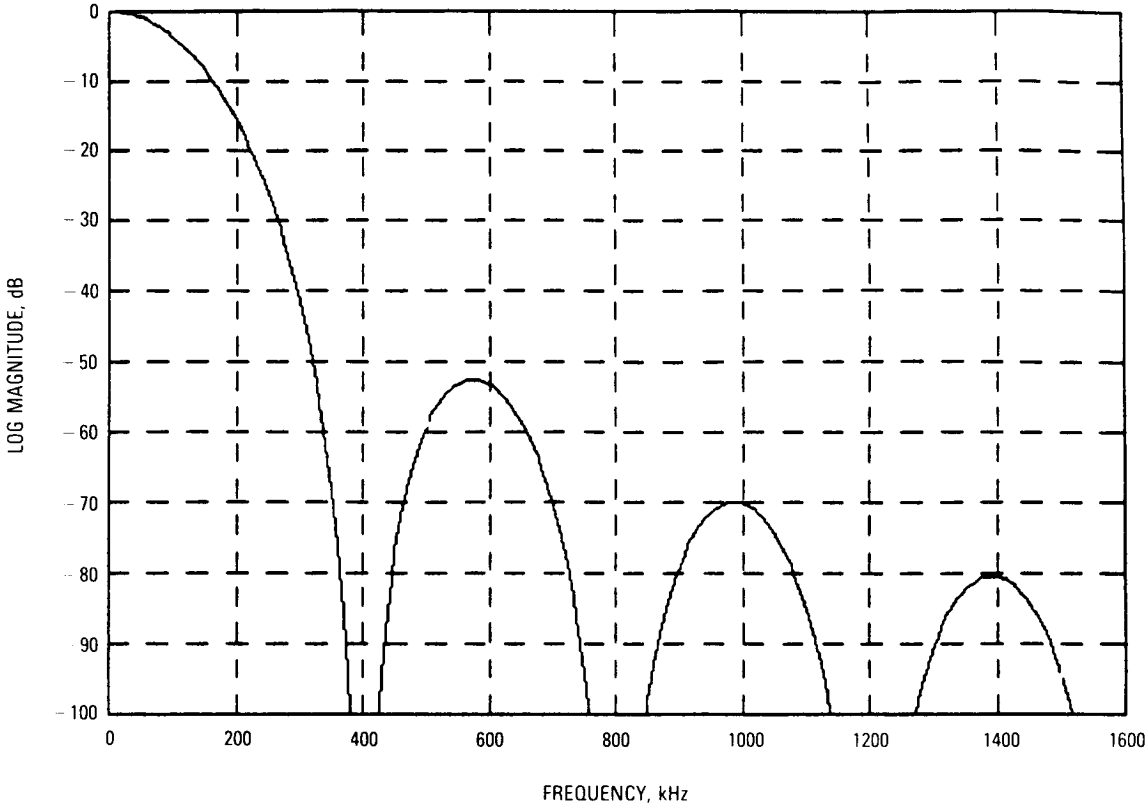


Figure 4. Magnitude Response of Comb Filter (CLKIN = 12.8 MHz)

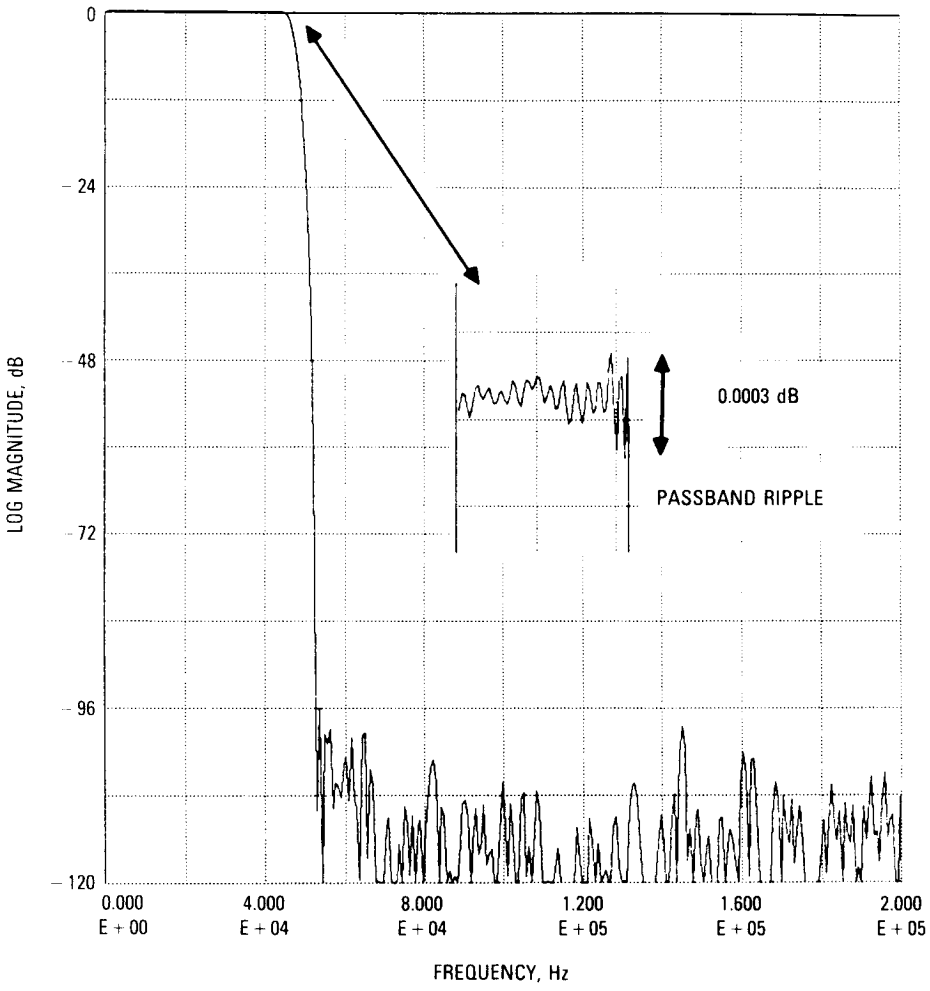


Figure 5. Magnitude Response of Low-Pass FIR Filter

value of the input over a fixed period of time. As with successive approximation, external trimming is required.

Flash A/D converters are simple and fast. This approach has found low-resolution and high-speed application. This method requires only one step in determining the input voltage — a series of comparators test the input signal against a set of voltage thresholds established by a ladder network. Digital logic is then employed to convert the comparator outputs to a binary number. To operate in such a fast manner $2^B - 1$ comparators are required where B denotes the number of bits of resolution. Therefore, for 16-bit resolution, 65,535 comparators and a significant amount of priority encoding logic would be needed to achieve current comparable performance.

Sigma-delta A/D converters use a low-resolution A/D converter (1-bit quantizer) in a feedback configuration. The high resolution (96-dB SNR) is achieved by the noise-shaper (third order for the DSP56ADC16). The noise transfer function is essentially a high-pass filter so that the noise is shifted to higher out-of-band frequencies where it is then filtered out. The input sampling rate for sigma-delta modulation is much higher (64 times for the DSP56ADC16) than the rate for the other three techniques for the same bandwidth. Because of the high sampling rate and the low-precision A/D conversion used on the front end of a sigma-delta system, an S/H circuit is not

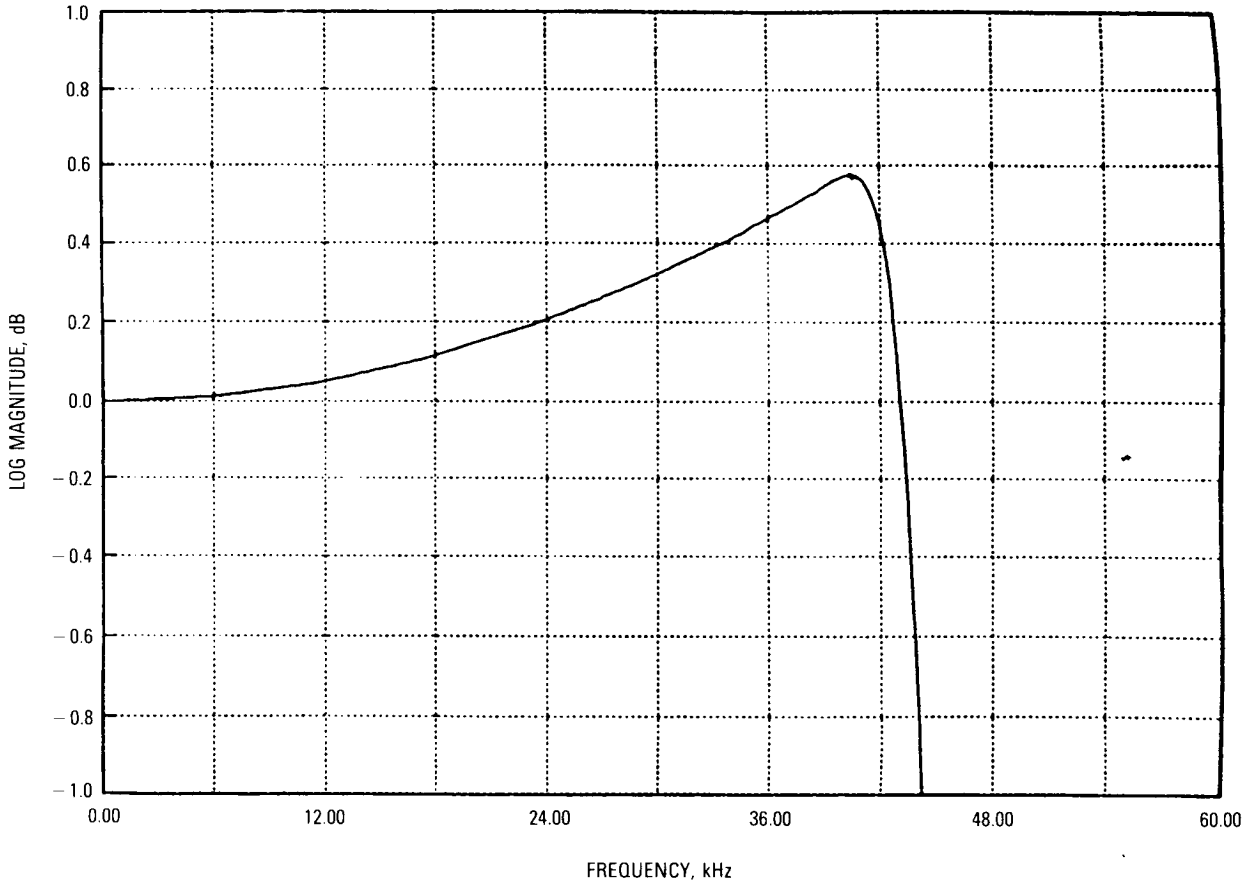


Figure 6. Magnitude Response of Compensation FIR Filter

needed. Since the sampling rate is much higher, the antialiasing filter is not required, or a simple one-pole RC filter can be used to attenuate a high-frequency input signal.

The successive-approximation, integrating, and flash techniques require extremely high-performance analog antialiasing filtering and precise S/H circuits to ensure 16-bit accuracy and 100-kHz sample rate. Therefore, the antialiasing filter has to be a very steep "brickwall" filtering outside the pass band. A 30-pole Bessel-approximated infinite impulse response (IIR) filter is necessary to obtain almost linear phase and less than 0.0001 ripple over the entire pass band, 96-dB stop-band attenuation, and fast transition between pass band and stop band, which is unachievable in real implementation. Also, the allowable aperture jitter of the S/H circuit is only 48.6 ps, which makes circuit manufacturing very expensive.

In contrast, sigma-delta modulation-based A/D technology can meet the performance goals of 16-bit resolution and 100-kHz sample rate with moderate cost. The tutorial of the sigma-delta technology can be found in *Technical Bulletin* of Motorola Digital Signal Processing Operations, entitled "*Principles of Sigma-Delta Modulation for Analog-to-Digital Converters,*" which can be requested from:

Motorola DSP Operations, OE314
6501 William Cannon Drive West
Austin, Texas 78735

PERFORMANCE EVALUATIONS

Figure 7 shows the input circuitry used for testing signal-to-noise and signal-to-THD ratios. A low-distortion (>96 dB SNR) signal generator is applied differentially to the BNC inputs, and an FFT with the Blackman-Harris window is performed to measure the noise and distortion. AC characteristics of digital outputs (FSO, SDO, and SCO) are measured while connected to one standard TTL load.

Figure 8(a) shows the spectral purity of the DSP56ADC16 with a 6-kHz full-scale sine-wave input when the output sampling rate is 48K samples per second. Since the 1024-point FFT has 512 spectral bins up to Nyquist frequency, the typical noise floor and the harmonic distortion can be measured by summing the power of corresponding bins, which gives −90 dB and −92 dB, respectively. The typical spectral plot for the comb filter output is shown in Figure 8(b).

Figure 9 illustrates the differential nonlinearity (DNL) plots of DSP56ADC16. Sigma-delta converters are inherently linear and do not suffer from appreciable DNL or missing codes. The plot shows the distributions of $2^{16} = 65{,}536$ possible codes for the 16-bit converter. The distribution of DNL codes are within ±0.5 LSB.

The measurements of the time delays due to the internal propagation delay and linear-phase filter operation may be useful for multiplexed applications. Figure 10(a) and 10(b) illustrates the rectangular pulse responses of the comb filter output and FIR filter output, respectively. Figure

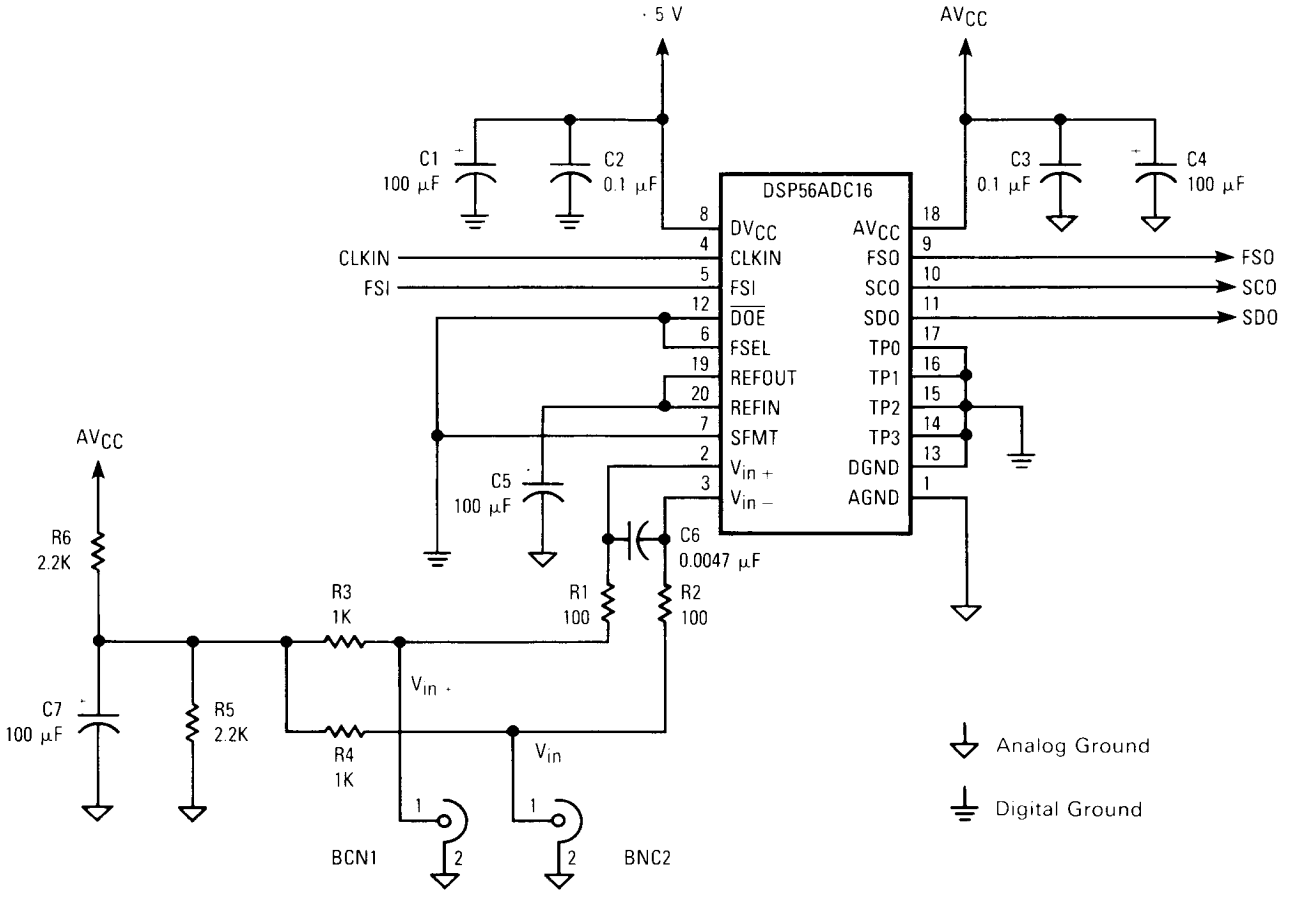


Figure 7. Functional Test Circuit

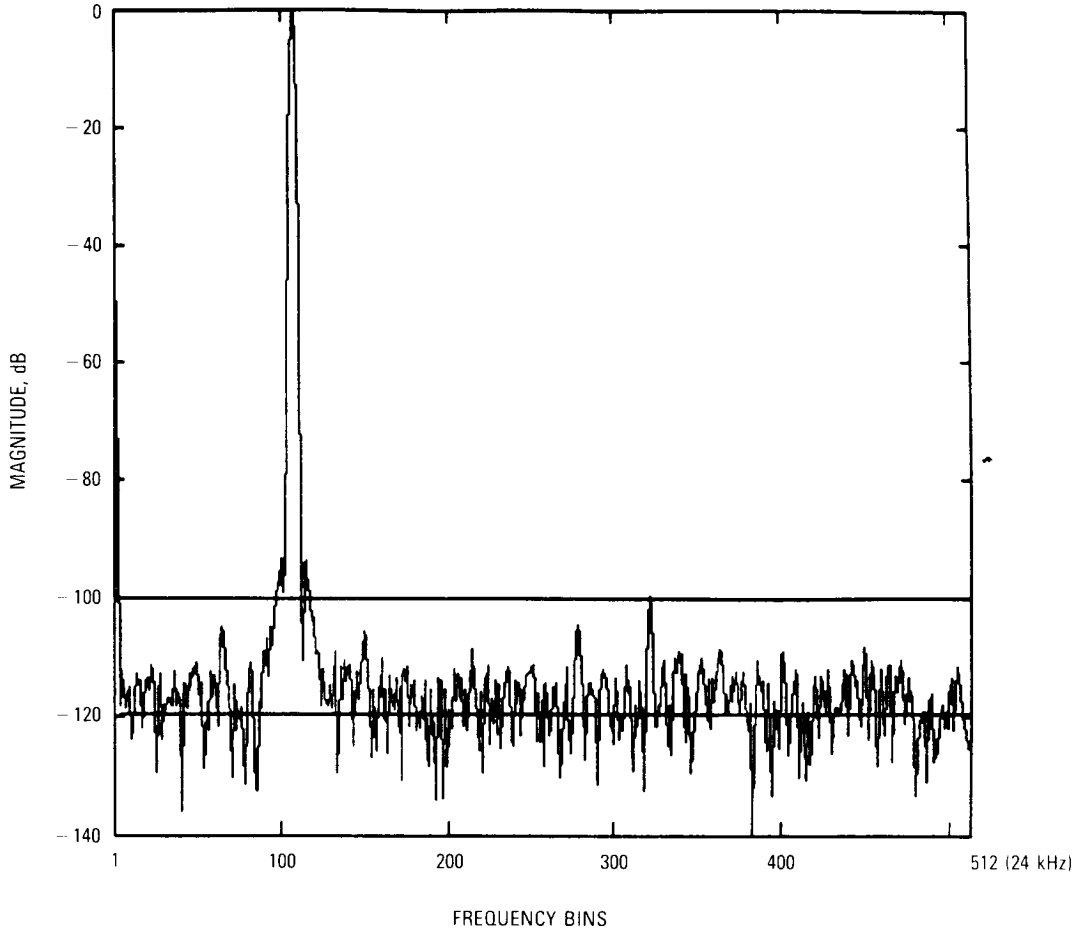


Figure 8(a). Typical Spectrum of FIR Filter Output (512 Bins of 1024 FFT)

11 illustrates a sine-wave input response. The output response includes not only the internal delays of DSP56ADC16 but also measurement delays, such as a data transfer time and a D/A conversion time of 2.5 μs and 3.0 μs, respectively, for these plots.

The DSP56ADC16 can also be used with an input multiplexer when the comb filter output is selected by setting FSEL = 1 (see **SIGNAL DESCRIPTIONS**). The minimum multiplex intervals which depend on the settling time as shown in Figure 10(a) can be given by

$$\tau_{mux} \geqslant \frac{162}{f_{clk}}; \text{excluding the time required to shift the data out from the serial interface}$$

and

$$\tau^{s}_{mux} \geqslant \frac{194}{f_{clk}}; \text{including the time required to shift the data out from the serial interface}$$

These expressions are based on theoretical analysis. However, there are practical aspects which need to be considred. First, the multiplex interval must be a multiple of 32 clock periods (i.e., the comb filter output rate). If the FSI and the multiplexer can be perfectly synchronized, this results in the multiplex intervals of $\tau_{mux} \geqslant 5\ T_S$ and $\tau^{s}_{mux} \geqslant 6\ T_S$ where T_S equals 32 t_{clk} (output sample interval). If the FSI and multiplexer are not synchronized, there can be one sample of time uncertainty so that $\tau_{mux} \geqslant 6\ T_S$ and $\tau^{s}_{mux} \geqslant 7\ T_S$. If $f_{clk} = 12.8$ MHz, the minimum multiplex intervals,

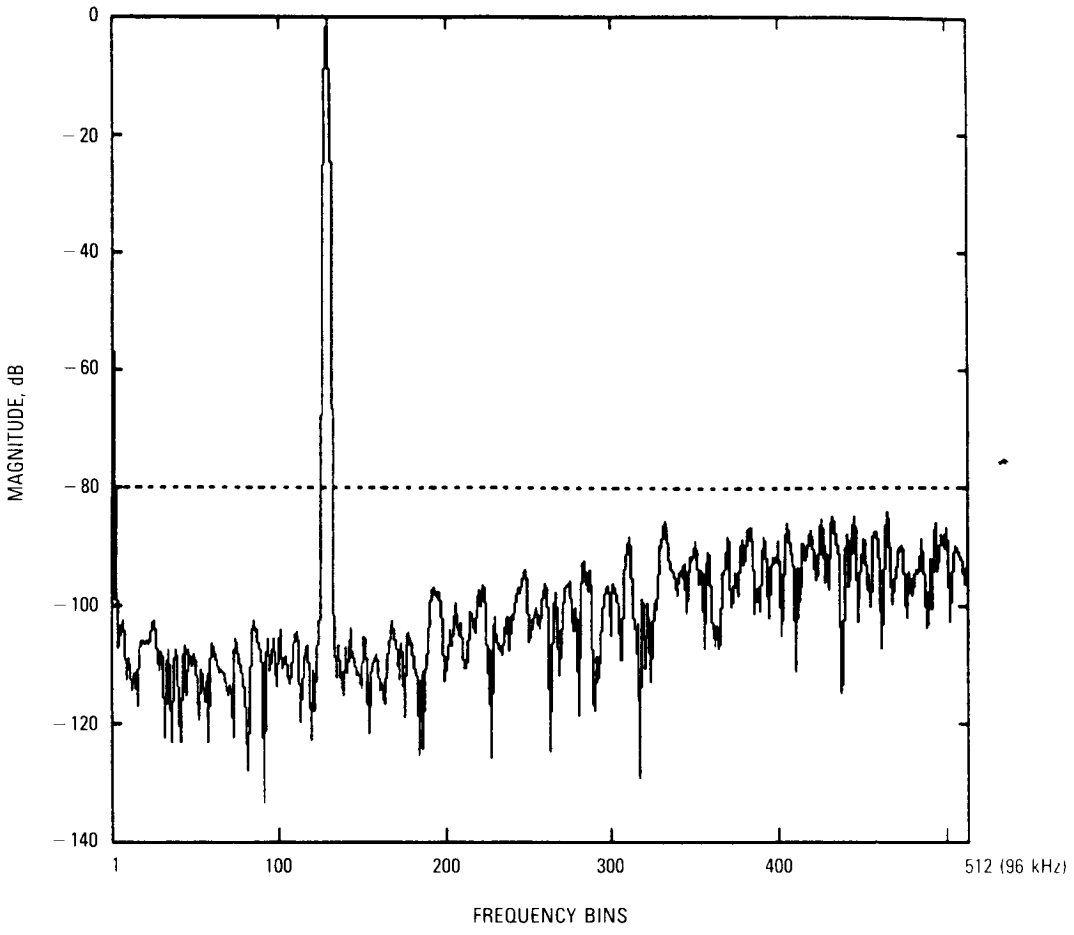


Figure 8(b). Typical Spectrum of Comb Filter Output (512 Bins of 1024 FFT)

τ_{mux} and τ_{mux}^{s}, are 15 μsec and 17.5 μsec, respectively. These results were verified by synchronizing a square wave input to the DSP56ADC16 and collecting and analyzing buffers of 32 data samples. In addition to these synchronization aspects, the following must be considered: 1) the response time of the multiplexer itself, 2) rolloff caused by any external antialiasing filter, and 3) if a DAC is used to display the output data, its response characteristic.

A general system connection diagram for an single-ended input signal is shown in Figure 12(a). Figure 12(b) illustrates the schematic diagram for multiplexing two DSP56ADC16s with the DSP56001. Figure 13 illustrates the system interface diagrams for popular general-purpose DSPs.

The analog input impedance, Z_{in}, and the minimum reference input impedance, Z_{ref}, can be computed by the following equations:

$$Z_{in} = \frac{10^{12}}{3\, f_{clk}}$$

$$Z_{ref} \geq \frac{10^{12}}{2.5\, f_{clk}}$$

where f_{clk} denotes the input clock rate. Table 1 shows the input impedances for selected input clock rates.

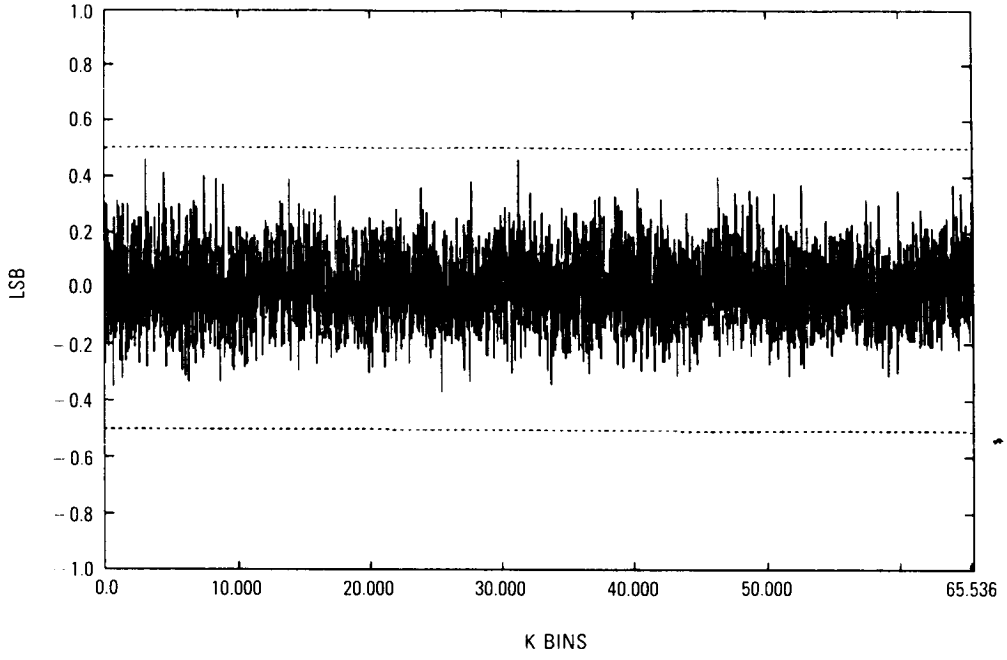


Figure 9. Typical Differential Nonlinearity (DNL) Plot

Table 1. Analog and Reference Input Impedance

Input Clock Rate (MHz)	Output Sample Rate (kHz)	Analog Input Impedance (kΩ)	Reference Input Impedance (kΩ)
12.8	100.0	26.0	Minimum 31.3
6.4	50.0	52.0	Minimum 62.5
6.144	48.0	54.3	Minimum 65.1
5.6448	44.1	59.0	Minimum 70.9

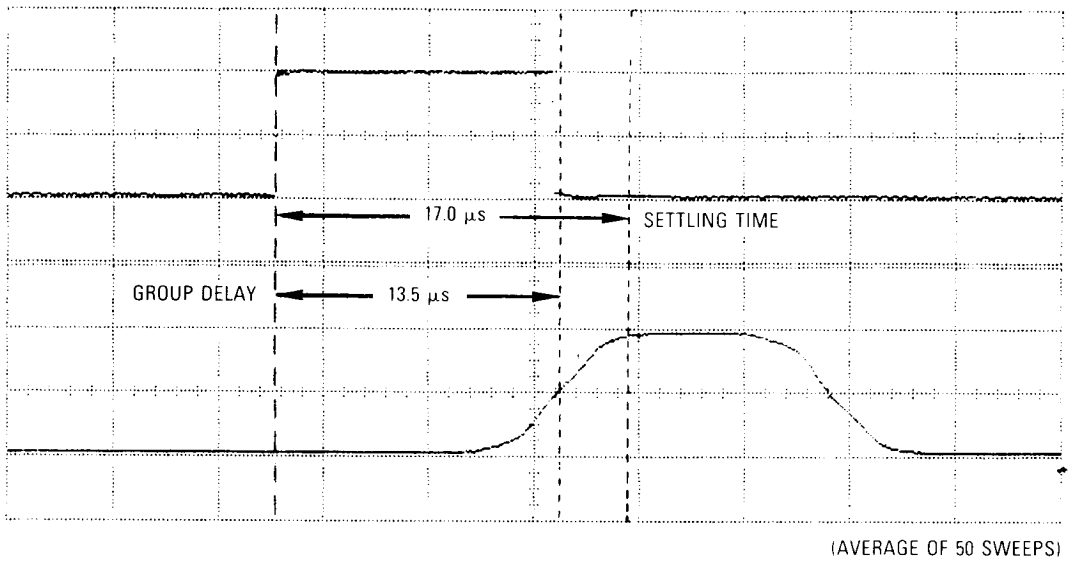


Figure 10(a). Typical Measured Group Delay and Settling Time of Comb Filter Output (CLKIN = 12.8 MHz)

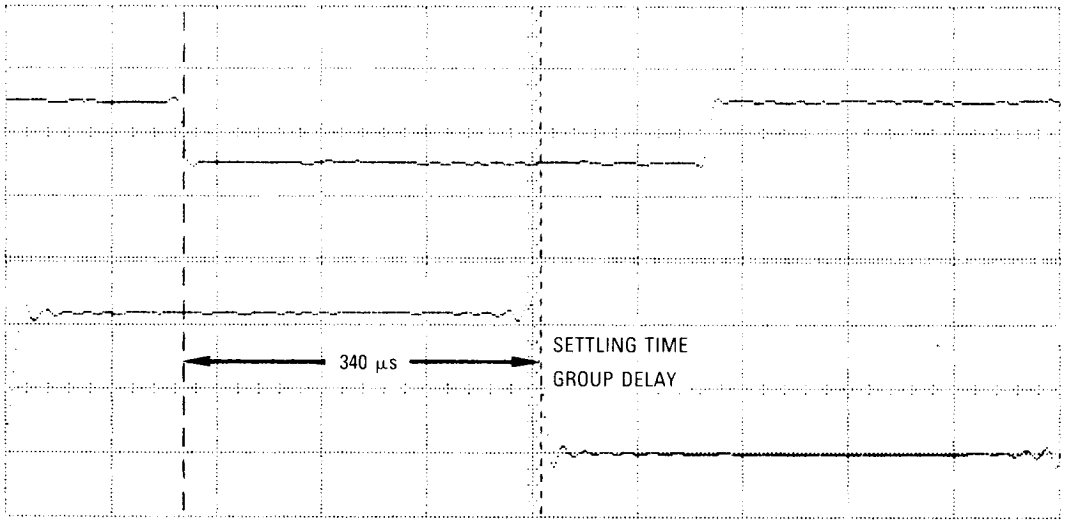
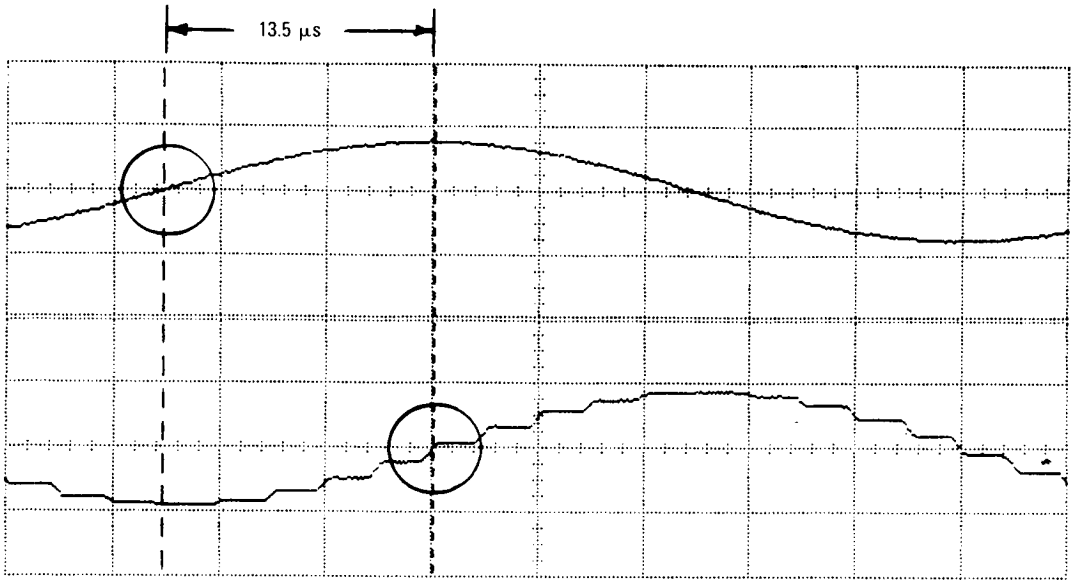
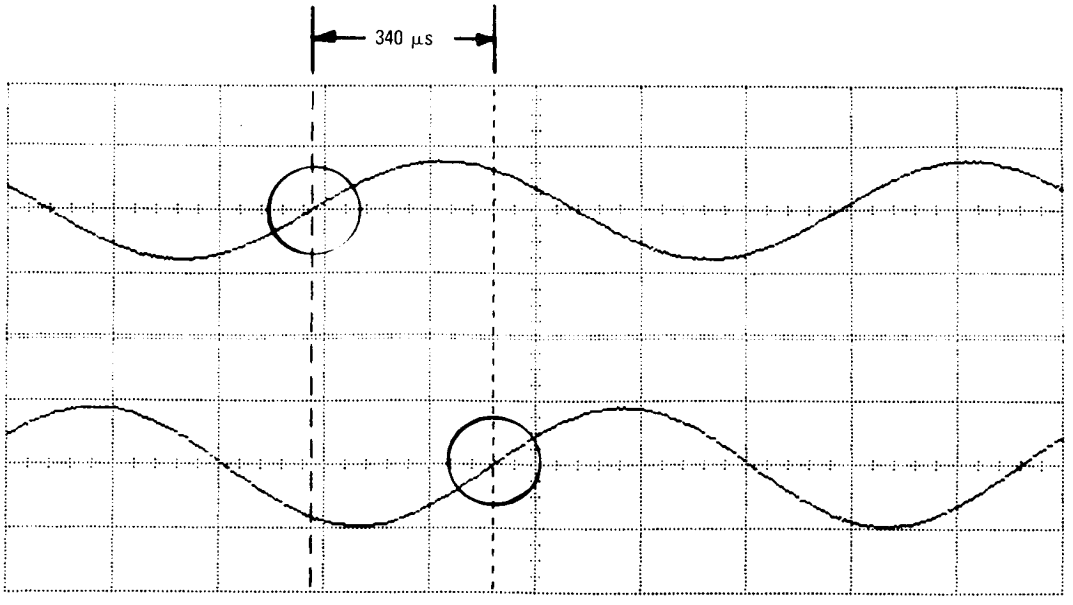


Figure 10(b). Typical Measured Group Delay and Settling Time of FIR Filter Output (CLKIN = 12.8 MHz)



Input Sinewave Frequency: 20.0 kHz @ 400 mV RMS (NO SWEEP AVERAGING)
CLKIN Frequency: 12.8 MHz

Figure 11(a). Typical Measured Group Delay of Comb Filter Output



Input Sinewave Frequency: 1.0 kHz @ 400 mV RMS
CLKIN Frequency: 12.8 MHz

Figure 11(b). Typical Measured Group Delay of FIR Filter Output

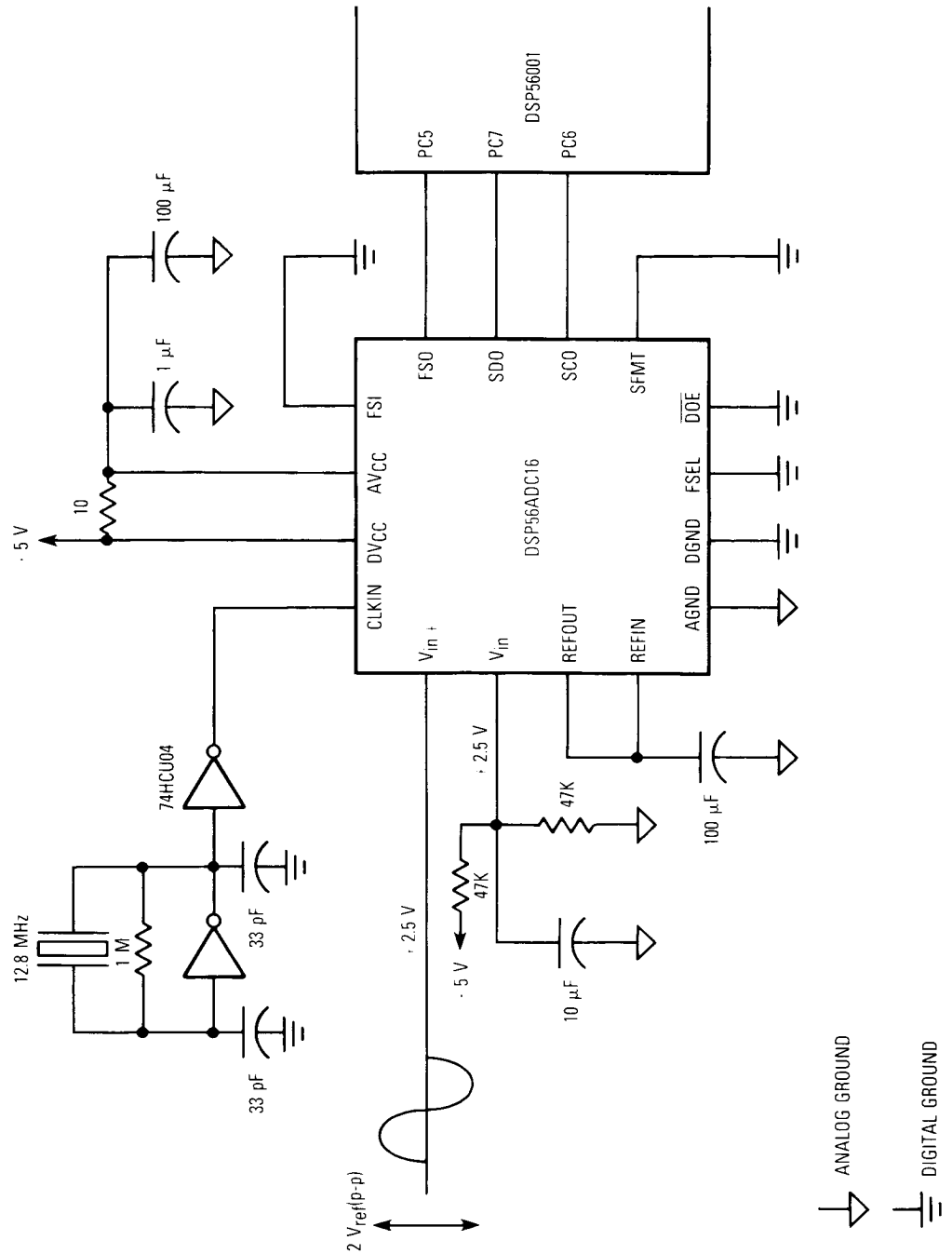


Figure 12(a). Single-Ended Mode Input Circuit

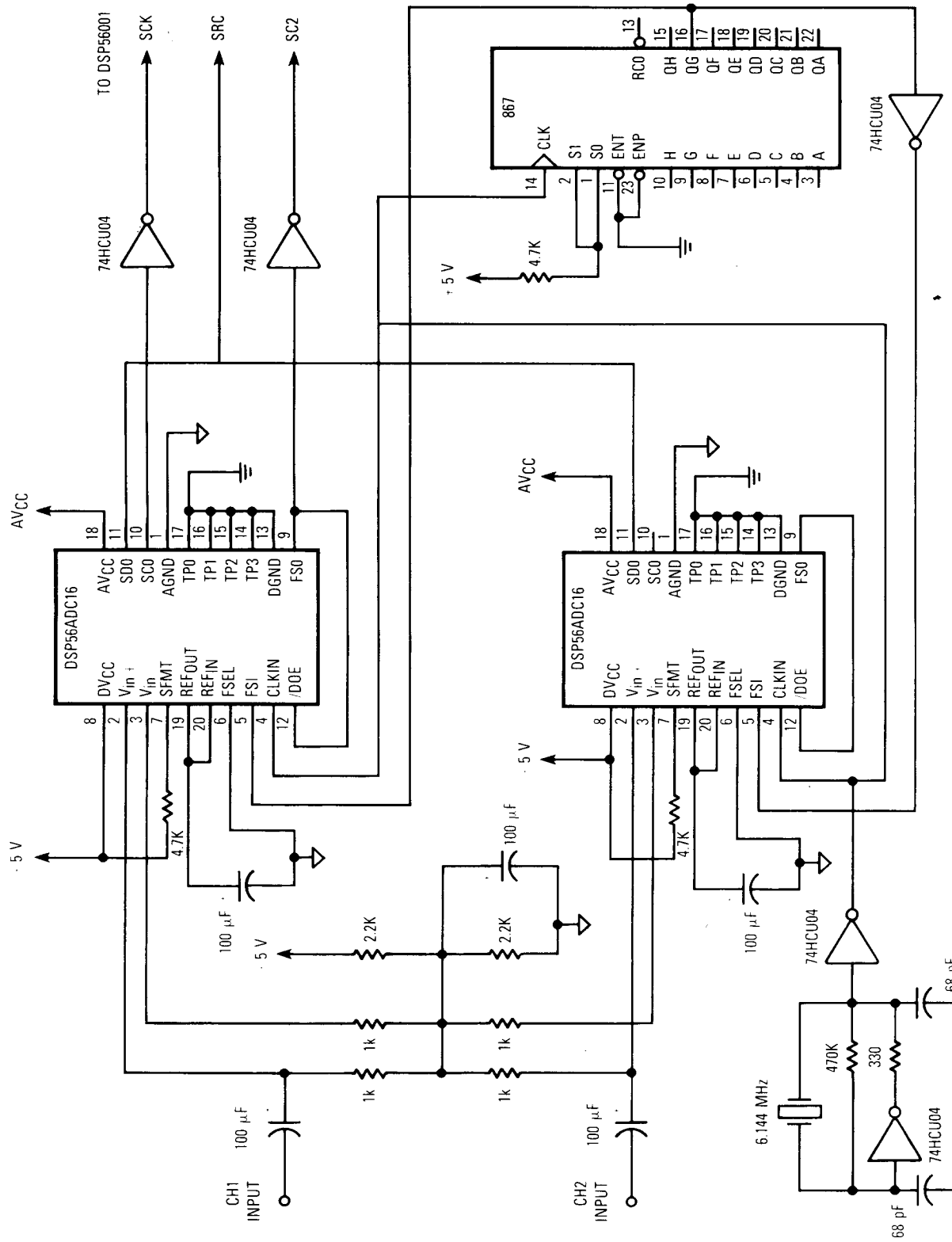


Figure 12(b). Schematic Diagram for Multiplexing Two DSP56ADC16s with the DSP56001

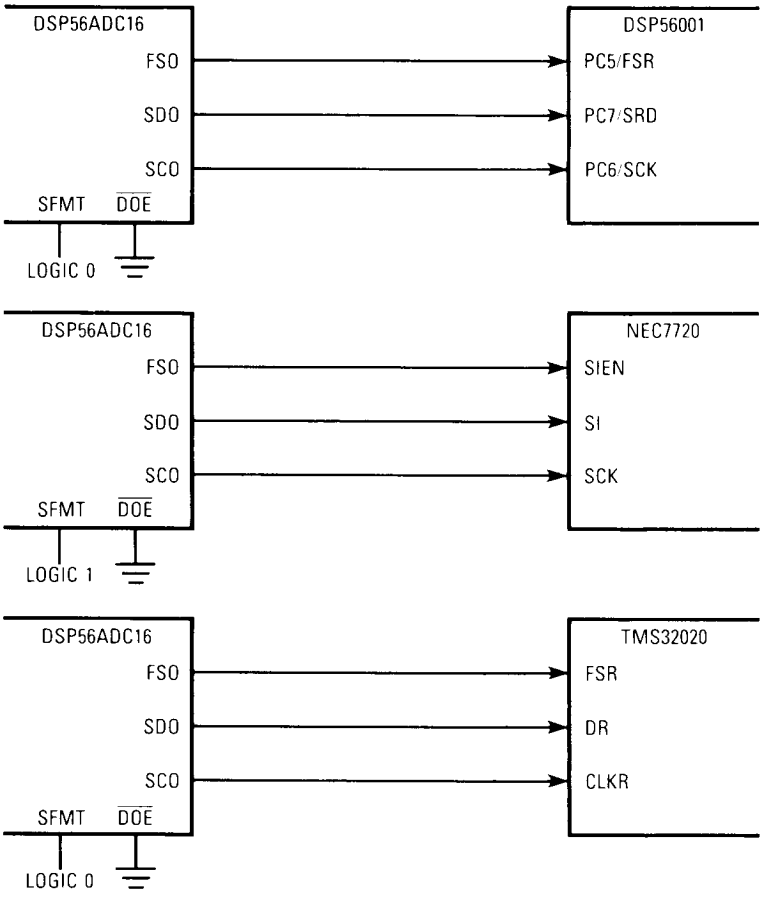


Figure 13. Connection Diagrams for Popular DPSs

MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Temperature Range	T_A	−40 to 85	C
Storage Temperature Range	T_{stg}	−55 to +150	C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Value	Unit
Thermal Resistance Plastic	θ_{JA}	70	°C/W

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = −40 to +85 C)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2.0	V_{CC}	V
Input Low Voltage	V_{IL}	−0.5	0.8	V
Input Leakage Current	I_{in}	—	1.0	μA
Hi-Z (OFF State) Input Current for SDO (V_{in} = 0.4 to 2.4 V)	I_{TSI}	—	10	μA
Output High Voltage (I_{OH} = −400 μA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OH} = 2 mA)	V_{OL}	—	0.5	V
Power Dissipation (V_{CC} = 5.5 V, f = 12.8 MHz, T_A = +85°C)	P_D	—	400	mW
Input Capacitance	C_{in}	—	10	pF

AC ELECTRICAL SPECIFICATIONS — CLOCK IN/OUT AND FRAME SYNC (V_{CC} = 5 V ± 10%, T_A = −40 to +85°C)

Characteristic	Symbol	Min	Max	Unit
Clock In Frequency (t_{clk} = 1/f)	f	1	12.8	MHz
Clock In Period	t_{clk}	78	100	ns
Clock Low Pulse Width at 12.8 MHz t_{clk}	t_{cl}	37	41	ns
Clock High Pulse Width at 12.8 MHz t_{clk}	t_{ch}	37	41	ns
Clock Low Pulse Width at 1 MHz t_{clk}	t_{cl}	475	525	ns
Clock High Pulse Width at 1 MHz t_{clk}	t_{ch}	475	525	ns
Duty Cycle	t_{PW}	0.473	0.525	t_{clk}
Rise and Fall Times	t_r, t_f	5	—	ns
Frame Sync Input Setup Time	t_{fsisu}	20	78	ns
Frame Sync Input Hold Time	t_{fsih}	20	*	ns
Serial Clock Output Delay Time	t_{scod}	30	75	ns
Serial Clock Output Period	t_{ckout}	156	312	ns

*The FSI input must be deasserted for at least two CLKIN periods prior to being asserted.

AC ELECTRICAL SPECIFICATIONS — FSO/SCO/SDO WHEN FSEL = 0 (V_{CC} = 5 V ± 10%, T_A = −40 to +85°C)

Characteristic	Symbol	Min	Max	Unit
Frame Sync Output Setup Time before Falling Edge of CLKIN	t_{fsckl}	130	—	ns
Frame Sync Output Hold Time after Falling Edge of CLKIN	t_{clklfs}	130	—	ns
Serial Data Output Setup Time	t_{dsu}	130	—	ns
Serial Data Output Hold Time	t_{dh}	130	—	ns
Frame Sync Output Setup Time before SCO Rising Edge	t_{fslckh}	130	—	ns
Frame Sync Output High to SCO Rising Edge	t_{fshckh}	130	—	ns
Delay from Frame Sync Input to Frame Sync Output	t_{fsifso}	5	—	cyc

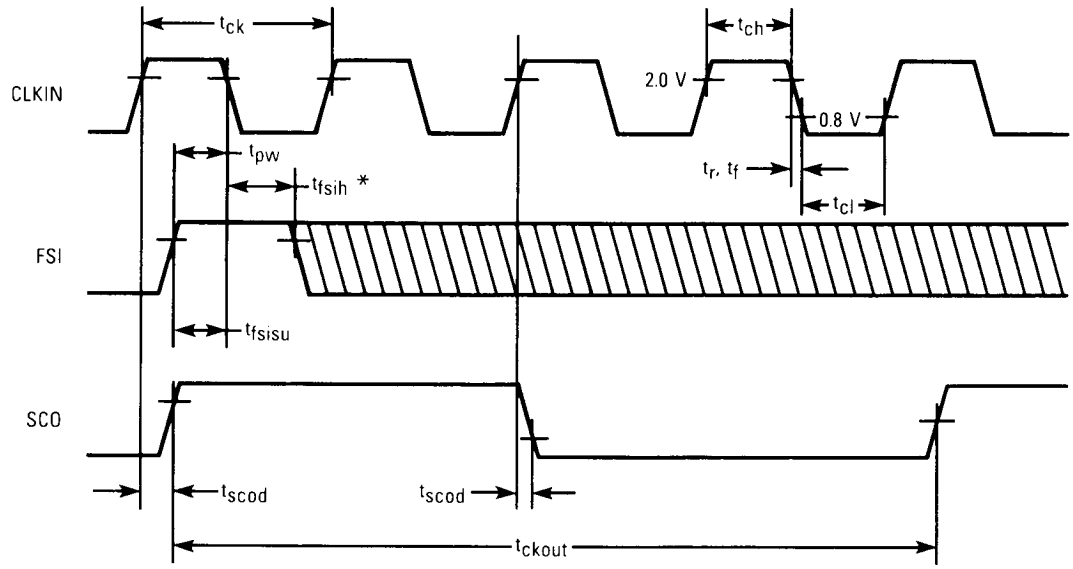
AC ELECTRICAL SPECIFICATIONS — FSO/SCO/SDO WHEN FSEL = 1 (V_{CC} = 5 V ± 10%, T_A = −40 to +85°C)

Characteristic	Symbol	Min	Max	Unit
Serial Data Output Setup Time	t_{sdosu}	40	—	ns
Serial Data Output Hold Time	t_{sdoh}	40	—	ns
Delay from Frame Sync Input to Fram Sync Output	t_{fsifso}	1	—	cyc

AC ELECTRICAL SPECIFICATIONS — $\overline{DOE}$ (V_{CC} = 5 V ± 10%, T_A = −40 to +85°C)

Characteristic	Symbol	Min	Max	Unit
Serial Data Output Enable Delay Time	t_{doedv}	0	20	ns
Serial Data Output Disable Delay Time	t_{doedz}†	0	20	ns

†t_{doedz} is three-state 500 mV from 2.4 V or 0.5 V level with C_L = 50 pF + 1 TTL load.



FIR FILTER OUTPUT MODE

*The FSI input must be deasserted for at least two CLKIN periods prior to being asserted.

Figure 14. Timing Diagram for CLKIN/FSI/SCO When FSEL = 0

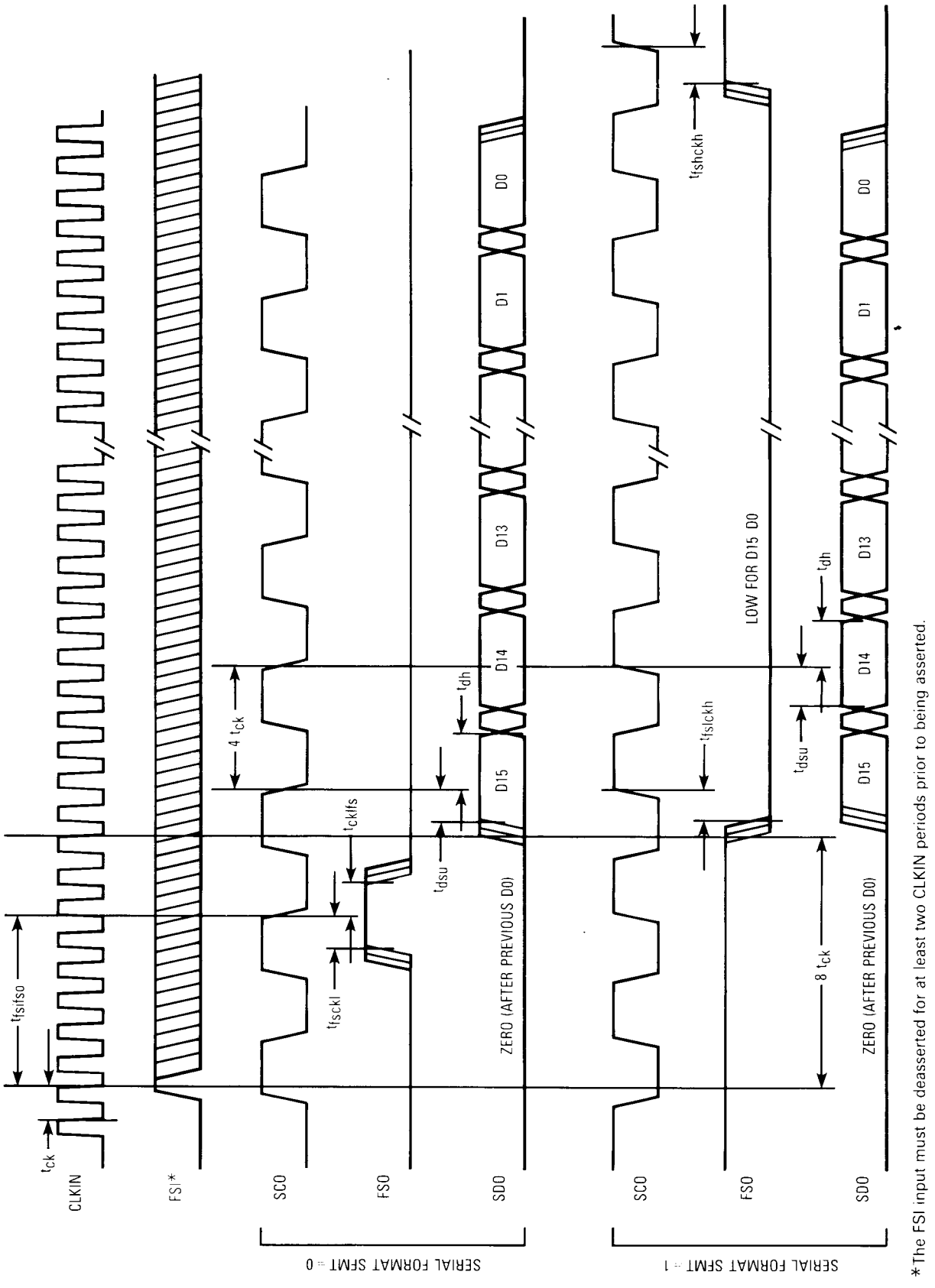


Figure 15(a). Timing Diagrams for FSO/SCO/SDO When FSEL = 0

*The FSI input must be deasserted for at least two CLKIN periods prior to being asserted.

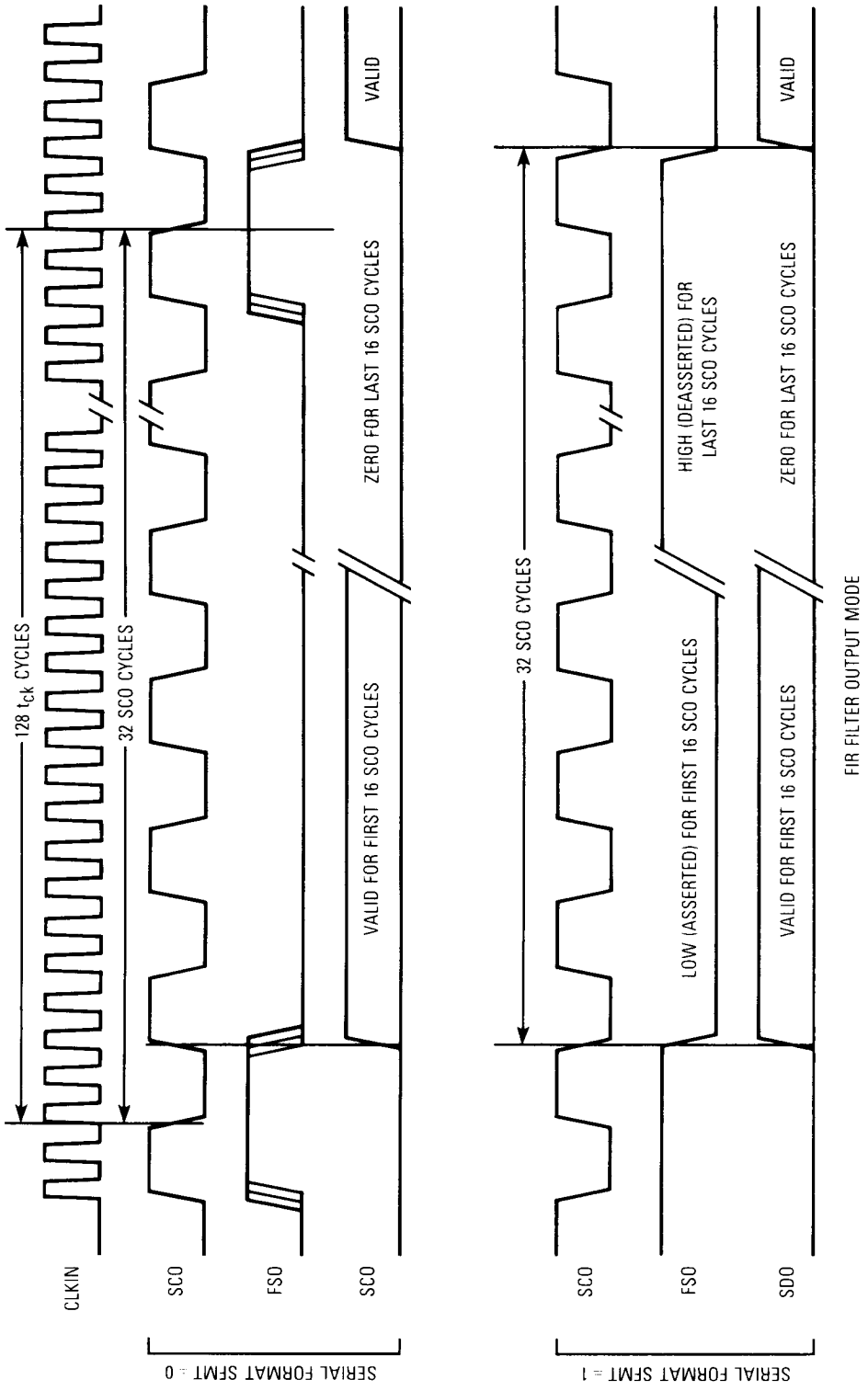
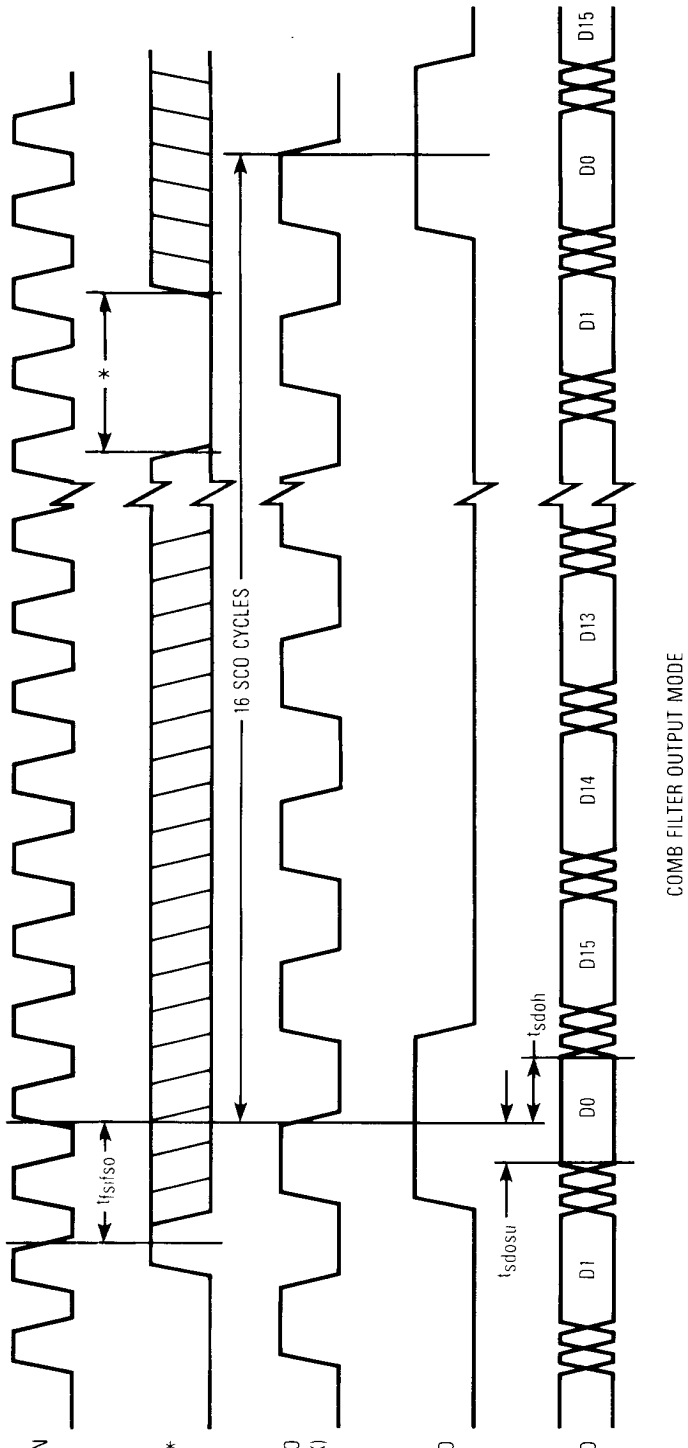


Figure 15(b). Timing Diagrams for FSO/SCO/SDO When FSEL = 0



* The FSI input must be deasserted for at least two CLKIN periods prior to being asserted.

Figure 16. Timing Diagrams for FSO/SCO/SDO When FSEL = 1

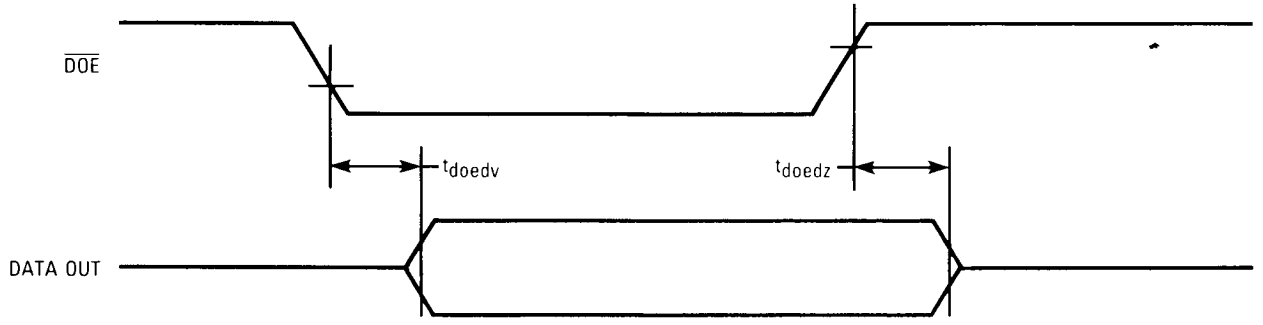
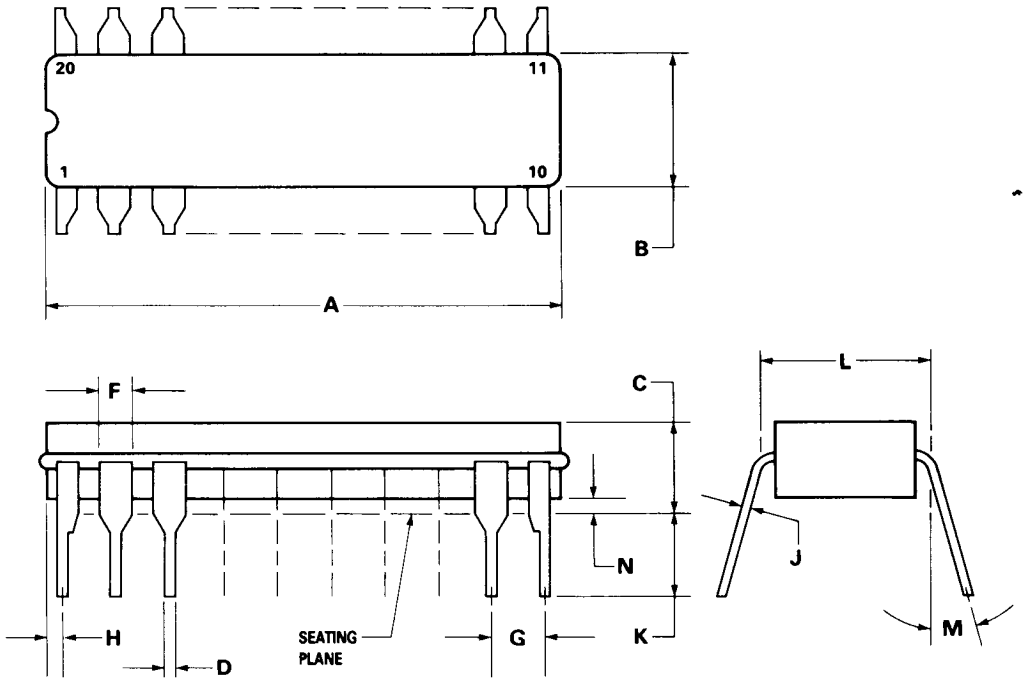


Figure 17. Timing Diagrams of $\overline{\text{DOE}}$ and Data Output

PACKAGE DIMENSIONS

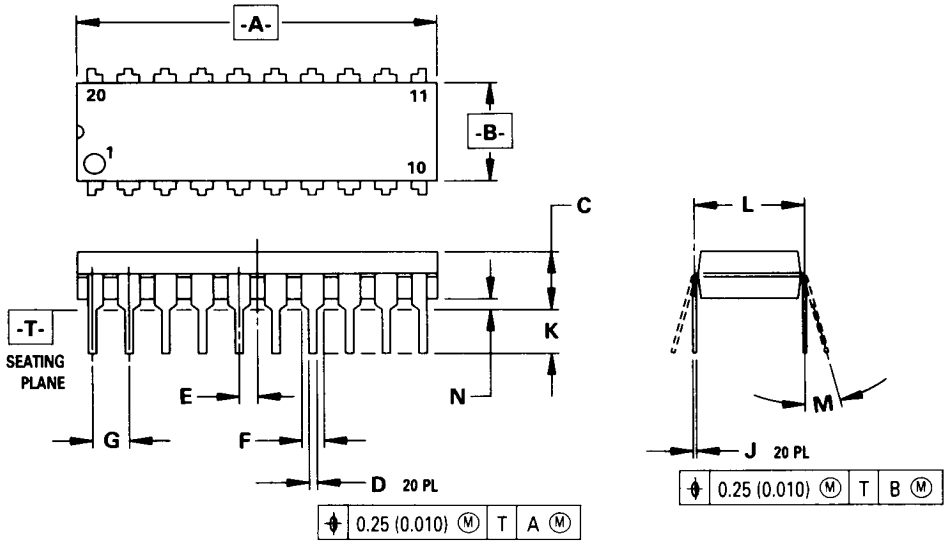
CERDIP PACKAGE
CASE 732-03



NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

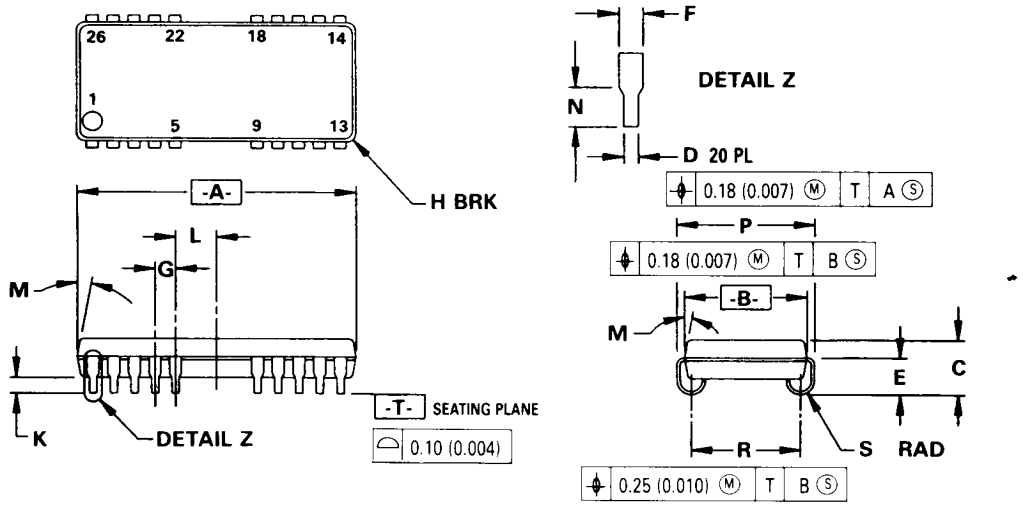
PLASTIC PACKAGE
CASE 738A-01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	24.39	24.89	0.960	0.980
B	7.12	7.49	0.280	0.295
C	3.69	4.44	0.145	0.175
D	0.39	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

SURFACE MOUNT PACKAGE
CASE 822-03



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	17.02	17.27	0.670	0.680
B	7.50	7.74	0.295	0.305
C	3.26	3.75	0.128	0.148
D	0.39	0.50	0.015	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
H	—	0.50	—	0.020
K	0.89	1.14	0.035	0.045
L	2.54 BSC		0.100 BSC	
M	0°	10°	0°	10°
N	0.89	1.14	0.035	0.045
P	8.39	8.63	0.330	0.340
R	6.61	6.98	0.260	0.275
S	0.77	1.01	0.030	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIM R TO BE DETERMINED AT DATUM -T-.
5. FOR LEAD IDENTIFICATION PURPOSES, PIN POSITIONS 6, 7, 8, 19, 20, & 21 ARE NOT USED.

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