



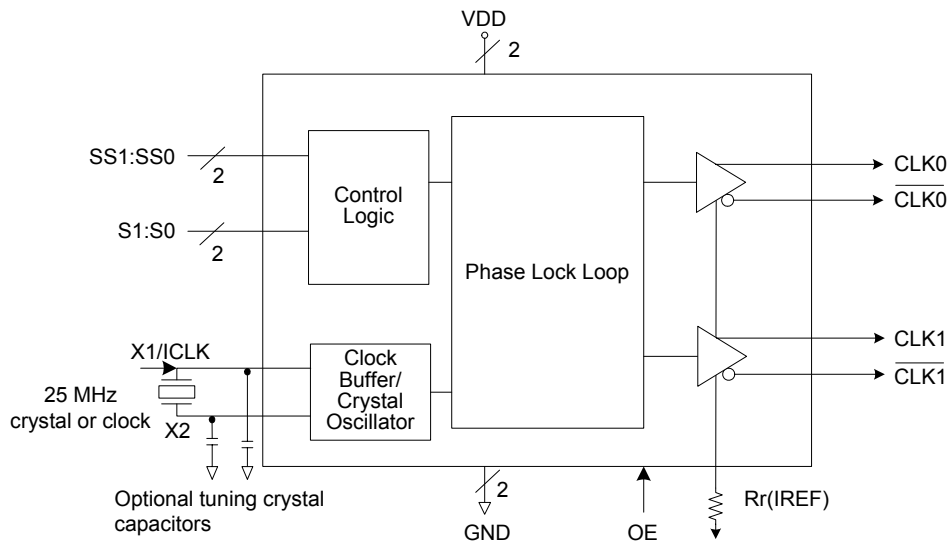
Description

The ICS557-03 is a spread spectrum clock generator supporting PCI-Express and Ethernet requirements. The device is used for PC or embedded systems to substantially reduce electromagnetic interference (EMI). The device provides two differential (HCSL) spread spectrum outputs. This device is pin configured to select spread and clock selection. Using ICS' patented Phase-Locked Loop (PLL) techniques, the device takes a 25 MHz crystal input and produces two pairs of differential outputs (HCSL) at 25 MHz, 100 MHz, 125 MHz and 200 MHz clock frequencies. It also provides spread selection of $\pm 0.25\%$, -0.5% , -0.75% , and no spread.

Features

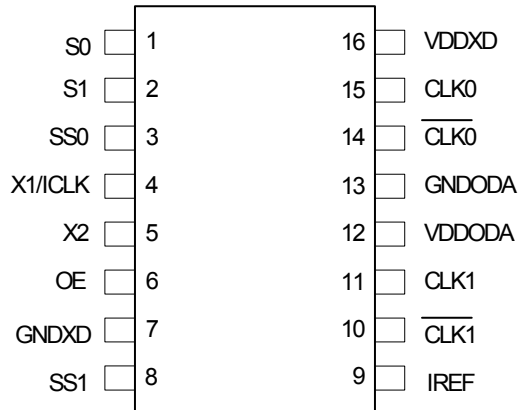
- Packaged in 16-pin TSSOP
- Available in Pb (lead) free package
- Supports LVDS Output Levels
- Operating voltage of 3.3 V
- Input frequency of 25 MHz
- Outputs (HCSL, 0.7 V Current mode differential pair)
- Jitter 100 ps (peak-to-peak)
- Spread of $\pm 0.25\%$, -0.5% , -0.75% , and no spread.
- Industrial and commercial temperature ranges

Block Diagram





Pin Assignment



16-pin (173 mil) TSSOP

Output Select Table 1(MHz)

S1	S0	CLK(1:0), CLK(1:0)
0	0	25M
0	1	100M
1	0	125M
1	1	200M

Spread Selection Table 2

SS1	SS0	Spread %
0	0	Center ±0.25
0	1	Down -0.5
1	0	Down -0.75
1	1	No Spread

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	S0	Input	Select pin 0. See Table1. Internal pull-up resistor.
2	S1	Input	Select pin 1. See Table 1. Internal pull-up resistor.
3	SS0	Input	Spread Select pin 0. See Table 2. Internal pull-up resistor.
4	X1/CLK	Input	Crystal or clock input. Connect to a 25 MHz crystal or single ended clock.
5	X2	Output	Crystal connection. Leave unconnected for clock input.
6	OE	Input	Output enable tri-states outputs and device is not shut down. Internal pull-up resistor.
7	GNDXD	Power	Connect to ground.
8	SS1	Input	Spread Select pin 1. See Table 2. Internal pull-up resistor.
9	IREF	Output	Precision resistor attached to this pin is connected to the internal current reference.
10	CLK1	Output	HCSL compliment clock output.
11	CLK1	Output	HCSL clock output.
12	VDDODA	Power	Connect to voltage supply +3.3 V for output driver and analog circuits
13	GNDODA	Power	Connect to ground.
14	CLK0	Output	HCSL compliment clock output.
15	CLK0	Output	HCSL clock output.
16	VDDXD	Power	Connect to voltage supply +3.3 V for crystal oscillator and digital circuit.

Applications Information

External Components

A minimum number of external components are required for proper operation.

Decoupling Capacitors

Decoupling capacitors of 0.01 μF should be connected between each VDD pin and the ground plane, as close to the VDD pin as possible. Do not share ground vias between components. Route power from power source through the capacitor pad and then into ICS pin.

Crystal

A 25 MHz fundamental mode parallel resonant crystal should be used. This crystal must have less than 300 ppm of error across temperature in order for the ICS557-03 to meet PCI Express specifications.

Crystal Capacitors

Crystal capacitors are connected from pins X1 to ground and X2 to ground to optimize the accuracy of the output frequency.

C_L = Crystal's load capacitance in pF

Crystal Capacitors (pF) = $(C_L - 8) * 2$

For example, for a crystal with a 16 pF load cap, each external crystal cap would be 16 pF. $(16-8)*2=16$.

Current Source (Iref) Reference Resistor - R_R

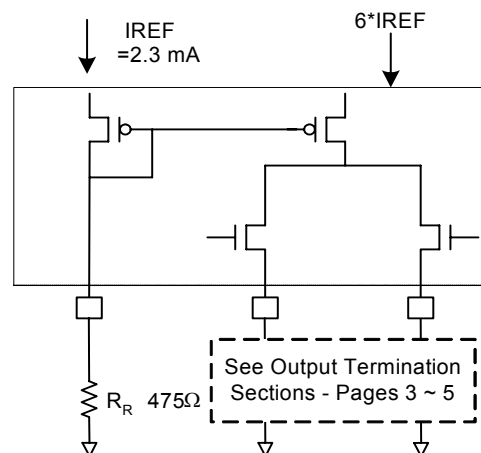
If board target trace impedance (Z) is 50 Ω , then $R_R = 475\Omega$ (1%), providing IREF of 2.32 mA. The output current (I_{OH}) is equal to 6*IREF.

Output Termination

The PCI-Express differential clock outputs of the ICS557-03 are open source drivers and require an external series resistor and a resistor to ground. These resistor values and their allowable locations are shown in detail in the **PCI-Express Layout Guidelines** section.

The ICS557-03 can also be configured for LVDS compatible voltage levels. See the **LVDS Compatible Layout Guidelines** section.

Output Structures



General PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1. Each 0.01 μF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible.
2. No vias should be used between decoupling capacitor and VDD pin.
3. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.
4. An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (any ferrite beads and bulk decoupling capacitors can be mounted on the back). Other signal traces should be routed away from the ICS557-03. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

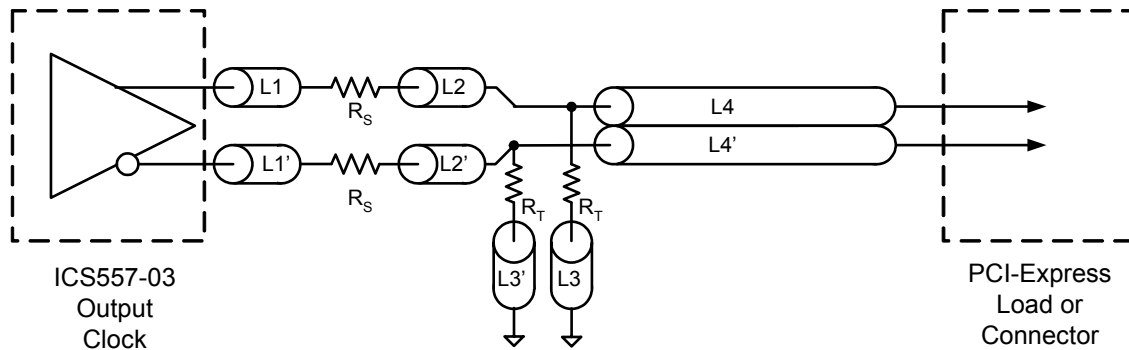
PCI-Express Layout Guidelines

Common Recommendations for Differential Routing	Dimension or Value	Unit
L1 length, Route as non-coupled 50 ohm trace.	0.5 max	inch
L2 length, Route as non-coupled 50 ohm trace.	0.2 max	inch
L3 length, Route as non-coupled 50 ohm trace.	0.2 max	inch
R_S	33	ohm
R_T	49.9	ohm

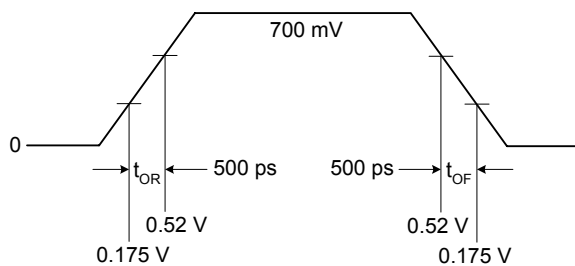
Differential Routing on a Single PCB	Dimension or Value	Unit
L4 length, Route as coupled microstrip 100 ohm differential trace.	2 min to 16 max	inch
L4 length, Route as coupled stripline 100 ohm differential trace.	1.8 min to 14.4 max	inch

Differential Routing to a PCI Express Connector	Dimension or Value	Unit
L4 length, Route as coupled microstrip 100 ohm differential trace.	0.25 to 14 max	inch
L4 length, Route as coupled stripline 100 ohm differential trace.	0.225 min to 12.6 max	inch

PCI-Express Device Routing



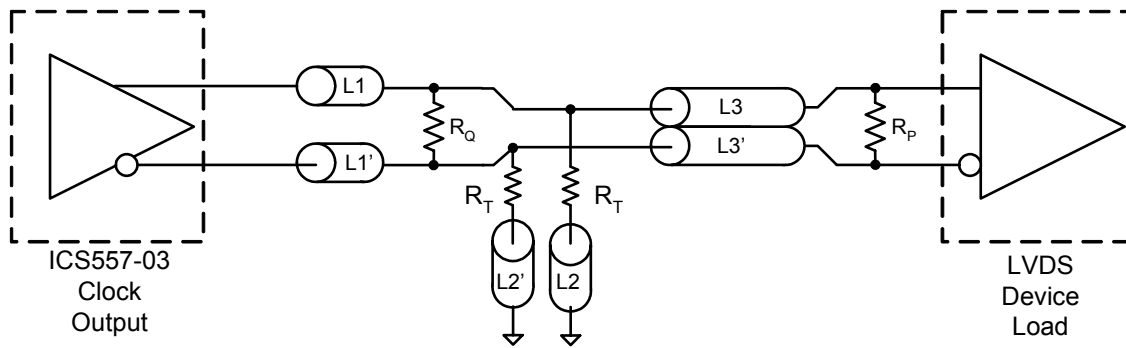
Typical PCI-Express (HCSL) Waveform



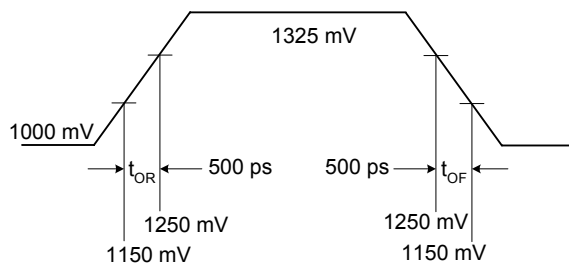
LVDS Compatible Layout Guidelines

LVDS Recommendations for Differential Routing	Dimension or Value	Unit
L1 length, Route as non-coupled 50 ohm trace.	0.5 max	inch
L2 length, Route as non-coupled 50 ohm trace.	0.2 max	inch
R_p	100	ohm
R_Q	100	ohm
R_T	150	ohm
L3 length, Route as coupled 50 ohm differential trace.		
L3 length, Route as coupled 50 ohm differential trace.		

LVDS Device Routing



Typical LVDS Waveform





Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS557-03. These ratings are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD, VDDA	5.5 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature (commercial)	0 to +70°C
Ambient Operating Temperature (industrial)	-40 to +85°C
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C
ESD Protection (Input)	2000 V min. (HBM)

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±10%**, Ambient Temperature -40 to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V		2.97	3.3	3.63	
Input High Voltage ¹	V _{IH}	S0, S1, OE, CLK, SS0, SS1	2.0		VDD +0.3	V
Input Low Voltage ¹	V _{IL}	S0, S1, OE, CLK, SS0, SS1	VSS-0.3		0.8	V
Input Leakage Current ²	I _{IL}	0 < Vin < VDD	-5		5	μA
Operating Supply Current	I _{DD}	50Ω, 2pF			65	mA
	I _{DDOE}	OE =Low			35	mA
Input Capacitance	C _{IN}	Input pin capacitance			7	pF
Output Capacitance	C _{OUT}	Output pin capacitance			6	pF
Pin Inductance	L _{PIN}				5	nH
Output Resistance	R _{OUT}	CLKOUT	3.0			kΩ
Pull-up Resistor	R _{PU}		100			kΩ

¹ Single edge is monotonic when transitioning through region.

² Inputs with pull-ups/-downs are not included.

**AC Electrical Characteristics - CLK0/CLK1, $\overline{\text{CLK0/CLK1}}$** Unless stated otherwise, **VDD=3.3 V \pm 10%**, Ambient Temperature -40 to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency				25		MHz
Output Frequency			25		200	MHz
Output High Voltage ^{1,2}	V _{OH}	Notes 1, 2	660	700	850	mV
Output Low Voltage ^{1,2}	V _{OL}	Notes 1, 2	-150	0		mV
Crossing Point Voltage ^{1,2}		Absolute, Notes 1, 2	250	350	550	mV
Crossing Point Voltage ^{1,2,4}		Variation over all edges, Notes 1, 2, 4			140	mV
Jitter, Cycle-to-Cycle ^{1,3}		Notes 1, 3		60		ps
Modulation Frequency		Spread spectrum	30	31.5	33	kHz
Rise Time ^{1,2}	t _{OR}	From 0.175 V to 0.525 V, Notes 1, 2	175	332	700	ps
Fall Time ^{1,2}	t _{OF}	From 0.525 V to 0.175 V, Notes 1, 2	175	344	700	ps
Rise/Fall Time Variation ^{1,2}		Notes 1, 2			125	ps
Skew between outputs		At VDD/2			50	ps
Duty Cycle ^{1,3}		Notes 1, 3	45		55	%
Output Enable Time ⁵		All outputs, Note 5		10		us
Output Disable Time ⁵		All outputs, Note 5		10		us
Stabilization Time	t _{STABLE}	From power-up VDD=3.3 V		3.0		ms
Spread Change Time	t _{SPREAD}	Settling period after spread change		3.0		ms

Note 1: Test setup is R_L=50 ohms with 2 pF, R_r = 475Ω (1%).

Note 2: Measurement taken from a single-ended waveform.

Note 3: Measurement taken from a differential waveform.

Note 4: Measured at the crossing point where instantaneous voltages of both CLK and $\overline{\text{CLK}}$ are equal.

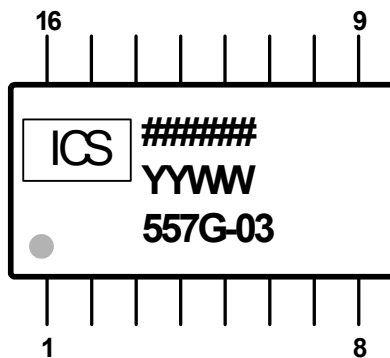
Note 5: CLK pins are tri-stated when OE is low asserted. CLK is driven differential when OE is high.



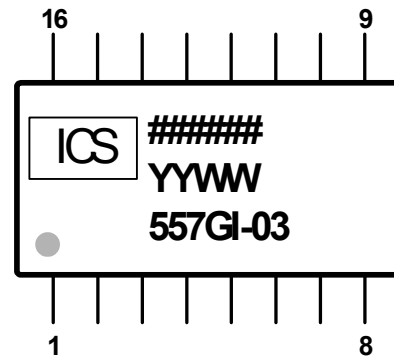
Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		78		$^{\circ}\text{C}/\text{W}$
	θ_{JA}	1 m/s air flow		70		$^{\circ}\text{C}/\text{W}$
	θ_{JA}	3 m/s air flow		68		$^{\circ}\text{C}/\text{W}$
Thermal Resistance Junction to Case	θ_{JC}			37		$^{\circ}\text{C}/\text{W}$

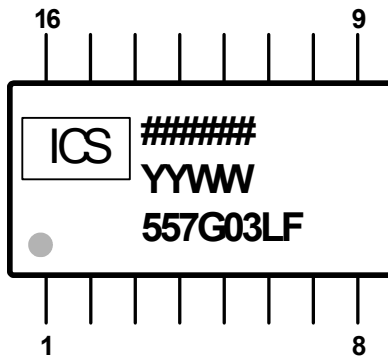
Marking Diagram (ICS557G-03)



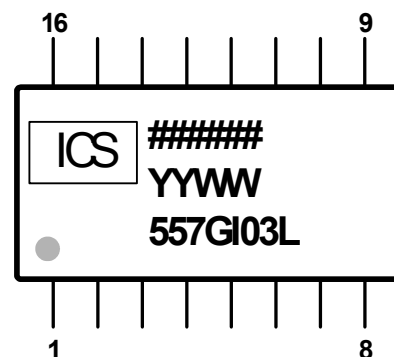
Marking Diagram (ICS557GI-03)



Marking Diagram (ICS557G-03LF)



Marking Diagram (ICS557GI-03LF)



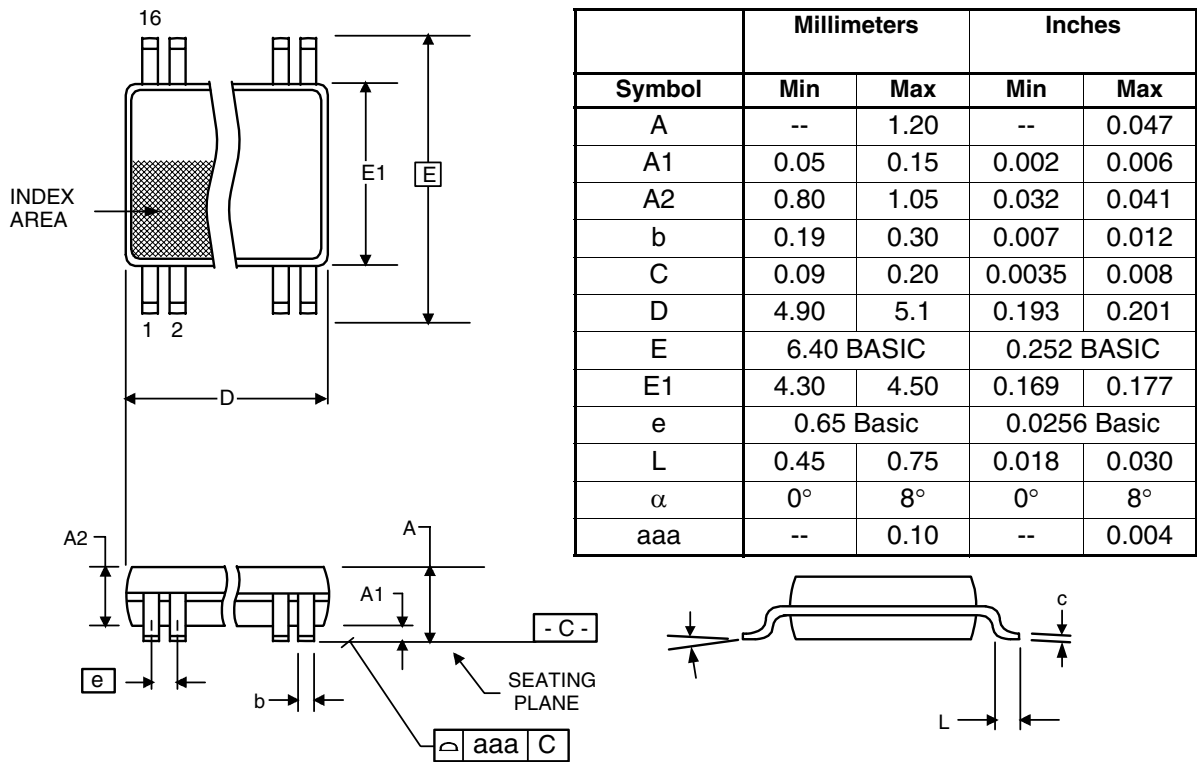
Notes:

1. ##### is the lot code.
2. YYWW is the last two digits of the year, and the week number that the part was assembled.
3. "LF" designates Pb (lead) free package.
4. "I" designates industrial temperature range.
5. Bottom marking: (origin). Origin = country of origin of not USA.



Package Outline and Package Dimensions (16-pin TSSOP, 173 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
ICS557G-03	See Page 8	Tubes	16-pin TSSOP	0 to +70° C
ICS557G-03T		Tape and Reel	16-pin TSSOP	0 to +70° C
ICS557G-03LF		Tubes	16-pin TSSOP	0 to +70° C
ICS557G-03LFT		Tape and Reel	16-pin TSSOP	0 to +70° C
ICS557GI-03	See Page 8	Tubes	16-pin TSSOP	-40 to +85° C
ICS557GI-03T		Tape and Reel	16-pin TSSOP	-40 to +85° C
ICS557GI-03LF		Tubes	16-pin TSSOP	-40 to +85° C
ICS557GI-03LFT		Tape and Reel	16-pin TSSOP	-40 to +85° C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

While the information presented herein has been checked for both accuracy and reliability, Integrated Circuit Systems (ICS) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by ICS. ICS reserves the right to change any circuitry or specifications without notice. ICS does not authorize or warrant any ICS product for use in life support devices or critical medical instruments.