PALC20RA10Z-40/45

T-46-13-47

CMOS Programmable Array Logic
Zero Standby Power/Electrically Erasable/Asynchronous ZPAL™ Device

DISTINCTIVE CHARACTERISTICS

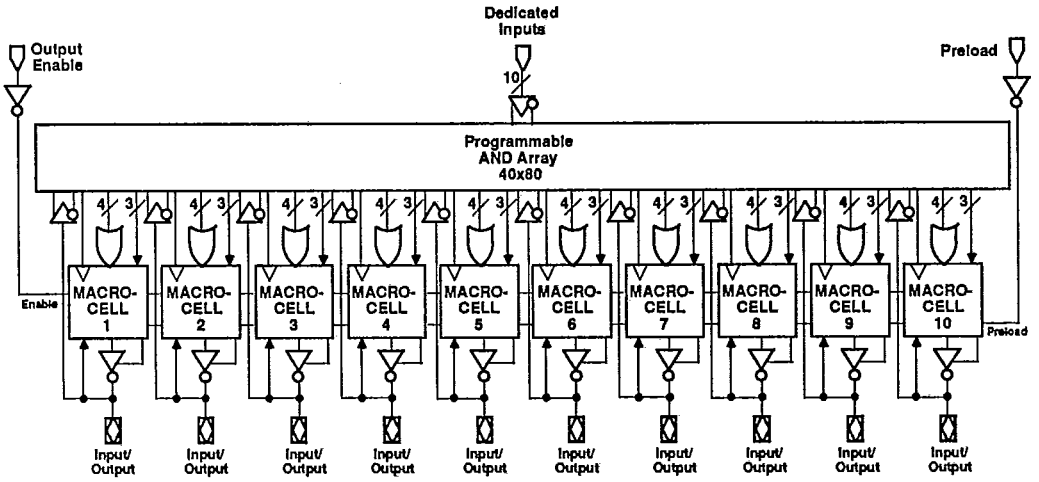
- CMOS technology provides zero standby power: 150 µA max
- Low CMOS operating power
- Electrically erasable in plastic SKINNYDIP and ceramic packages
- Electrically erasable feature provides highest programming and functional yields
- Reduces chip count by a factor of seven
- Programmable output polarity
- Individually programmable asynchronous clock, preset and reset
- Registers can be bypassed individually
- TTL-level register preload guarantees testability
- Special security bit for design secrecy
- Easy design with PALASM® 2 software
- Programmed on standard PAL® device programmers
- 24-pin SKINNYDIP® package saves space
- Available in commercial and industrial temperature ranges

GENERAL DESCRIPTION

The PALC20RA10Z device is a CMOS version of the bipolar 24-pin PAL20RA10. The PALC20RA10Z is built using a high performance double poly single metal 1.2 micron EEPROM technology optimized for programmable logic. A grounded substrate allows an extremely low standby current. Standby power consumption is typically less than 10 µA. Active power rises at less than 5 mA per MHz of operating frequency. Electrically erasable CMOS technology eliminates the need for windowed packages, lowering cost. Reprogrammability not only reduces development and field retrofit costs but also guarantees 100% testability and field programmability.

The PALC20RA10Z is a 24-pin registered asynchronous PAL device. It adds a new dimension to PAL device flexibility. In addition to the programmable output polarity and the register preload features, such additional features as programmable asynchronous preset and reset, individually programmable clock signals, and registers that can be bypassed individually provide flexibility which is unique to the PAL20RA10 architecture.

BLOCK DIAGRAM



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Publication #	Rev.	Amendment
10427	B	/0

Issue Date: July 1988

CONNECTION DIAGRAM
(Top View)

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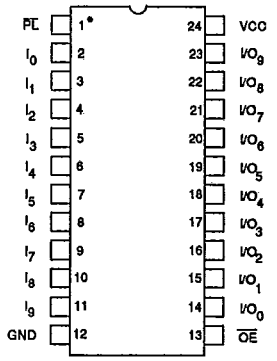
SKINNYDIP



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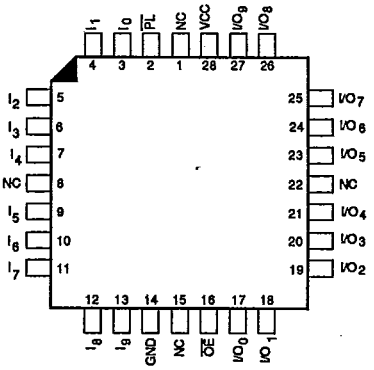
PLCC



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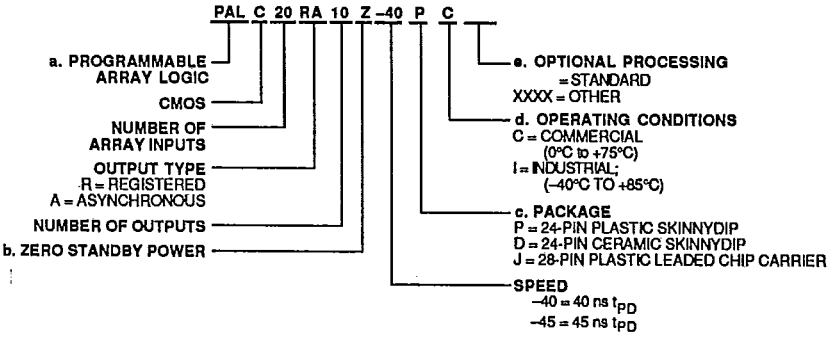
Pin Designations: I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
GND = Ground
NC = No Connection
$\overline{PL}$ = Preload
$\overline{OE}$ = Output Enable

Note: Pin 1 is marked for orientation

ORDERING INFORMATION
Standard Products

AMD/MMI standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:
a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
PALC20RA10Z-40	PC, DC, JC
PALC20RA10Z-45	PC, DC, JC PI, DI, JI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

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FUNCTIONAL DESCRIPTION

The PALC20RA10Z has ten dedicated input lines and ten programmable I/O macrocells. The Registered Asynchronous (RA) macrocell is shown in Figure 1. Pin 1 serves as global register preload and pin 13 serves as global output enable. Programmable output polarity is available to provide user-programmable output polarity for each individual macrocell.

The programmable functions in the PALC20RA10Z are automatically configured from the user's design specification, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.

RA CELL CONFIGURATION

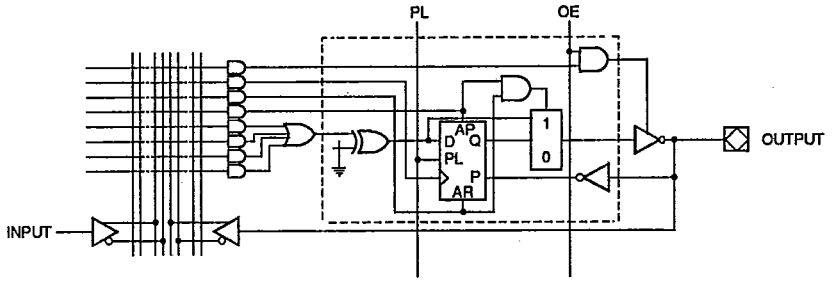


Figure 1. PALC20RA10Z Macrocell

Programmable Preset and Reset

In each macrocell, two product lines are dedicated to asynchronous preset and asynchronous reset. If the preset product line is HIGH, the Q output of the register becomes logic 1. If the reset product line is HIGH, the Q output of the register becomes a logic 0. The operation of the programmable preset and reset overrides the clock.

Bypass Mode/Registered Mode

If both the preset and reset product lines are HIGH, the flip-flop is bypassed (Bypass Mode) and the output becomes combinatorial. Otherwise, the output is from the register (Registered Mode). Each output can be configured to be combinatorial or registered.

Programmable Clock

The clock input to each flip-flop comes from the programmable array, allowing any flip-flop to be clocked independently if desired.

Three-State Outputs

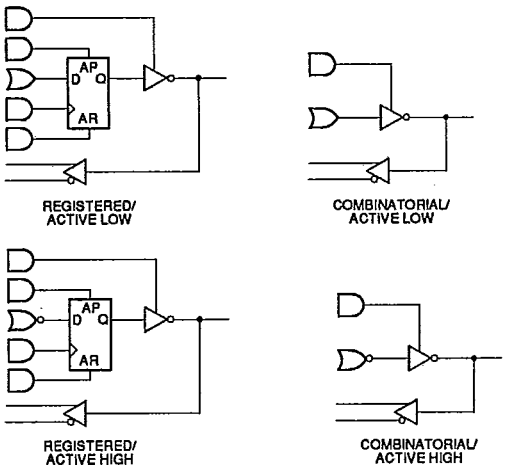
The devices provide a product term dedicated to local output control. There is also a global output control pin. The output is enabled if both the global output control pin is LOW and the local output control product term is HIGH. If the global output control pin is HIGH, all outputs will be disabled. If the local output control product term is LOW, then that output will be disabled.

Security Bit

A security bit is also provided to prevent unauthorized copying of PAL device patterns. Once the bit is programmed, the circuitry enabling verification is permanently disabled. With the verification not operating, it is impossible to simply copy the PAL device pattern on a PAL device programmer.

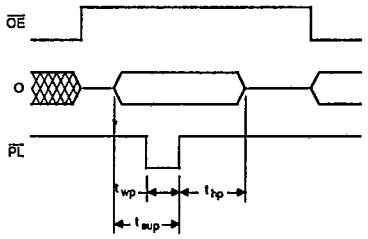
Programmable Polarity

The outputs can be programmed either active-LOW or active-HIGH. This is represented by the Exclusive-OR gate shown in the PALC20RA10Z logic diagram. When the output polarity is programmed, the lower input to the Exclusive-OR gate is HIGH, so the output is active-HIGH. Similarly when the output polarity bit is unprogrammed, the output is active-LOW. The programmable output polarity feature allows the user a higher degree of flexibility when writing equations.



Register Preload

Register preload allows any arbitrary state to be loaded into the PAL device output registers. This allows complete logic verification, including states that are impossible or impractical to reach. To use the preload feature, first disable the outputs by bringing $\overline{OE}$ HIGH, and present the data at the output pins. A LOW level on the preload pin ($\overline{PL}$) will then load the data into the registers.



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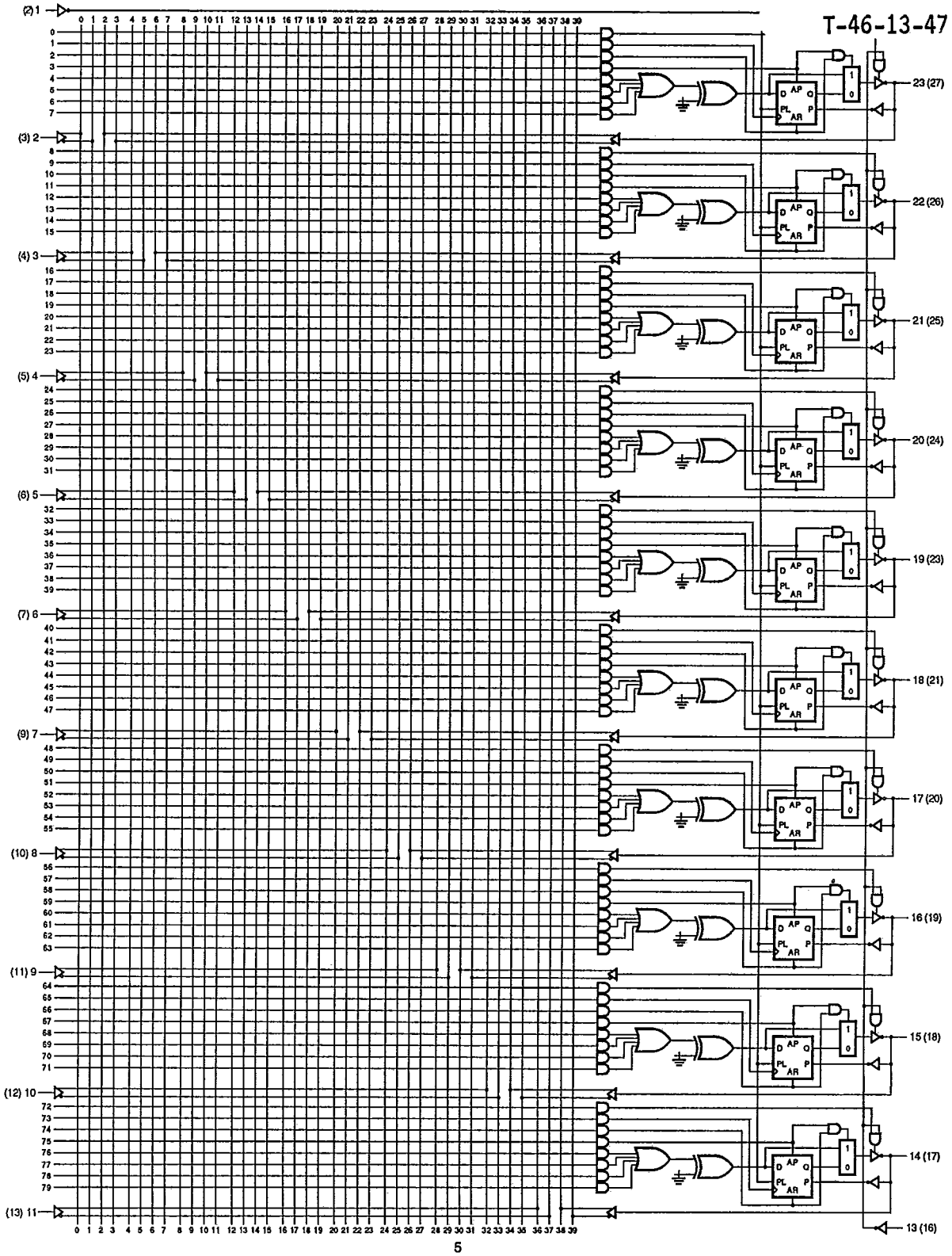
Programming and Erasing

The PALC20RA10Z can be programmed on standard logic programmers. Programmers approved by Advanced Micro Devices are listed on page 11. The PALC20RA10Z is automatically erased prior to programming.

If the user wants to erase the PALC20RA10Z but not program it to a new pattern, an empty Jedec file should be loaded.

CMOS PALC20RA10Z

Logic Diagram



DIP (PLCC) Pinouts

T-46-13-47

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC} ..... −0.5 V to 7 V
DC input voltage, V_I ..... −0.5 V to V_{CC} + 0.5 V
DC output voltage, V_O ..... −0.5 V to V_{CC} + 0.5 V
DC output source/sink current per output pin, I_O ..... ±35 mA
DC V_{CC} or ground current, I_{CC} or I_{GND} ..... ±100 mA
Input diode current, I_{IK}:
$V_I < 0$ ..... −20 mA
$V_I > V_{CC}$ ..... +20 mA
Output diode current, I_{OK}:
$V_O < 0$ ..... −20 mA
$V_O > V_{CC}$ ..... +20 mA
Storage temperature ..... −65°C to 150°C
Static discharge voltage ..... >2001 V
Latchup current ..... >100 mA
Ambient Temperature under Bias ..... −55°C to + 125°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

T-46-13-47

Commercial (C) Devices
Temperature (T_A) Operating Free Air ..... 0°C to +75°C
Supply voltage, V_{CC} ..... 4.75 V to +5.25 V
Industrial (I) Devices
Temperature (T_A) Operating Free Air ... −40°C to +85°C
Supply Voltage, V_{CC} ..... + 4.5 V to + 5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating conditions unless otherwise specified.

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{IL}	Low-level input voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0	0.8	V
V_{IH}	High-level input voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2	V_{CC}	V
I_{IL}	Low-level input current	V_{CC} = Max.	V_I = GND (Note 4)	−1		µA
I_{IH}	High-level input current	V_{CC} = Max.	$V_I = V_{CC}$ (Note 4)		1	µA
V_{OL}	Low-level output voltage	V_{CC} = Min.	I_{OL} = 8 mA		0.5	V
		V_{CC} = 5 V	I_{OL} = 1 µA		0.05	
V_{OH}	High-level output voltage	V_{CC} = Min.	I_{OH} = −4.0 mA	3.80		V
		V_{CC} = 5 V	I_{OH} = −1 µA	4.95		
I_{OZL}	Off-state output current	V_{CC} = Max.	V_O = GND (Note 4)	−10		µA
I_{OZH}			$V_O = V_{CC}$ (Note 4)		10	µA
I_{CC}	Standby supply current(Note 2)	I_O = 0 mA, V_I = GND or V_{CC}			150	µA
	Operating supply current(Note 3)	f = 1 MHz	I_O = 0 mA, V_I = GND or V_{CC}		25	mA

Note: 1. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. Disabled output pins = V_{CC} or GND.
3. Frequency of any input. See graph on page 9.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH})

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Unit
C_{IN}	Input capacitance(Note 1)	V_{IN} = 2.0 V at f = 1.0 MHz, V_{CC} = 5.0 V, T_A = 25°C	7	pF
C_{OUT}	Output capacitance(Note 1)	V_{OUT} = 2.0 V at f = 1.0 MHz, V_{CC} = 5.0 V, T_A = 25°C	8	

Note: 1. Sampled but not 100% tested.

SWITCHING CHARACTERISTICS over commercial and industrial operating range (Note 1, 2)

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Symbol	Parameter (note 2)		Commercial Only -40		Commercial and Industrial -45		Unit
			Min.	Max.	Min.	Max.	
t_{PD}	Input or feedback to output			40		45	ns
t_S	Setup time for input or feedback to clock		20		20		ns
t_H	Hold time		15		15		ns
t_{CO}	Clock to output or feedback			40		45	ns
t_{WP}	Preload pulse width		30		30		ns
t_{SUP}	Preload setup time		25		25		ns
t_{HP}	Preload hold time		25		25		ns
t_{AP}	Asynchronous Preset to Registered Output (note 3)			45		45	ns
t_{APW}	Asynchronous Preset Width		25		30		ns
t_{APR}	Asynchronous Preset Recovery Time		15		15		ns
t_{AR}	Asynchronous Reset to Registered Output (note 3)			45		45	ns
t_{ARW}	Asynchronous Reset Width		25		30		ns
t_{ARR}	Asynchronous Reset Recovery Time		15		15		ns
t_{WL}	Width of clock	LOW	20		20		ns
t_{WH}		HIGH	20		20		ns
f_{MAX}	Maximum frequency	External Feedback $1/(t_S + t_{CO})$	16.6		15.3		MHz
		No feedback $1/(t_{WL} + t_{WH})$	25		25		
t_{PZX}	Pin $\overline{OE}$ to output enable			25		30	ns
t_{PXZ}	Pin $\overline{OE}$ to output disable			25		30	ns
t_{EA}	Input to output enable (note 4)			40		45	ns
t_{ER}	Input to output disable (note 4)			40		45	ns

1. The PALC20RA10Z Series is designed to operate over the full military operating conditions. For availability and specifications, contact Advanced Micro Devices.
2. Test conditions (see Test Load) $R_1 = 440\ \Omega$. $R_2 = 190\ \Omega$
3. Minimum value of these parameters is guaranteed to be larger than t_H
4. Equivalent function to t_{PZX}/t_{PXZ} but using product term control.

PROGRAMMING CHARACTERISTICS

Symbol	Parameter	Value	Units	Test Conditions
t_{DR}	Min. Pattern Data Retention time	10	years	Max. storage temperature
N	Min. Reprogamming cycles	100	cycles	operating conditions

SWITCHING WAVEFORMS

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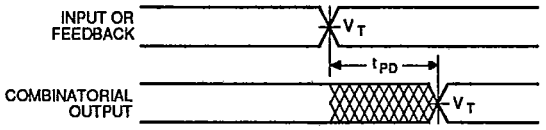

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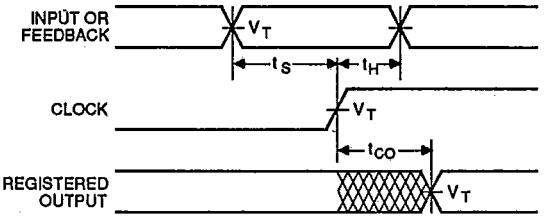
Combinatorial Output (Bypass Mode)



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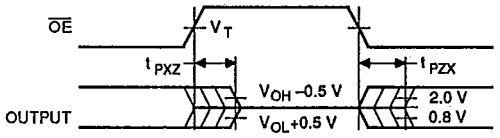
Registered Output (Registered Mode)



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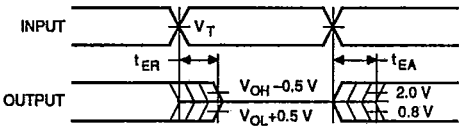
Pin $\overline{OE}$ to Output Disable/Enable



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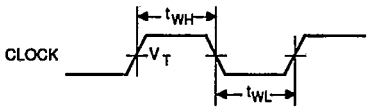
Input to Output Disable/Enable



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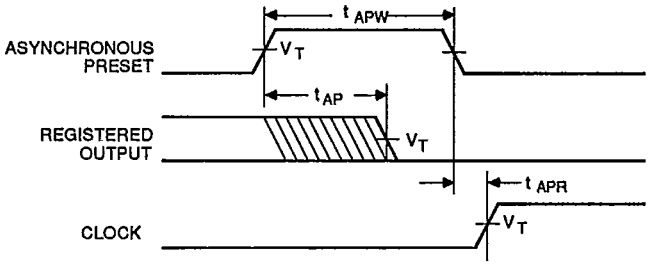
Clock Width



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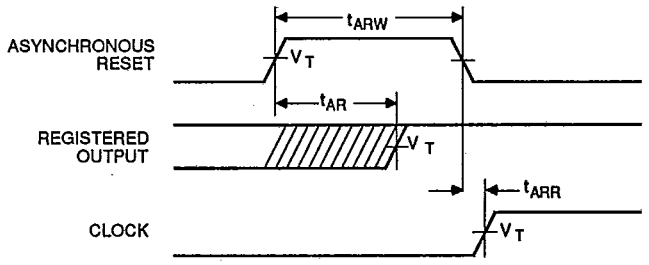
Asynchronous Preset



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Asynchronous Reset

SWITCHING TEST LOAD

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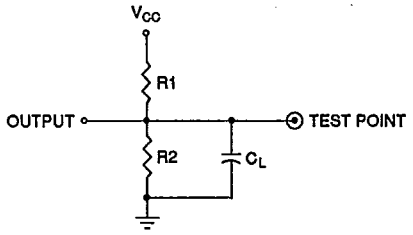

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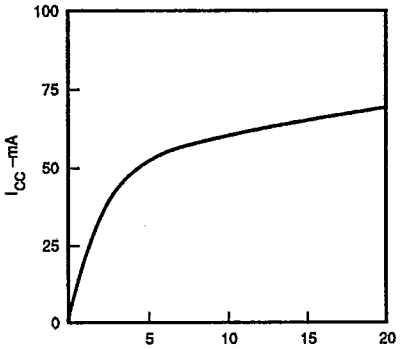
Specification	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}	50 pF	440Ω	190Ω	1.5V
t_{PZX}, t_{EA}	50 pF	440Ω	190Ω	Z->H: 2.0 V Z->L: 0.8 V
t_{PXZ}, t_{ER}	5 pF	440Ω	190Ω	H->Z: V_{OH} – 0.5 V L->Z: V_{OL} + 0.5V

I_{CC} VS. FREQUENCY

TYPICAL: V_{CC} = 5 V, T_A = 25°C



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KEY TO TIMING DIAGRAMS

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE: CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

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Notes:
1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2–5 ns typical

f_{MAX} Parameters

The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified in this case for two types of synchronous designs.

The first type of design is a *state machine with feedback signals* sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "$f_{MAX,\ External\ Feedback}$."

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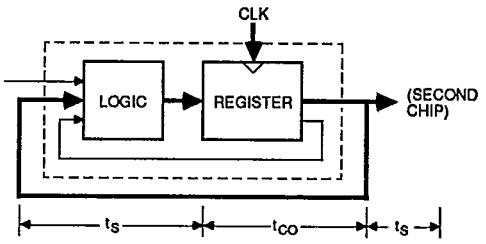
The second type of design is a *simple data path application.* In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). However, a lower limit for the period of each f_{MAX} type is the minimum clock period ($t_{WH} + t_{WL}$). Usually, this minimum clock period determines the period for the third f_{MAX}, designated "$f_{MAX,\ No\ Feedback}$."



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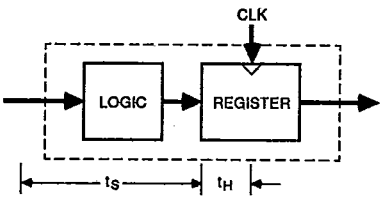
$f_{MAX,\ External\ Feedback}$; $1/(t_S + t_{CO})$



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$f_{MAX,\ No\ Feedback}$; $1/(t_S + t_H)$ or $1/(t_{WH} + t_{WL})$

Programmers/Development Systems (Subject to change)

T-46-13-47

Manufacturer	Programmer Configuration
Adams MacDonald 800 Airport Road. Monterey, CA 93940 (408) 373-3607	Contact programmer manufacturer
Data I/O Corporation 10525 Willows Road NE P.O. Box 97046 Redmond, WA 98073-9746 (800) 247-5700	System 29A, 29B LogicPak™ 303A-V04 Adapter 303A-011-V06 Family/Pinout Code: DE-45
Digelec Inc. 22736 Vanowen St. Canoga Park, CA 91307 (800) 367-8750 Or (818) 887-3755	Contact programmer manufacturer
Kontron Electronics Inc. 630 Clyde Ave. Mountain View, CA 94039-7230 (800) 227-8834	Contact programmer manufacturer
Logical Devices 1201 N.W. 65th Pl. Fort Lauderdale, FL 33309 (800) 331-7766	Contact programmer manufacturer
Micropross Parc d'Activite des Pres 5, rue Denis-Papin 59650 Villeneuve-d'Ascq (20) 47 90 40	Contact programmer manufacturer
Stag Microsystems Inc. 1600 Wyatt Dr., Suite 3 Santa Clara, CA 95054 (408) 988-1118	Contact programmer manufacturer
Storey Systems 3201 N. Hwy 67, Suite E Mesquite, TX 75150 (214) 270-4135	Contact programmer manufacturer
Structured Design 333 Cobalt Way, Suite 107 Sunnyvale, CA 94086 (408) 988-0725	Contact programmer manufacturer
Varix Corporation 1210 E. Campbell Rd., Suite 100 Richardson, TX 75081 (214) 437-0777	Contact programmer manufacturer

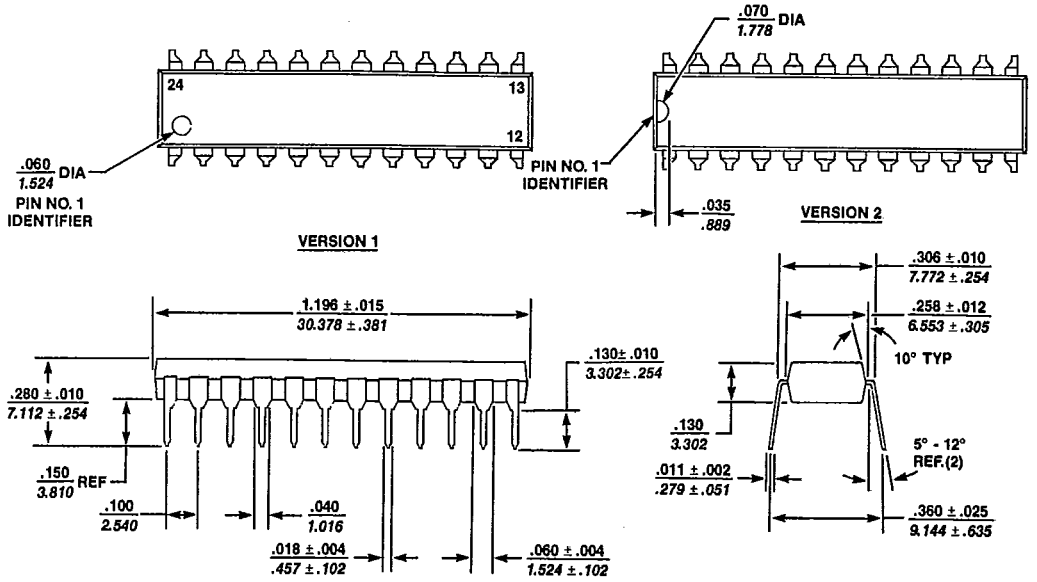
Manufacturer	Software Development System
Advanced Micro Devices 901 Thompson Place Sunnyvale, CA 94088 (800) 222-9323	PALASM®2 Software, rev. 2.18 and later
Data I/O Corporation 10525 Willows Road NE, P.O. Box 97046 Redmond, WA 98073-9746 (800) 247-5700	ABEL™ Software, rev. 2.0 and later
Personal CAD Systems Assisted Technology Division 1290 Parkmoor Ave. San Jose, CA 95126 (408) 971-1300	CUPL™ Software, rev. 2.02 b

LogicPak™ and ABEL™ are trademarks of Data I/O Corporation.
CUPL™ is a trademark of Personal CAD Systems.

PACKAGE DRAWING

T-46-13-47

24-Pin Plastic SKINNYDIP
1/4" X 1 3/16"

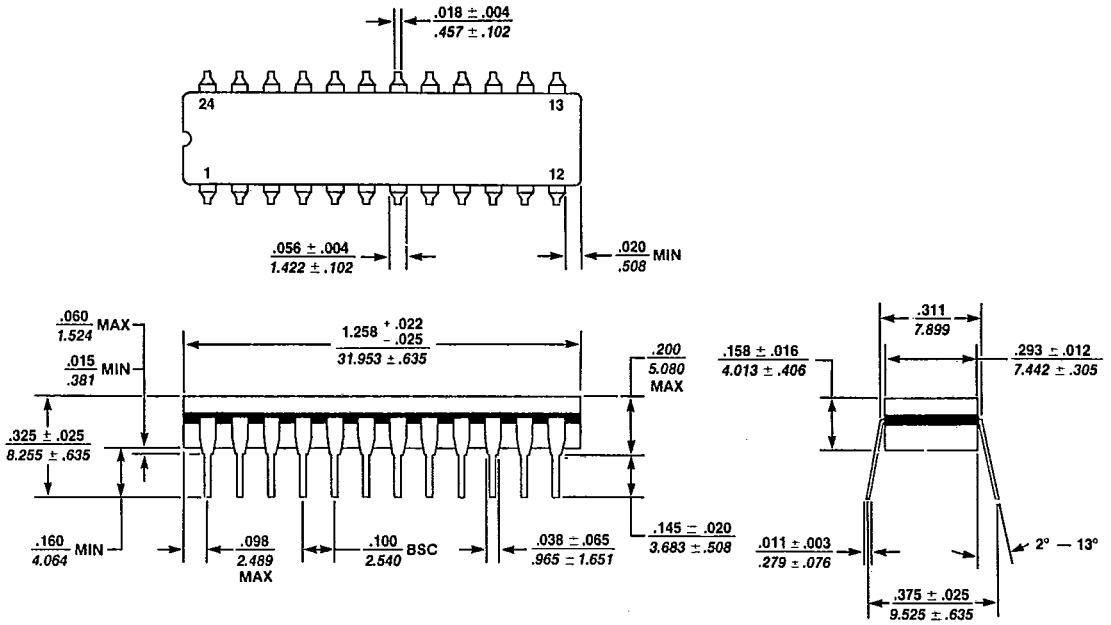


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

PACKAGE DRAWING

T-46-13-47

24-Pin Ceramic SKINNYDIP
(5/16" X 1-1")



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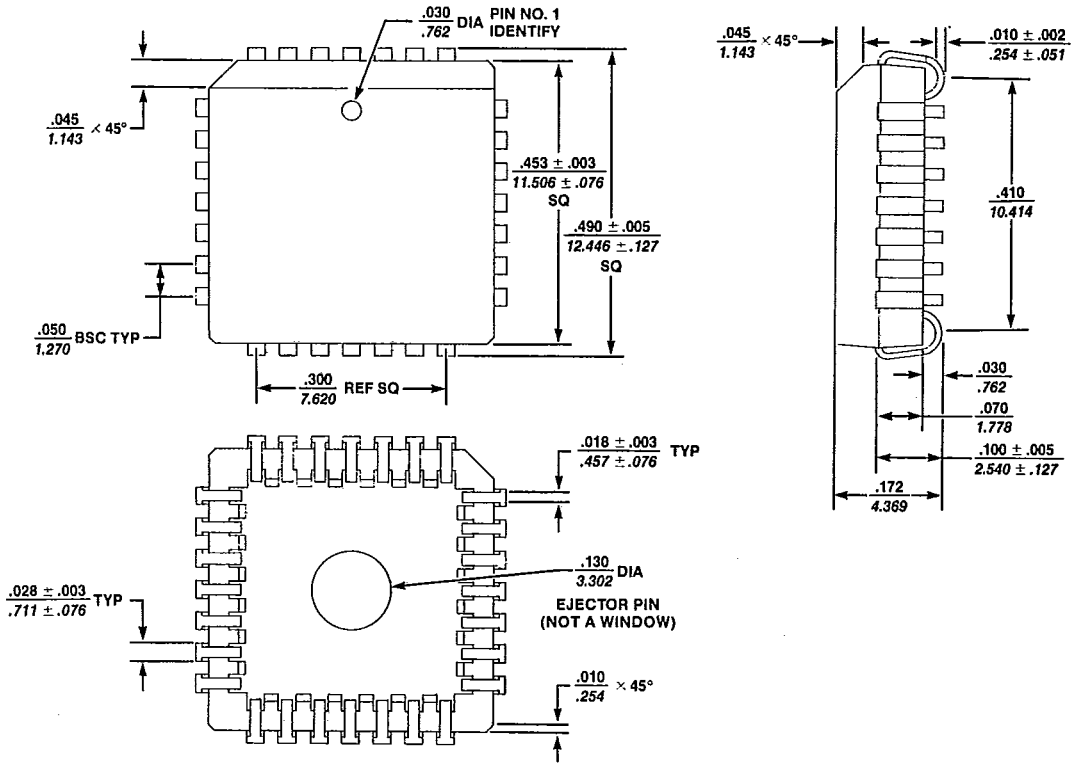
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

PACKAGE DRAWING

T-46-13-47

28-Pin Plastic Leaded Chip Carrier
.451" X .451"



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