NEC

MOS INTEGRATED CIRCUIT

μPD6700

FIP STATIC DISPLAY DRIVER
CMOS LSI

DESCRIPTION

μPD6700 is a CMOS display driver which can directly drive a static display fluorescent indicator panel (FIP). It is a small 56 pin flat package and composed of a 48 bit shift register, latch circuit, dimmer circuit and LED dot driver. It is optimum for a static display driver for fluorescent indicator panel (FIP) use, such as a counter display in compact disk (CD) player as well as a frequency display and a clock display in automotive audio system.

FEATURES

- A small 56 pin Flat package (0.8 mm pin pitch) capable of easily installing in front panel of automotive audio system.
- 2 power sources
  Power for Logic use (LED driver): V_{DD} = 5 V ± 10 %
  Power for display driver (FIP driver): V_{DD} to 18 V
- FIP drive by only positive power (V_{FIP} = 18 V MAX.)
- Direct connection with FIP (CMOS Push-pull output: No use of external resistances)
- Dimmer control (by ON/OFF terminal)
- Built-in power-on reset circuit (the display automatically turns out reset)
- Powerful segment output (47 segments MAX.): 1 mA TYP./seg.
- Dot display of 10 points by LED (selected by LED/FIP terminal): 15 mA TYP./seg.
  At LED/FIP = 1, it is capable of dot display of 10 points in addition to 37 FIP segment display (and capable of lighting MAX. 3 points at the same time).
- Cascade connection (with data output terminal)
  Easy control by microprocessor incorporating a serial interface function (data transmission per 8-bit unit)

ORDERING INFORMATION

Part Number	Package	Quality Grade
μPD6700GH-3B7	56-pin plastic QFP (10 × 14)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

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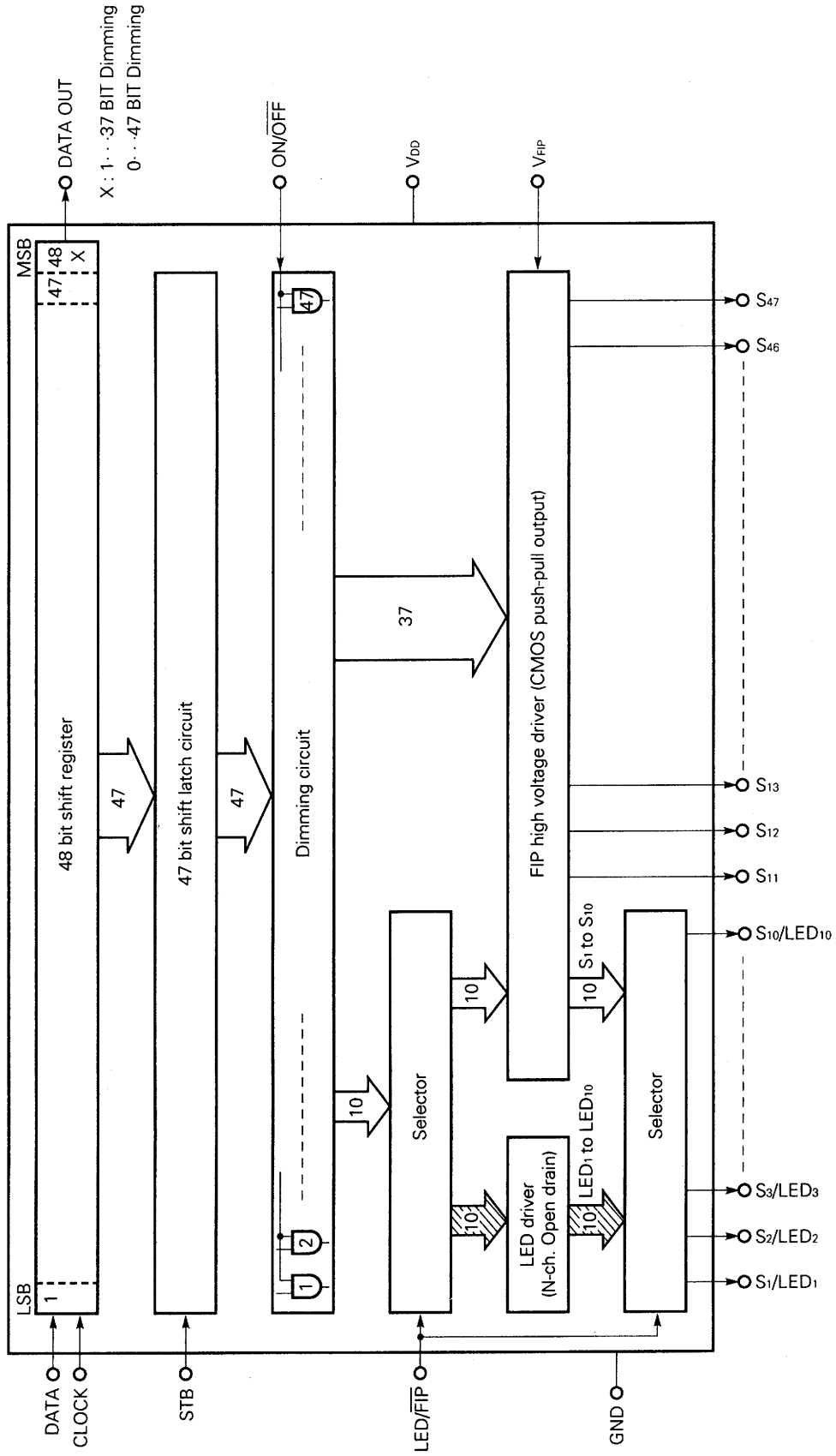
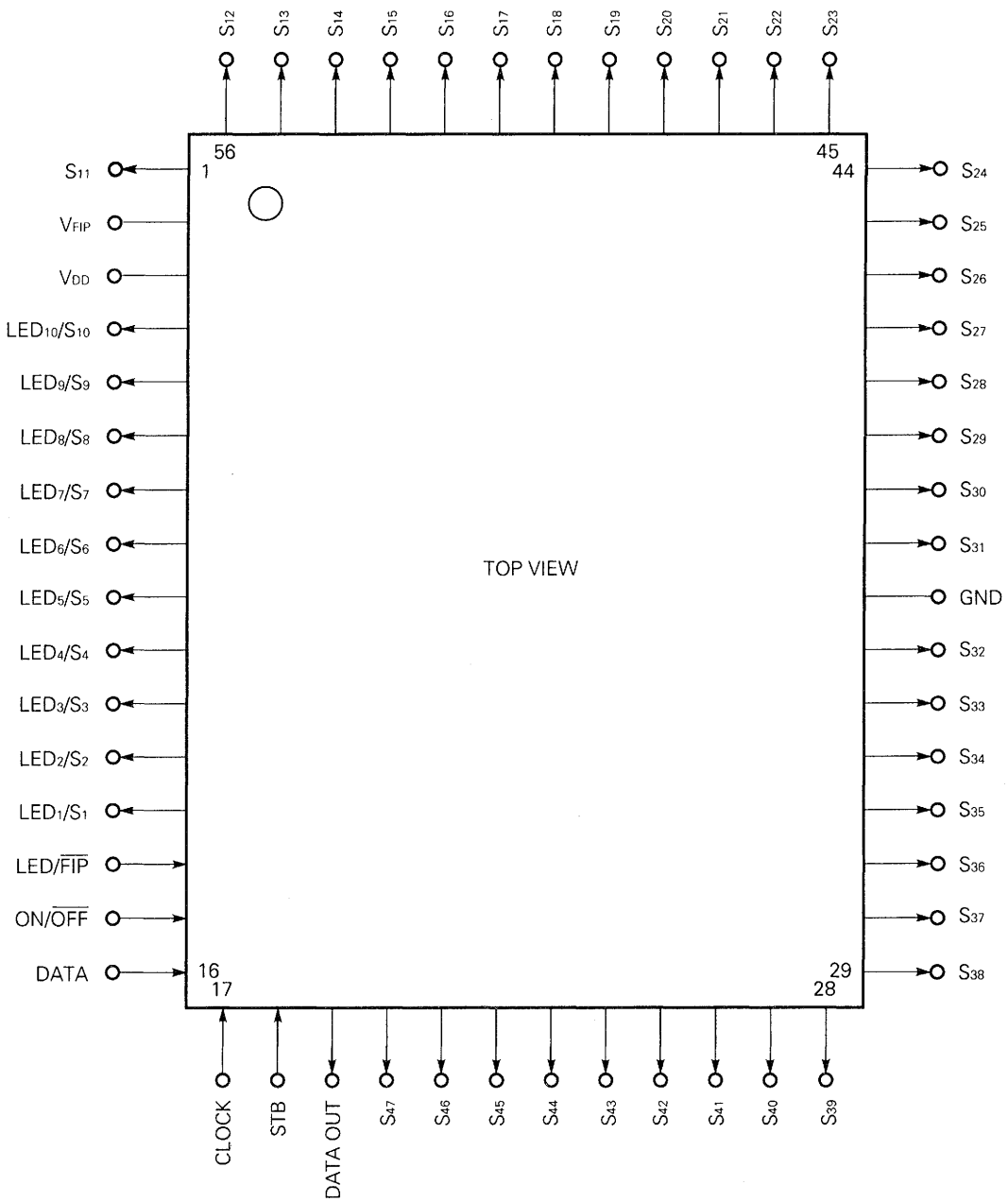
BLOCK DIAGRAM



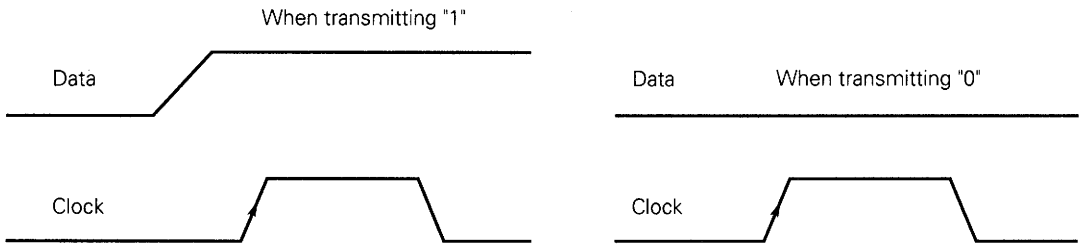
PIN CONNECTION DIAGRAM (Top View)



EXPLANATION OF MAIN PIN FUNCTION

- DATA/CLOCK : Pin 16/17

  These are data input Pins to shift resister. At the rising edge of clock Pin 17, data are shifted by one bit.



  Display data are shifted from the 48th bit in order, and data transmission finishes when the 1st bit (LSB) Display datum is transmitted.

  If display is changed, 48-bits data and clocks shall be transmitted necessarily.

- STB : PIN 18

  At the rising edge of STB Pin 18, Shift register (48 bits) data and clocks are transmitted to Latch circuit and display are performed.

  When Pin 18 is between high level and low, Latch circuit holds previous data regardless of Shift register data.

  Therefore, it is not until Pin 18 changes low to high that Display data change.

- LED/$\overline{\text{FIP}}$: PIN 14

  It is a selection Pin which switches all of 47 driver Pins to FIP driver or a part (10) of them to LED driver.

  High Level ..... 10 LED (S_1 to S_{10}) Drivers and 37 FIP Drivers

  Low Level ..... (S_1 to S_{47}) All FIP drivers

- ON/$\overline{\text{OFF}}$: PIN 15

  While this Pin is high, Display data are output.

  While low, output is off.

  This Pin is used as dimming by PWM signal input.

- DATA OUT : PIN 19

  This is a cascade-connection Pin, capable of connecting with another μPD6700GH's data input.

  (Cautions)

  To prevent latch up break down, the power should be turned ON in the order, V_{DD}, logic signal, V_{FIP}. It should be turned OFF in the opposite order.

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

PARAMETER	SYMBOL	RATINGS	UNIT	TEST CONDITIONS
Power supply voltage	V_{DD}	−0.3 to +6.0	V	
FIP drive voltage	V_{FIP}	−0.3 to +20	V	
Input voltage	V_I	−0.3 to V_{DD} +0.3	V	
Output current	I_{OLED}	25	mA	LED drive port
Output current High	I_{OH1}	−10	mA	FIP drive port
Output current Low	I_{OL}	+10	mA	FIP drive port
Output current High	I_{OH2}	−50	mA	Total FIP drive port
Power Consumption	P_D	300	mW	
Operating Temperature	T_{opt}	−40 to +85	°C	
Storage Temperature	T_{stg}	−55 to +125	°C	

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Power supply voltage	V_{DD}	4.5	5.0	5.5	V	
FIP drive voltage	V_{VIP}	V_{DD}	12	18	V	
Input voltage High	V_{IH}	0.7 V_{DD}		V_{DD}	V	DATA, CLOCK, STB, LED/FIP, ON/OFF
Input voltage Low	V_{IL}	0		0.3 V_{DD}	V	DATA, CLOCK, STB, LED/FIP, ON/OFF
LED port output current	I_{OLED}		10	20	mA	
FIP port output current	I_{OFIP}		0.5	1.0	mA	
V_{DD} rising time	t_{Ur}			200	MS	from V_{DD} = 0 V to 0.7 V_{DD}

ELECTRICAL CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 5 V ± 10 %, V_{FIP} = 15 V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Output voltage 1 High	V_{OH1}	V_{FIP}−1.0	V_{FIP}−0.4		V	S_1 to S_{47}, I_O = −1 mA
Output voltage 2 High	V_{OH2}	V_{DD}−0.5	V_{DD}−0.2		V	DATA OUT, I_O = −0.5 mA
Output voltage 1 Low	V_{OL1}		0.2	0.5	V	S_1 to S_{47}, I_O = 1 mA
Output voltage 2 Low	V_{OL2}		0.2	0.5	V	DATA OUT, I_O = 0.5 mA
Output voltage 3 Low	V_{OL3}		1.0	1.4	V	LED_1 to LED_{10}, I_O = 20 mA
Input leak current	I_I			±10	μA	DATA, CLOCK, STB, ON/OFF, LED/FIP, V_I = V_{DD} or Vss
Output leak current 1	I_{LO1}			±10	μA	LED_1 to LED_{10}, V_O = 0 V
Output leak current 2	I_{LO2}			±10	μA	LED_1 to LED_{10}, V_O = 5 V
Supply current	I_{DD}			0.1	mA	V_I = V_{DD} or Vss

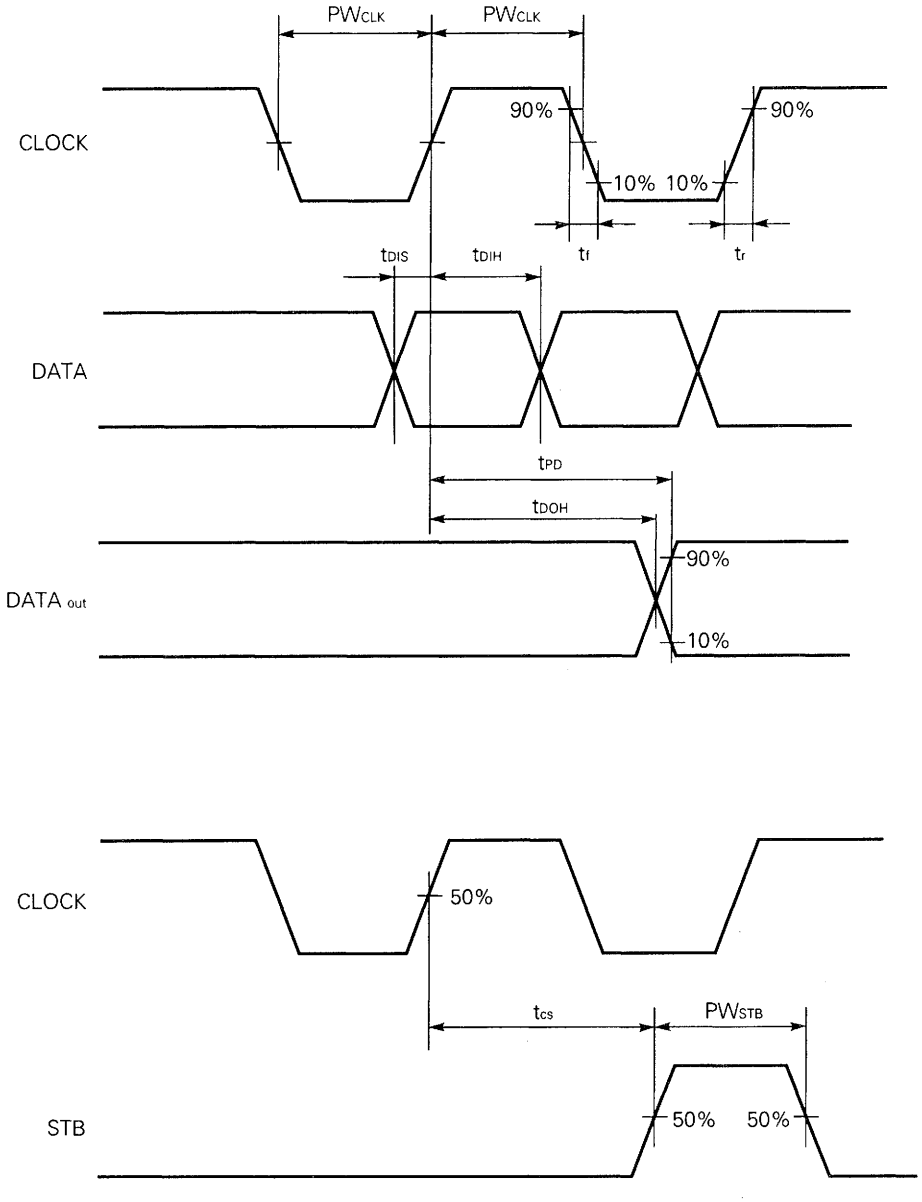
SWITCHING CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 5 V ± 10 %, V_{FIP} = 15 V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Clock Frequency	f_{CLK}			1.0	MHz	
Data out delay time	t_{PD}			500	ns	for CLOCK ↑
Data out hold time	t_{DOH}	200			ns	

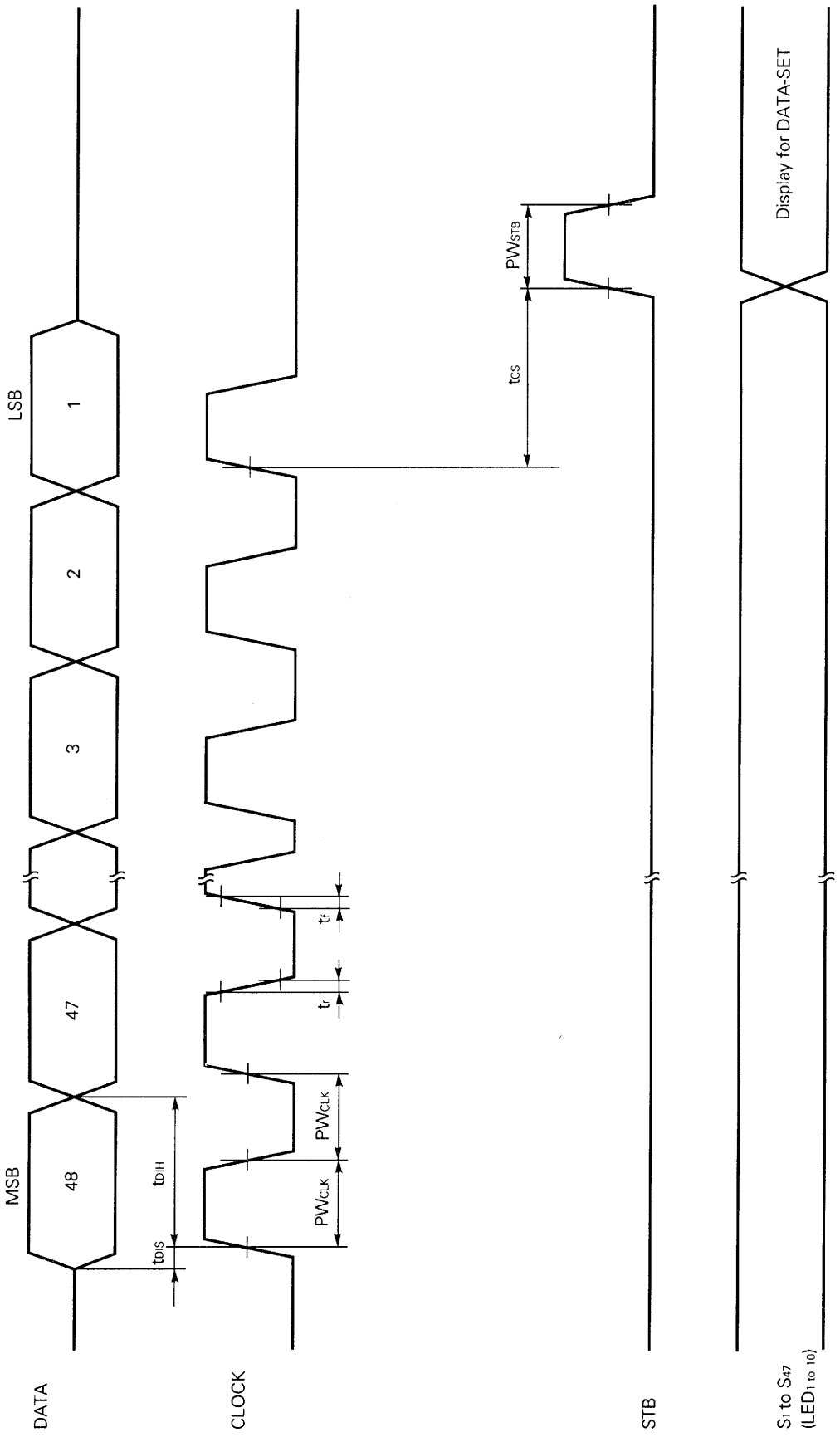
SWITCHING CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 5 V ± 10 %, V_{FIP} = 15 V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Clock Rising Time	t_r			1.0	μs	
Clock Falling Time	t_r			1.0	μs	
Clock Pulse Width	PW_{CLK}	400			ns	
Strobe Pulse Width	PW_{STB}	400			ns	
Data Set-up Time	t_{DIS}	200			ns	for CLOCK ↑
Data Hold Time	t_{DIH}	100			ns	for CLOCK ↑
Clock Set-up Time	t_{CS}	500			ns	for STB ↑

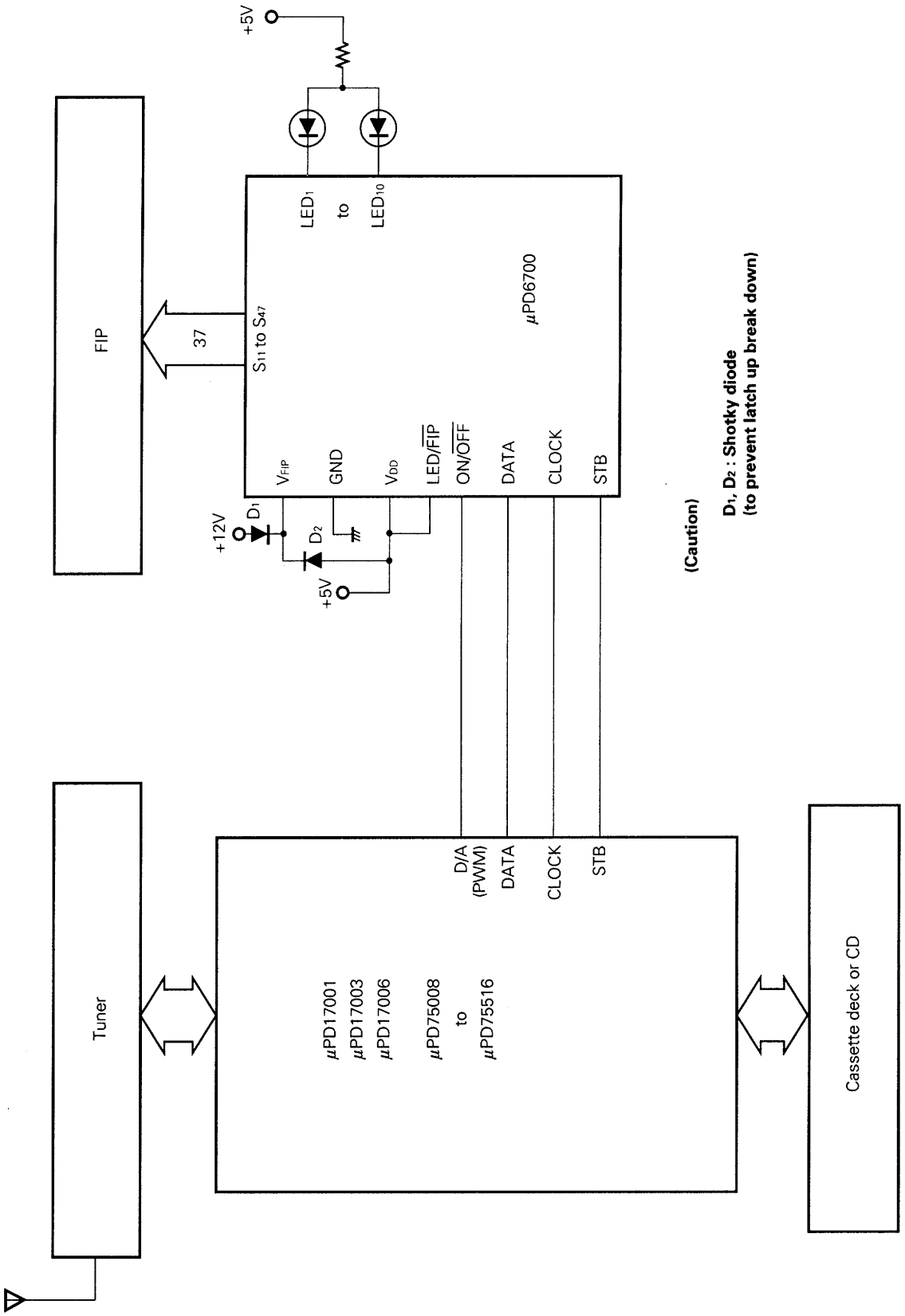
SWITCHING TIMING



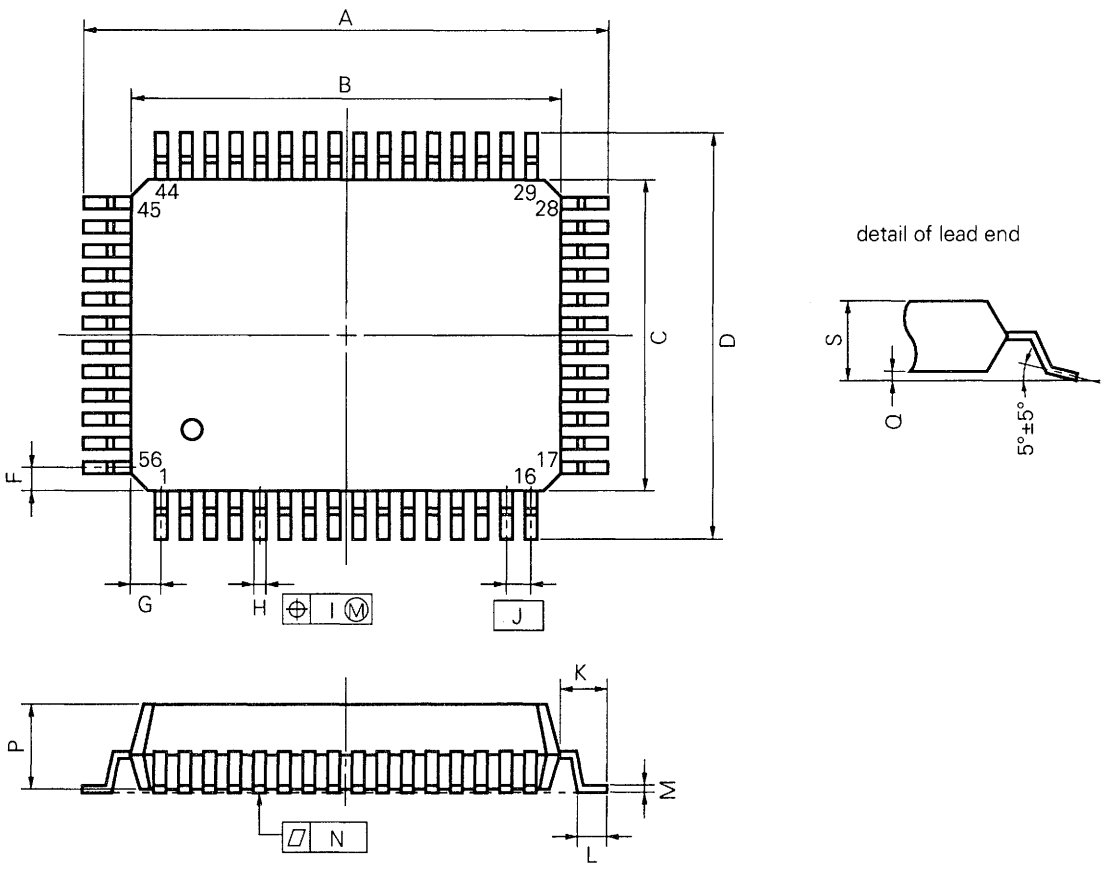
TIMING CHART



APPLICATION CIRCUIT (AUTOMOTIVE AUDIO BLOCK DIAGRAM)



56 PIN PLASTIC QFP (10 × 14)



S56GH-80-3B7-1

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	10.0±0.2	$0.394^{+0.008}_{-0.009}$
D	13.2±0.4	0.520±0.016
F	0.6	0.024
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product. Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

TYPES OF SURFACE MOUNT DEVICE

For more details, refer to our document "Semiconductor Device Mounting Technology Manual" (IEI-1207).

μPD6700GH-3B7

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 230 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow process: 1, Exposure limit*: None	IR30-00-1
VPS	Peak package's surface temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 1, Exposure limit*: None	VP15-00-1
Partial heating method	Terminal temperature: 300 °C or below, Flow time: 10 seconds or below, Exposure limit*: None	

* Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Note Do not apply more than a single process at once, except for "Partial heating method".

Reference

「Quality Grades On NEC Semiconductor Devices」(IEI-1209)
「NEC Semiconductor Device Reliability/Quality Controls」(IEI-1206)