FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-22004-1E

ASSP Communication Control

IEEE 1394 Open HCI Controller

MB86613

■ DESCRIPTION

The MB86613 a high-performance, host-bus (PCI) and serial-bus (1394) controller chip for controlling transfer between the PCI and 1394 buses. This chip conforms to the PCI Standard Version 2.1 for PCI control, the IEEE 1394-1995 Standard for 1394 control, and the Open HCI Standard Version 1.0 for PCI-1394 control.

The MB86613 consists of the PCI/DMA, OHCI, and 1394 blocks. The PCI/DMA block provides PCI bus protocol control. The block has the slave function for responding register access from a bus master, the master function for issuing transfer requests from the MB86613 as the bus master, the power management function (compliant with PCI bus power management standard version 1.0), and the interfaces to BIOS ROM and PCI configuration ROM.

The OHCI block analyzes context programs pre-stored in host memory to store the packet to be sent out from host memory to the FIFO buffer or to store the received packet from the FIFO buffer to host memory.

The 1394 block incorporates the LINK layer module, PHYsical layer module, 1394 transceiver, comparator, and PLL, providing 1394 bus protocol control. The block converts the packet stored in the FIFO buffer to serial data and send it onto the 1394 bus or converts the packet received from the 1394 bus to parallel data and stores it in the FIFO buffer.

For packet transmission and reception, the chip supports a transfer rate of up to S400.

In addition, the cycle master function is provided for automatic management of isochronous cycles.

The chip reserves 6K bytes of FIFO memory. The on-chip dual port RAM contains 3K bytes for packet transmission and 3K bytes for packet reception.

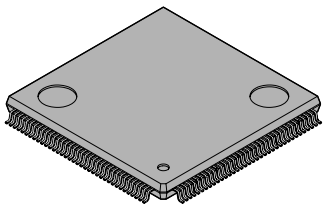
The MB86613 uses the 0.35 micron CMOS process technology, integrating the LINK and PHYsical layer modules on this single chip to reduce the packaging area and power consumption.

The chip has a dual-voltage system to support both 5 V (PCI/DMA) and 3.3 V (1394) power-supply voltages. Note that the PCI/DMA block can operate at 3.3 V.

The package is a plastic package of LQFP144 or FBGA176.

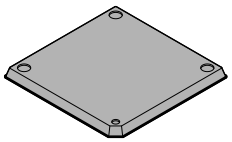
■ PACKAGES

144-pin plastic LQFP



(FPT-144P-M08)

176-pin plastic FBGA



(BGA-176P-M02)

■ FEATURES

1. 1394 serial bus controller Unit

- Compliant with IEEE 1394-1995 Standard
- PHYsical and LINK layer modules integrated on a single chip
- Three internal ports
- Transfer rates of S100, S200, and S400 supported
- On-chip PLL for generating 400-MHz (PHY) and 50-MHz (LINK) CLK signals
- Built-in cycle master function
- Bus management CSR (control and status register)
- Six-conductor cable supported
- Internal transceiver and comparator
- Internal comparator for cable power detection

2. Context program controller unit

- Compliant with Open HCI Standard (Draft 1.00)
- Thirteen context program controllers integrated:

Asynchronous Transmit DMA	…2ch	•Asynchronous response	…1ch
		•Asynchronous request	…1ch
Isochronous Transmit DMA	…4ch		
Receive DMA	…7ch	•Asynchronous response	…1ch
		•Asynchronous request	…1ch
		•Isochronous	…4ch
		•SelfID	…1ch

- Internal 6-KB FIFO buffers

Asynchronous Transmit FIFO	…1.5 Kbyte
isochronous Transmit FIFO	…1.5 Kbyte
Asynchronous/Isochronous Receive FIFO	…3.0 Kbyte

3. PCI bus controller unit

- Compliant with PCI Standard (Revision 2.2)
- On-chip 32-bit DMA controller
- Built-in power management function (Compliant with PCI bus power management standard version 1.0)
- Built-in alignment function
- Built-in byte swap function
- Operating frequency of up to 33 MHz
- Internal parallel ROM interface
- Internal serial ROM interface
- Internal universal (5/3.3 V shared) PCI buffer

4. Physical specifications

- Package: LQFP144 (FPT-144P-M08), FBGA176 (BGA-176P-M02)
- Power-supply voltage: Dual system for 5 V (± 5%) and 3.3 V (± 5%)

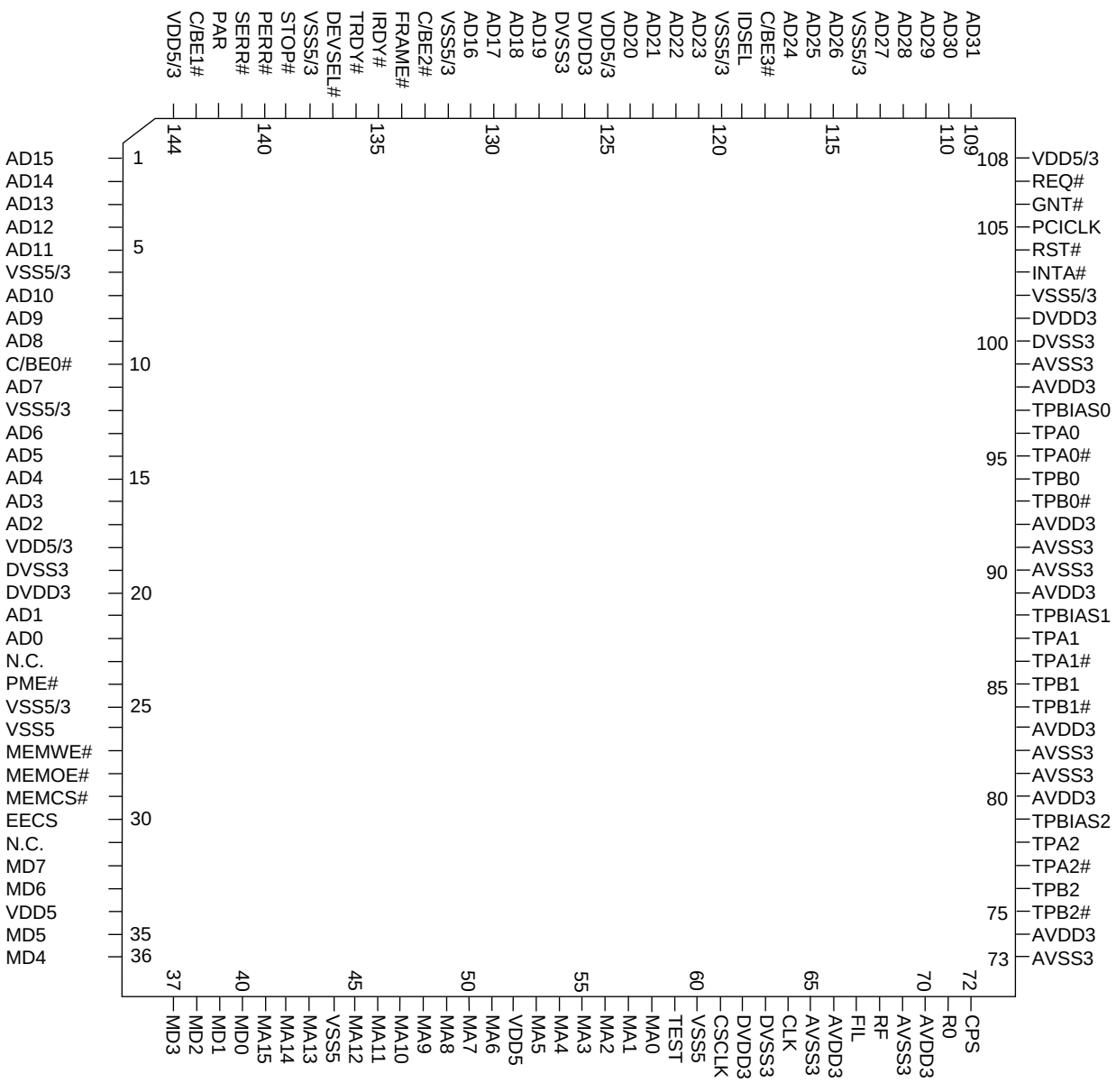
5. Reference standards

- IEEE Standard for a High Performance 1394-1995
- 1394 Open Host Controller Interface Specification (Release 1.00)
- PCI Specification (Revision 2.2)
- PCI Bus Power Management Interface Specification (Version 1.0)

■ PIN ASSIGNMENT

1. LQFP-144

(TOP VIEW)



(FPT-144P-M08)

2. FBGA-176

	N.C.	N.C.	AVSS3	AVSS3	CSCLK	MA1	MA5	MA8	VSS5	MA15	MD3	N.C.		P
N.C.	AVSS3	N.C.	AVDD3	AVDD3	DVDD3	MA0	VDD5	MA9	VSS3	MD0	N.C.	N.C.	N.C.	N
TPB2	TPB2#	N.C.	RO	FIL	DVSS3	TEST	MA6	MA10	MA13	MD2	N.C.	N.C.	N.C.	M
TPA2	TPA2#	N.C.	AVDD3	RF	CLK	MA2	MA7	MA11	MD1	N.C.	MD5	VDD5	MD6	L
AVSS3	AVDD3	TPBIAS2	N.C.	CPS	VSS5	MA3	MA4	MA14	MD4	MD7	N.C.	EECS	MEMCS#	K
TPB1	TPB1#	AVDD3	AVSS3	N.C.					PME#	MEMOE#	MEMWE#	VSS5	VSS5/3	J
TPBIAS1	TPA1	TPA1#	N.C.	AVDD3					DVSS3	DVDD3	N.C.	AD0	AD1	H
AVDD3	TPB0#	TPB0	AVSS3	AVSS3		(TOP VIEW)			VDD5/3	AD5	AD4	AD3	AD2	G
TPA0#	TPA0	TPBIAS0	AVDD3	N.C.					VSS5/3	C/BE0#	AD7	VSS5/3	AD6	F
AVSS3	DVSS3	DVDD3	VSS5/3	GNT#	VSS5/3	DVDD3	DVSS3	VSS5/3	VDD5/3	AD13	AD10	AD9	AD8	E
INTA#	RST#	PCICLK	N.C.	AD29	C/BE3#	AD22	AD19	TRDY#	PERR#	N.C.	AD14	AD12	AD11	D
REQ#	VDD5/3	N.C.	AD30	AD26	IDSEL	AD22	AD16	IRDY#	STOP#	C/BE1#	N.C.	N.C.	AD15	C
N.C.	N.C.	N.C.	AD28	AD25	VSS5/3	AD20	AD17	FRAME#	VSS5/3	PAR	N.C.	N.C.	N.C.	B
	N.C.	AD31	AD27	AD24	AD23	VDD5/3	AD18	C/BE2#	DEVSEL#	SERR#	N.C.	N.C.		A
14	13	12	11	10	9	8	7	6	5	4	3	2	1	

(BGA-176P-M02)

■ PIN LIST

1. LQFP-144

Pin No.	I/O	Pin name	Supply Voltage (V)	Pin No.	I/O	Pin name	Supply Voltage (V)
1	I/O	AD15	5/3.3	36	I/O	MD4	5
2	I/O	AD14	5/3.3	37	I/O	MD3	5
3	I/O	AD13	5/3.3	38	I/O	MD2	5
4	I/O	AD12	5/3.3	39	I/O	MD1	5
5	I/O	AD11	5/3.3	40	I/O	MD0	5
6	—	VSS5/3	—	41	O	MA15	5
7	I/O	AD10	5/3.3	42	O	MA14	5
8	I/O	AD9	5/3.3	43	O	MA13	5
9	I/O	AD8	5/3.3	44	—	VSS5	—
10	I/O	C/BE0#	5/3.3	45	O	MA12	5
11	I/O	AD7	5/3.3	46	O	MA11	5
12	—	VSS5/3	—	47	O	MA10	5
13	I/O	AD6	5/3.3	48	O	MA9	5
14	I/O	AD5	5/3.3	49	O	MA8	5
15	I/O	AD4	5/3.3	50	O	MA7	5
16	I/O	AD3	5/3.3	51	O	MA6	5
17	I/O	AD2	5/3.3	52	—	VDD5	—
18	—	VDD5/3	—	53	O	MA5	5
19	—	DVSS3	—	54	O	MA4	5
20	—	DVDD3	—	55	O	MA3	5
21	I/O	AD1	5/3.3	56	O	MA2	5
22	I/O	AD0	5/3.3	57	O	MA1	5
23	—	N.C	—	58	O	MA0	5
24	O	PME#	5/3.3	59	I	TEST	5
25	—	VSS5/3	—	60	—	VSS5	—
26	—	VSS5	—	61	I	CSCLK	5/3.3
27	O	MEMWE#	5	62	—	DVDD3	—
28	O	MEMOE#	5	63	—	DVSS3	—
29	O	MEMCS#	5	64	I	CLK	5/3.3
30	O	EECS	5	65	—	AVSS3	—
31	—	N.C	—	66	—	AVDD3	—
32	I/O	MD7	5	67	I	FIL	3.3
33	I/O	MD6	5	68	O	RF	3.3
34	—	VDD5	—	69	—	AVSS3	—
35	I/O	MD5	5	70	—	AVDD3	—

(Continued)

(Continued)

Pin No.	I/O	Pin name	Supply Voltage (V)	Pin No.	I/O	Pin name	Supply Voltage (V)
71	O	R0	3.3	108	—	VDD5/3	—
72	I	CPS	3.3	109	I/O	AD31	5/3.3
73	—	AVSS3	—	110	I/O	AD30	5/3.3
74	—	AVDD3	—	111	I/O	AD29	5/3.3
75	I/O	TPB2#	3.3	112	I/O	AD28	5/3.3
76	I/O	TPB2	3.3	113	I/O	AD27	5/3.3
77	I/O	TPA2#	3.3	114	—	VSS5/3	—
78	I/O	TPA2	3.3	115	I/O	AD26	5/3.3
79	O	TPBIAS2	3.3	116	I/O	AD25	5/3.3
80	—	AVDD3	—	117	I/O	AD24	5/3.3
81	—	AVSS3	—	118	I/O	C/BE3#	5/3.3
82	—	AVSS3	—	119	I	IDSEL	5/3.3
83	—	AVDD3	—	120	—	VSS5/3	—
84	I/O	TPB1#	3.3	121	I/O	AD23	5/3.3
85	I/O	TPB1	3.3	122	I/O	AD22	5/3.3
86	I/O	TPA1#	3.3	123	I/O	AD21	5/3.3
87	I/O	TPA1	3.3	124	I/O	AD20	5/3.3
88	O	TPBIAS1	3.3	125	—	VDD5/3	—
89	—	AVDD3	—	126	—	DVDD3	—
90	—	AVSS3	—	127	—	DVSS3	—
91	—	AVSS3	—	128	I/O	AD19	5/3.3
92	—	AVDD3	—	129	I/O	AD18	5/3.3
93	I/O	TPB0#	3.3	130	I/O	AD17	5/3.3
94	I/O	TPB0	3.3	131	I/O	AD16	5/3.3
95	I/O	TPA0#	3.3	132	—	VSS5/3	—
96	I/O	TPA0	3.3	133	I/O	C/BE2#	5/3.3
97	O	TPBIAS0	3.3	134	I/O	FRAME#	5/3.3
98	—	AVDD3	—	135	I/O	IRDY#	5/3.3
99	—	AVSS3	—	136	I/O	TRDY#	5/3.3
100	—	DVSS3	—	137	I/O	DEVSEL#	5/3.3
101	—	DVDD3	—	138	—	VSS5/3	—
102	—	VSS5/3	—	139	I/O	STOP#	5/3.3
103	OD	INTA#	5/3.3	140	I/O	PERR#	5/3.3
104	I	RST#	5/3.3	141	OD	SERR#	5/3.3
105	I	PCICLK	5/3.3	142	I/O	PAR	5/3.3
106	I	GNT#	5/3.3	143	I/O	C/BE1#	5/3.3
107	O	REQ#	5/3.3	144	—	VDD5/3	—

2. FBGA-176

Ball No.	I/O	Pin name	Supply Voltage (V)	Ball No.	I/O	Pin name	Supply Voltage (V)
B1	—	N.C.	—	K4	I/O	MD7	5
B2	—	N.C.	—	L1	I/O	MD6	5
D4	—	N.C.	—	L2	—	VDD5	—
C2	—	N.C.	—	L3	I/O	MD5	5
C1	I/O	AD15	5/3.3	K5	I/O	MD4	5
D3	I/O	AD14	5/3.3	M1	—	N.C.	—
E4	I/O	AD13	5/3.3	M2	—	N.C.	—
D2	I/O	AD12	5/3.3	M3	—	N.C.	—
D1	I/O	AD11	5/3.3	N1	—	N.C.	—
F5	—	VSS5/3	—	P2	—	N.C.	—
E3	I/O	AD10	5/3.3	N2	—	N.C.	—
E2	I/O	AD9	5/3.3	L4	—	N.C.	—
E1	I/O	AD8	5/3.3	N3	—	N.C.	—
F4	I/O	C/BE0#	5/3.3	P3	I/O	MD3	5
F3	I/O	AD7	5/3.3	M4	I/O	MD2	5
F2	—	VSS5/3	—	L5	I/O	MD1	5
F1	I/O	AD6	5/3.3	N4	I/O	MD0	5
G4	I/O	AD5	5/3.3	P4	O	MA15	5
G3	I/O	AD4	5/3.3	K6	O	MA14	5
G2	I/O	AD3	5/3.3	M5	O	MA13	5
G1	I/O	AD2	5/3.3	N5	—	VSS5	—
G5	—	VDD5/3	—	P5	O	MA12	5
H5	—	DVSS3	—	L6	O	MA11	5
H4	—	DVDD3	—	M6	O	MA10	5
H1	I/O	AD1	5/3.3	N6	O	MA9	5
H2	I/O	AD0	5/3.3	P6	O	MA8	5
H3	—	N.C	—	L7	O	MA7	5
J5	OD	PME#	5/3.3	M7	O	MA6	5
J1	—	VSS5/3	—	N7	—	VDD5	—
J2	—	VSS5	—	P7	O	MA5	5
J3	O	MEMWE#	5	K7	O	MA4	5
J4	O	MEMOE#	5	K8	O	MA3	5
K1	O	MEMCS#	5	L8	O	MA2	5
K2	O	EECS	5	P8	O	MA1	5
K3	—	N.C.	—	N8	O	MA0	5

(Continued)

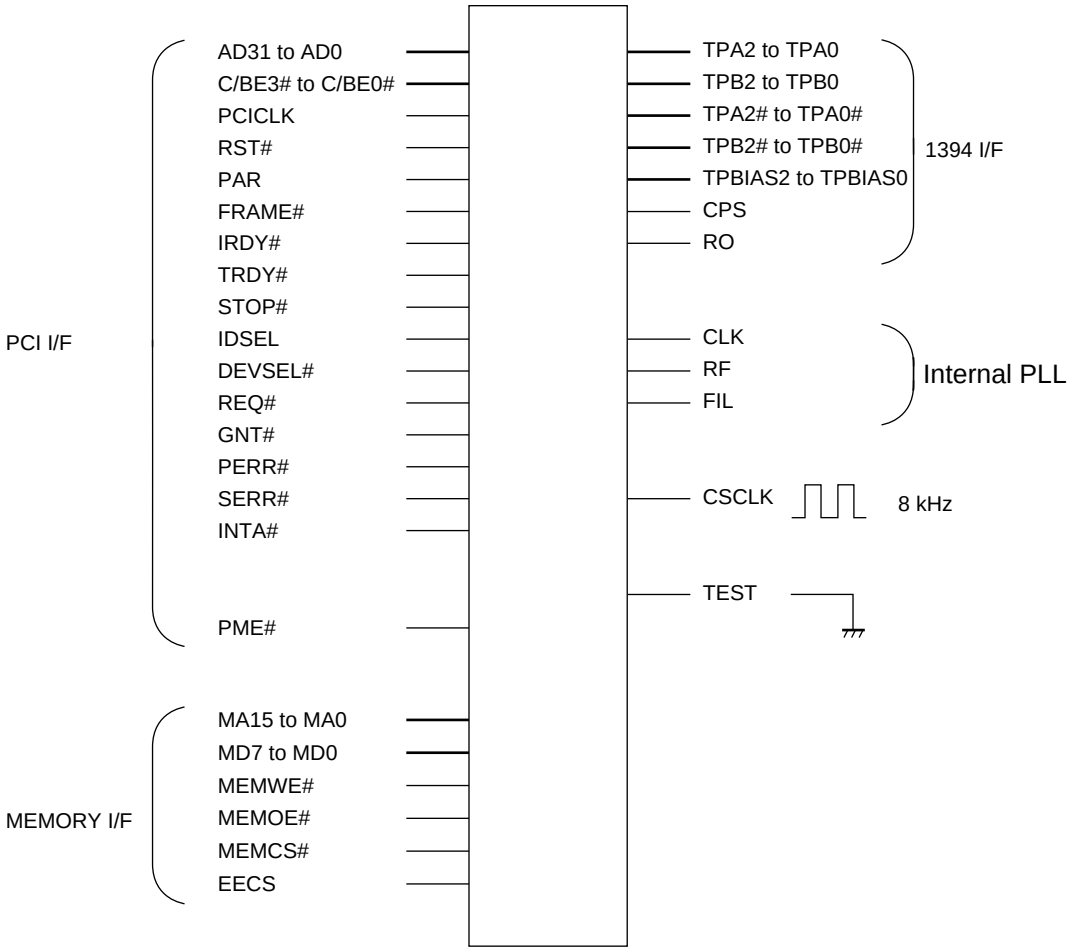
Ball No.	I/O	Pin name	Supply Voltage (V)	Ball No.	I/O	Pin name	Supply Voltage (V)
M8	I	TEST	5	H11	—	N.C.	—
K9	—	VSS5	—	H12	I/O	TPA#1	3.3
P9	I	CSCLK	5/3.3	H13	I/O	TPA1	3.3
N9	—	DVDD3	—	H14	O	TPBIAS1	3.3
M9	—	DVSS3	—	H10	—	AVDD3	—
L9	I	CLK	5/3.3	G10	—	AVSS3	—
P10	—	AVSS3	—	G11	—	AVSS3	—
N10	—	AVDD3	—	G14	—	AVDD3	—
M10	I	FIL	3.3	G13	I/O	TPB0#	3.3
L10	O	RF	3.3	G12	I/O	TPB0	3.3
P11	—	AVSS3	—	F10	—	N.C.	—
N11	—	AVDD3	—	F14	I/O	TPA0#	3.3
M11	O	R0	3.3	F13	I/O	TPA0	3.3
K10	I	CPS	3.3	F12	O	TPBIAS0	3.3
P12	—	N.C.	—	F11	—	AVDD3	—
N12	—	N.C.	—	E14	—	AVSS3	—
M12	—	N.C.	—	E13	—	DVSS3	—
P13	—	N.C.	—	E12	—	DVDD3	—
N14	—	N.C.	—	E11	—	VSS5/3	—
N13	—	AVSS3	—	D14	OD	INTA#	5/3.3
L11	—	AVDD3	—	D13	I	RST#	5/3.3
M13	I/O	TPB2#	3.3	D12	I	PCICLK	5/3.3
M14	I/O	TPB2	3.3	E10	I	GNT#	5/3.3
L12	—	N.C.	—	C14	O	REQ#	5/3.3
K11	—	N.C.	—	C13	—	VDD5/3	—
L13	I/O	TPA2#	3.3	C12	—	N.C.	—
L14	I/O	TPA2	3.3	B14	—	N.C.	—
J10	—	N.C.	—	A13	—	N.C.	—
K12	O	TPBIAS2	3.3	B13	—	N.C.	—
K13	—	AVDD3	—	D11	—	N.C.	—
K14	—	AVSS3	—	B12	—	N.C.	—
J11	—	AVSS3	—	A12	I/O	AD31	5/3.3
J12	—	AVDD3	—	C11	I/O	AD30	5/3.3
J13	I/O	TPB1#	3.3	D10	I/O	AD29	5/3.3
J14	I/O	TPB1	3.3	B11	I/O	AD28	5/3.3

(Continued)

(Continued)

Ball No.	I/O	Pin name	Supply Voltage (V)	Ball No.	I/O	Pin name	Supply Voltage (V)
A11	I/O	AD27	5/3.3	C7	I/O	AD16	5/3.3
E9	—	VSS5/3	—	E6	—	VSS5/3	—
C10	I/O	AD26	5/3.3	A6	I/O	C/BE2#	5/3.3
B10	I/O	AD25	5/3.3	B6	I/O	FRAME#	5/3.3
A10	I/O	AD24	5/3.3	C6	I/O	IRDY#	5/3.3
D9	I/O	C/BE3#	5/3.3	D6	I/O	TRDY#	5/3.3
C9	I	IDSEL	5/3.3	A5	I/O	DEVSEL#	5/3.3
B9	—	VSS5/3	—	B5	—	VSS5/3	—
A9	I/O	AD23	5/3.3	C5	I/O	STOP#	5/3.3
D8	I/O	AD22	5/3.3	D5	I/O	PERR#	5/3.3
C8	I/O	AD21	5/3.3	A4	OD	SERR#	5/3.3
B8	I/O	AD20	5/3.3	B4	I/O	PAR	5/3.3
A8	—	VDD5/3	—	C4	I/O	C/BE1#	5/3.3
E8	—	DVDD3	—	E5	—	VDD5/3	—
E7	—	DVSS3	—	A3	—	N.C.	—
D7	I/O	AD19	5/3.3	B3	—	N.C.	—
A7	I/O	AD18	5/3.3	C3	—	N.C.	—
B7	I/O	AD17	5/3.3	A2	—	N.C.	—

■ PIN DESCRIPTION



Output pins of MB86613

1. PCI Interface Pin Description

Pin name	I/O	Function
AD31 to AD0	I/O	32-bit data/address multiplexed signal
C/BE3# to C/BE0#	I/O	Bus-command and byte-enable multiplexed signal
PCICLK	I	PCI bus clock input pin (Up to 33 MHz)
RST#	I	System reset input pin
PAR	I/O	Even parity bit for AD31:0 and C/BE3:0. Enabled one PCI clock signal after address phase.
FRAME#	I/O	Signal indicating that the bus is being driven by the master.
IRDY#	I/O	Master data ready signal
TRDY#	I/O	Target data ready signal
STOP#	I/O	Target-to-master data transfer stop request signal
IDSEL	I	Chip select signal for accessing the configuration register
DEVSEL#	I/O	During target operation: Output signal indicating that the this device has been selected. During master operation: Input signal indicating that the device connected to the PCI bus has been selected.
REQ#	O	Output signal requesting the bus arbiter for using the PCI bus
GNT#	I	Input signal for bus arbiter's response to REQ#
PERR#	I/O	Data parity error I/O signal
SERR#	OD	Address parity error I/O signal
INTA#	OD	Interrupt output signal
PME#	OD	Power supply request signal in power save mode

2. Memory Interface Pin Description

Pin name	I/O	Function
MA15 to MA0	O	Externally-connected EPROM (BIOS ROM) address signal
MD7 to MD0	I/O	Externally-connected EPROM (BIOS ROM) data signal
MEMWE#	O	Connect this pin to the WE pin on the externally-connected EPROM (BIOS ROM)
MEMOE#	O	Connect this pin to the OE pin on the externally-connected EPROM (BIOS ROM)
MEMCS#	O	Connect this pin to the CS pin on the externally-connected EPROM (BIOS ROM)
EECS	O	Connect this pin to the CS pin on the externally-connected EEPROM (PCI configuration ROM)

3. 1394 Interface Pin Description

Pin name	I/O	Function
TPA2 to TPA0	I/O	Differential I/O positive terminal of 1394 bus port A
TPB2 to TPB0	I/O	Differential I/O positive terminal of 1394 bus port B
TPA2# to TPA0#	I/O	Differential I/O negative terminal of 1394 bus port A
TPB2# to TPB0#	I/O	Differential I/O negative terminal of 1394 bus port B
TPBIAS2 to TPBIAS0	O	1394 bus bias voltage supply pin. For connecting a terminal resistor to TPBIAS and TPA/B, see “ ■COMPONENT CONNECTION DIAGRAM 1. 1394 Ports”.
CPS	I	Cable power input pin
RO	O	Connect a 5.1 kΩ resistor between the RO and GND pins. For details, see “ ■COMPONENT CONNECTION DIAGRAM 1. 1394 Ports”.

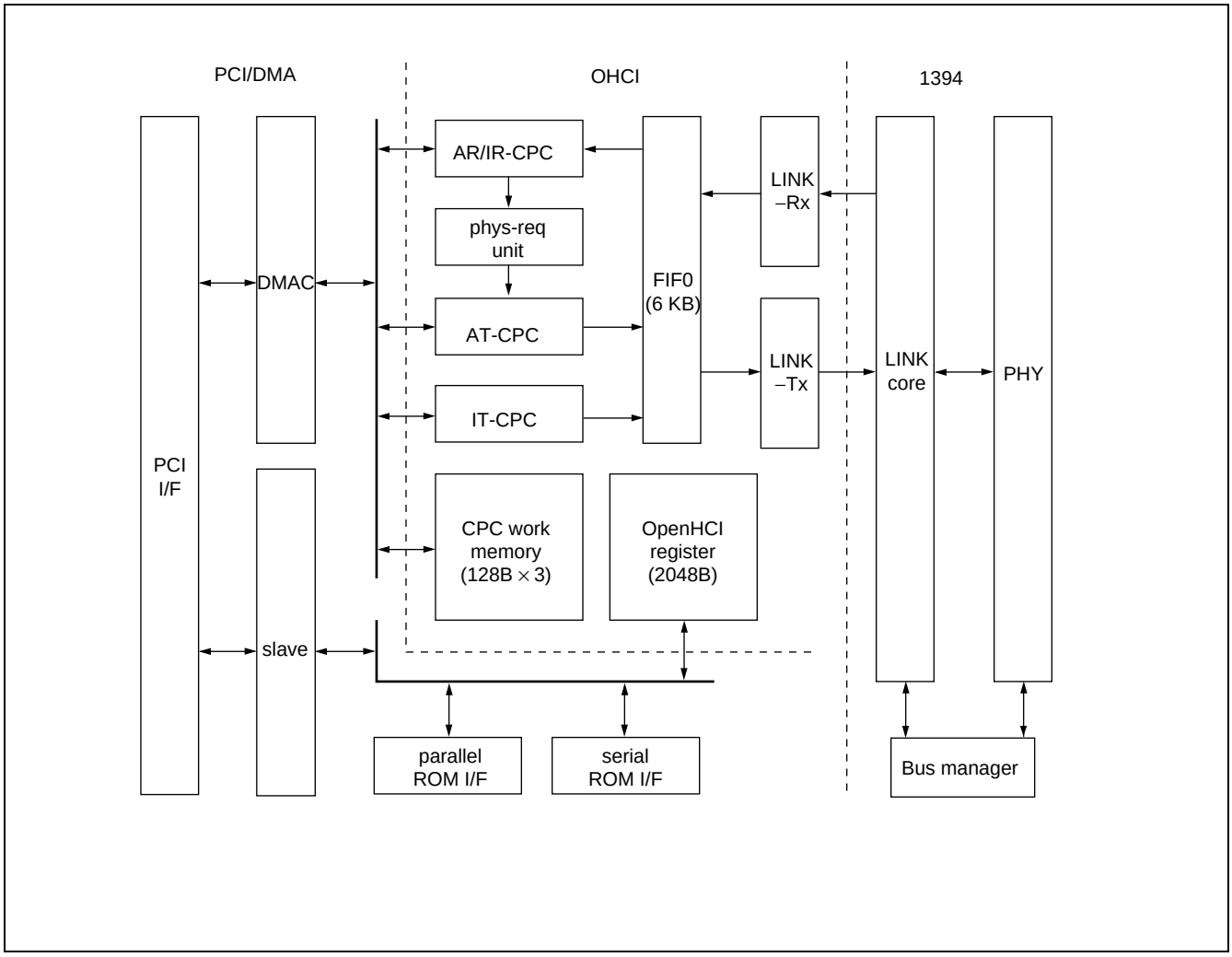
4. Internal PLL Pin Description

Pin name	I/O	Function
CLK	I	Internal PLL clock input pin. Input a 24.576 MHz clock signal.
RF	O	Connect a 5.6 kΩ resistor between the RO and GND pins. For details, see “ ■COMPONENT CONNECTION DIAGRAM 2. Filter Circuit”.
FIL	O	Filter circuit connection pin. For connecting the filter circuit, see “ ■COMPONENT CONNECTION DIAGRAM 2. Filter Circuit”.

5. Miscellaneous Pin Description

Pin name	I/O	Function
CSCLK	I	This pin inputs the trigger signal for sending a cycle start packet during cycle master operation. Input an 8 kHz (125 μs) clock signal. If the CLK pin is not used (with no Link Control. cycle Source bit set), however, connect this pin to GND.
TEST	I	This pin in used for test mode. During normal operation, leave this pin connected to GND.
N.C.	—	Leave this pin unconnected.

■ BLOCK DIAGRAM



■ BLOCK DESCRIPTION

• Parallel ROM I/F

This block is the parallel port ROM interface to which EPROM (BIOS ROM) with a data width of 8 bits and that EEPROM (PCI configuration ROM) are connected which contains PCI subsystem ID and subsystem vendor ID information. For details, see " ■COMPONENT CONNECTION DIAGRAM 3. Memory Interface"

• CPC (context program controller)

This block analyzes context programs stored in host memory to store the packet to be sent out from host memory to the FIFO buffer or to store the received packet from the FIFO buffer to host memory (AR-CPC, IR-CPC). Upon reception of a physical request packet, this block analyzes the packet automatically for servicing the request (phys-req unit).

• CPC work memory

This block is work memory which stores context programs prepared in host memory or packet header information upon reception of a physical request packet.

• OHCI register

This block holds 2048 bytes of registers defined in the Open HCI Standard.

• FIFO

This block is a 6-KB FIFO buffer. This FIFO consists of a transmit-packet storage area (AT-FIFO and IT-FIFO) and a receive-packet storage area (AR-FIFO and IR-FIFO), each of which is freely addressable.

• LINK-Rx

This block stores the LINK-received, 1394-formatted packet in the FIFO buffer, with trailer data defined in the Open HCI Standard added.

• LINK-Tx

This block converts the packet stored in the FIFO buffer into the 1394 format and sends it to the LINK.

• PCI I/F

This block provides PCI bus protocol control.

• PCI-DMAC

This block issues a transfer request with the MB86613 serving as the bus master.

• PCI-slave

This block responds to the register access from the bus master.

• LINK core

This block generates data CRC and header CRC, transmits the selfID packet, and controls packet transmission and reception.

• PHY

This block provides 1394 bus protocol control.

• Bus manager

This block manages the cycle timer, generates a variety of interrupts, and holds the bus management CSR.

■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating		Unit
			Min.	Max.	
Power supply voltage*1	at 5 V*2	V_{DD}	V_{SS} – 0.5	6.0	V
	at 3 V*3		V_{SS} – 0.5	4.0	
Input current*1		V_I	V_{SS} – 0.5	V_{DD} + 0.5	V
Output current*1		V_O	V_{SS} – 0.5	V_{DD} + 0.5	V
Storage temperature		T_{ST}	–55	+125	°C
Operating junction temperature		T_{OP}	–40	+125	°C

*1 : The voltages are bassed on V_{SS} = 0 V.

*2 : The 5 V power supply is the voltage applied at the VDD5/3 and VDD5 power supply pins.

*3 : The 3 V power supply is the voltage applied at the DVDD3 and AVDD3 power supply pins.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Value		Unit
			Min.	Max.	
Power supply voltage*1	at 5 V*2	V_{DD5}	4.75	5.25	V
	at 3 V*3	V_{DD3}	3.0	3.6	
Differential input voltage	TPA/B arbitration	V_{ID}	168	265	mV p-p diff
	TPA/B S100*4		142	260	
	TPA/B S200*4		132	260	
	TPA/B S400*4		118	260	
TPBias input voltage	TPA/B S100*4	V_{CM}	1.165	2.515*5	V
	TPA/B S200*4		0.935	2.515*5	
	TPA/B S400*4		0.523	2.515*5	
Receiving input jitter	TPA/B S100*4	—	—	±1.08	ns
	TPA/B S200*4		—	±0.5	
	TPA/B S400*4		—	±0.315	
Receiving input skew*6	TPA/B S100*4	—	—	±0.8	ns
	TPA/B S200*4		—	±0.55	
	TPA/B S400*4		—	±0.5	
Output current	TPBIAS pin	I_O	−2	+2	mA
	MD pin		−4	+4	
Operating ambient temperature		Ta	0	70	°C

*1 : Voltage values are based on Vss =0V.

*2 : The 5 V power supply is the voltage applied at the VDD5/3 and VDD5 power supply pins.

*3 : The 3 V power supply is the voltage applied at the DVDD3 and AVDD3 power supply pins.

*4 : During speed signaling

*5 : With cable power feed, the value is 2.015 (V).

*6 : Skew between TPA pin and TPB pin.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(V_{DD} = 4.75 to 5.25 V (for 5 V) , V_{DD} = 3.0 to 3.6 V (for 3 V) , V_{SS} = 0 V, Ta = 0 to + 70 °C)

Parameter		Symbol	Value		Unit
			Min.	Max.	
Power supply voltage	at 5 V*1	I_{DD}	—	50	mA
	at 3 V*2		—	200 (10) *3	

*1 : The 5 V power supply is the voltage applied at the VDD5/3 and VDD5 power supply pins.

*2 : The 3 V power supply is the voltage applied at the DVDD3 and AVDD3 power supply pins.

*3 : Supply current in sleep mode.

(1) PCI Interface

(V_{DD} = 3.0 to 3.6 V, Ta = 0 to + 70 °C)

Parameter	Symbol	Condition	Value		Unit
			Min.	Max.	
“H” level input voltage	V_{IH}	—	$V_{DD3} \times 0.5$	$V_{DD3} + 0.5$	V
“L” level input voltage	V_{IL}	—	$V_{SS} - 0.5$	$V_{DD3} \times 0.3$	V
“H” level output voltage	V_{OH}	I_{OH} = –0.5 (mA)	$V_{DD3} \times 0.9$	—	V
“L” level output voltage	V_{OL}	I_{OL} = 1.5 (mA)	—	$V_{DD3} \times 0.1$	V
Input leak current	I_{IL}	$0 < V_{IN} < V_{DD3}$	—	±10	µA
Input pin capacitance	C_{IN}	—	—	10	pF
Clock pin capacitance	C_{CLK}	—	5	12	pF

(2) PCI Interface

(V_{DD} = 4.75 to 5.25 V, T_a = 0 to + 70 °C)

Parameter	Symbol	Condition	Value		Unit
			Min.	Max.	
“H” level input voltage	V_{IH}	—	2.0	$V_{DD5} + 0.5$	V
“L” level input voltage	V_{IL}	—	$V_{SS} - 0.5$	0.8	V
“H” level output voltage	V_{OH}	I_{OH} = –2.0 (mA)	2.4	—	V
“L” level output voltage	V_{OL}	I_{OL} = 3.0 (mA)	—	0.55	V
Input leak current	I_{IH}	V_{IN} = 2.7 (V)	—	±10	µA
	I_{IL}	V_{IN} = 0.5 (V)	—	±10	µA
Input pin capacitance	C_{IN}	—	—	10	pF
Clock pin capacitance	C_{CLK}	—	5	12	pF

(3) Memory Interface

Parameter	Symbol	Condition	Value		Unit
			Min.	Max.	
"H" level input voltage	V_{IH}	—	2.0	$V_{DD5} + 0.5$	V
"L" level input voltage	V_{IL}	—	$V_{SS} - 0.5$	0.8	V
"H" level output voltage	V_{OH}	$I_{OH} = -4.0$ (mA)	2.4	—	V
"L" level output voltage	V_{OL}	$I_{OL} = 4.0$ (mA)	—	0.4	V
Input leak current*1	I_{IH}	$V_{IN} = 2.7$ (V)	—	±10	µA
	I_{IL}	$V_{IN} = 0.5$ (V)	—	±10	µA
Input pull-up/pull-down resistance*2	R_P	$V_{IH} = V_{DD5}$	25	100	kΩ

*1 : For input at 3-state pin.

*2 : Typical resistance value 50 kΩ.

(4) CLK, CSCLK Pins

Parameter	Symbol	Condition	Value		Unit
			Min.	Max.	
"H" level input voltage	V_{IH}	—	$V_{DD3} \times 0.7$	$V_{DD3} + 0.3$	V
"L" level input voltage	V_{IL}	—	V_{SS}	$V_{DD3} \times 0.2$	V
Input leak current*	I_{IL}	$0 < V_{IN} < V_{DD3}$	–5	+5	µA
Input pull-up/pull-down resistance	R_P	$V_{IH} = V_{DD3}$	25	200	kΩ
Clock pin capacitance	C_{CLK}	—	TBD	TBD	pF

* : For input at 3-state pin.

(5) 1394 Interface

Parameter	Symbol	Condition	Value		Unit
			Min.	Max.	
Differential output voltage	V_{OD}	56 Ω terminal	172	265	mV
Common phase current	I_{CM}	Transceiver OFF	–0.81	0.44	mA
Off state voltage	V_{OFF}	Transceiver OFF	—	20	mV
Speed-signal drive current	—	S100	–0.81	0.44	mA
		S200	–2.53	–4.84	mA
		S400	–8.10	–12.40	mA
TPBIAS output voltage*1	V_O	—	1.665	2.015	V
DS comparator offset voltage*2	V_{IT}	—	–30	30	mV
Arbitration comparator offset voltage*2	V_{ITH}	—	89	168	mV
	V_{ITL}	—	–168	–89	mV
Speed-signal comparator offset voltage*3	V_{IT}	S200	120	180	mV
		S400	290	380	mV
Port status comparator offset voltage*4	V_{IT}	—	0.6	1.0	V
Schmitt trigger receiver threshold voltage for detection connection	V_{IT+}*6	—	1.95	2.40	V
	V_{IT-}*6	—	1.00	1.45	V
Comparator offset voltage for detecting cable power supply	V_{IT}	—	1.125 (7.5) *5	1.275 (8.5) *5	V
CPS pin input voltage	V_{CPS}	—	V_{SS}	V_{DD5}	V
Common input current	I_{IC}	—	–20	20	µA

*1 : When the TPBIAS supply is Off, the maximum value with cable connected is 0.4 V, and when the cable is not connected the maximum output voltage is V_{DD}.

* 2 : Electrical potential created between TPA and TPB pins.

*3 : Electrical potential created between TPBIAS and TPA/B pins

*4 : At a point midway between the TPB/TPB# pins.

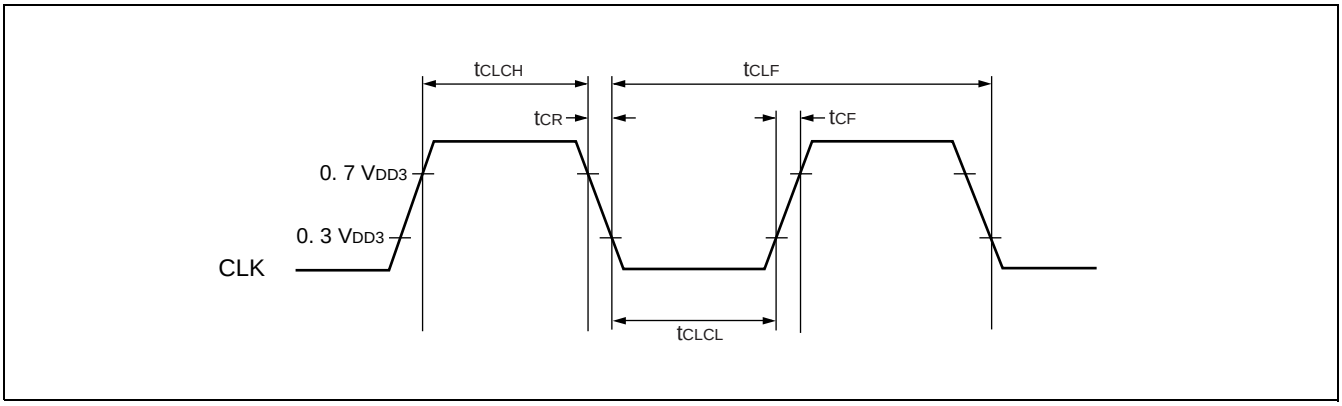
*5 : Cable supply voltage (VP) : voltage before division by 510 kΩ to 91 kΩ resistance

*6 : VIT+ is the voltage before cable disconnection is detected. VIT- is the voltage after cable connection is detected.

2. AC Characteristics

(1) CLK

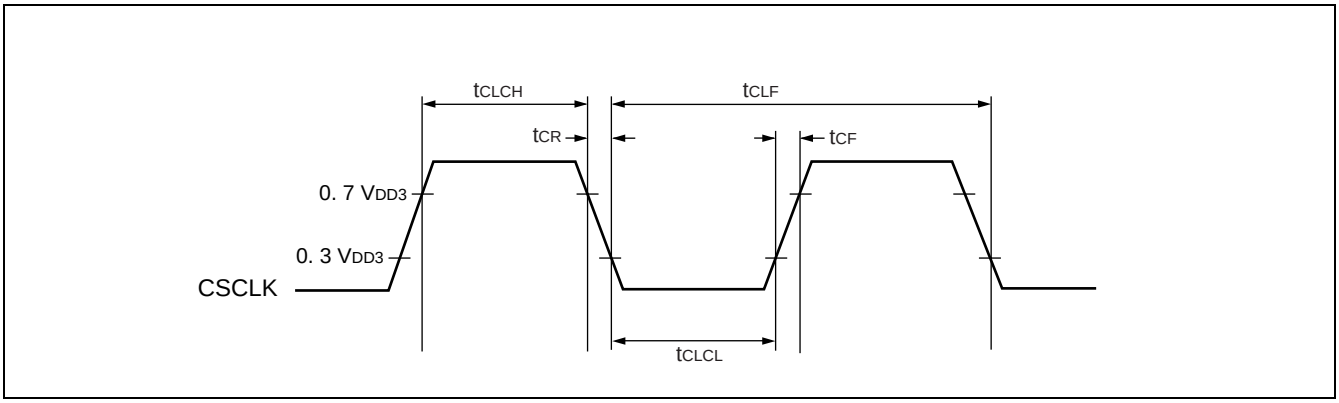
Parameter	Symbol	Condition	Value		Unit
			Min.	Max.	
Clock frequency	f_C	—	24.576		MHz
Clock cycle time	t_{CLF}	—	1 / f_C		µs
Clock pulse width	t_{CLCH}, t_{CLCL}	—	10	—	ns
Clock rise/fall time	t_{CR}, t_{CF}	—	—	5	ns



Note : The CLK pin is the pin used for input of the reference clock signal for the built-in PLL circuit.

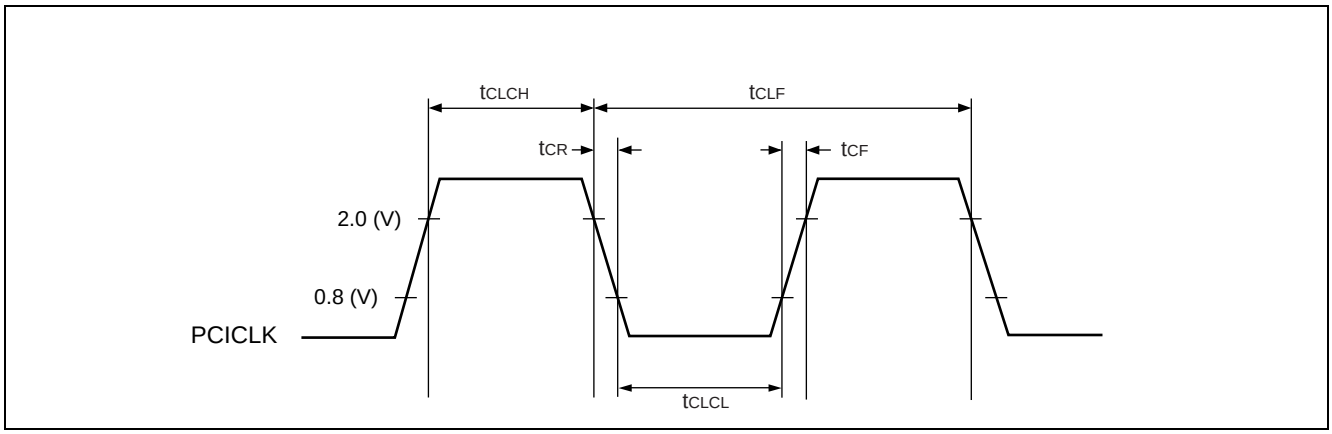
(2) CSCLK

Parameter	Symbol	Condition	Value		Unit
			Min.	Max.	
Clock frequency	f_C	—	8		kHz
Clock cycle time	t_{CLF}	—	1 / f_C		ms
Clock pulse width	t_{CLCH}, t_{CLCL}	—	50	—	µs
Clock rise/fall time	t_{CR}, t_{CF}	—	—	5	ns



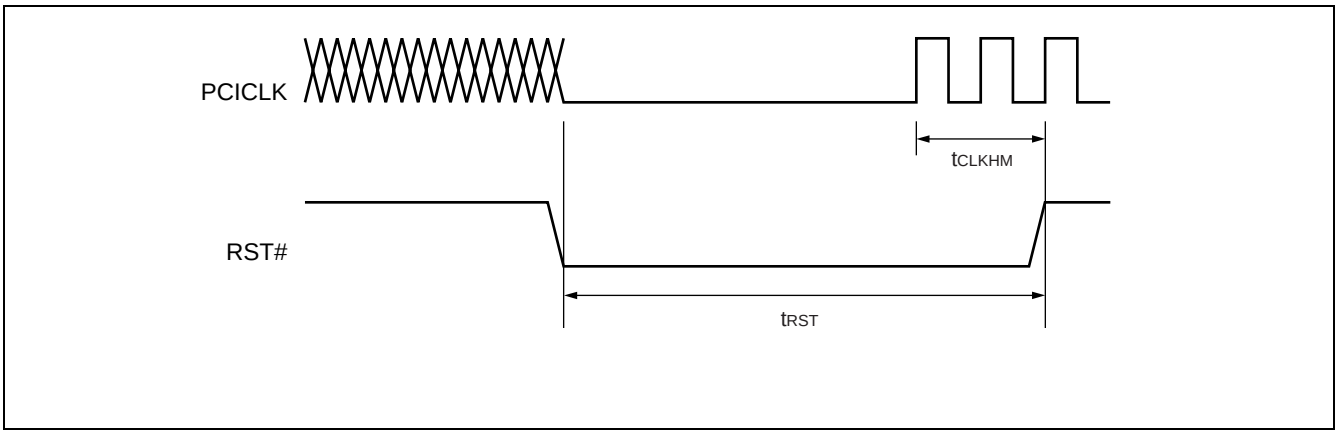
(3) PCICLK

Parameter	Symbol	Condition	Value		Unit
			Min.	Max.	
Clock frequency	f_C	—	—	33	MHz
Clock cycle time	t_{CLF}	—	30	∞	ns
Clock pulse width	t_{CLCH}, t_{CLCL}	—	11	—	ns
Clock rise/fall time	t_{CR}, t_{CF}	—	—	6	ns
Slew rate	—	—	1	4	V/ns



(4) RST#

Parameter	Symbol	Condition	Value		Unit
			Min.	Max.	
Hold time after power stabilization	t_{RST}	—	0	—	PCI CLK
Hold time after clock stabilization	t_{CLKHM}	—	6	—	PCI CLK



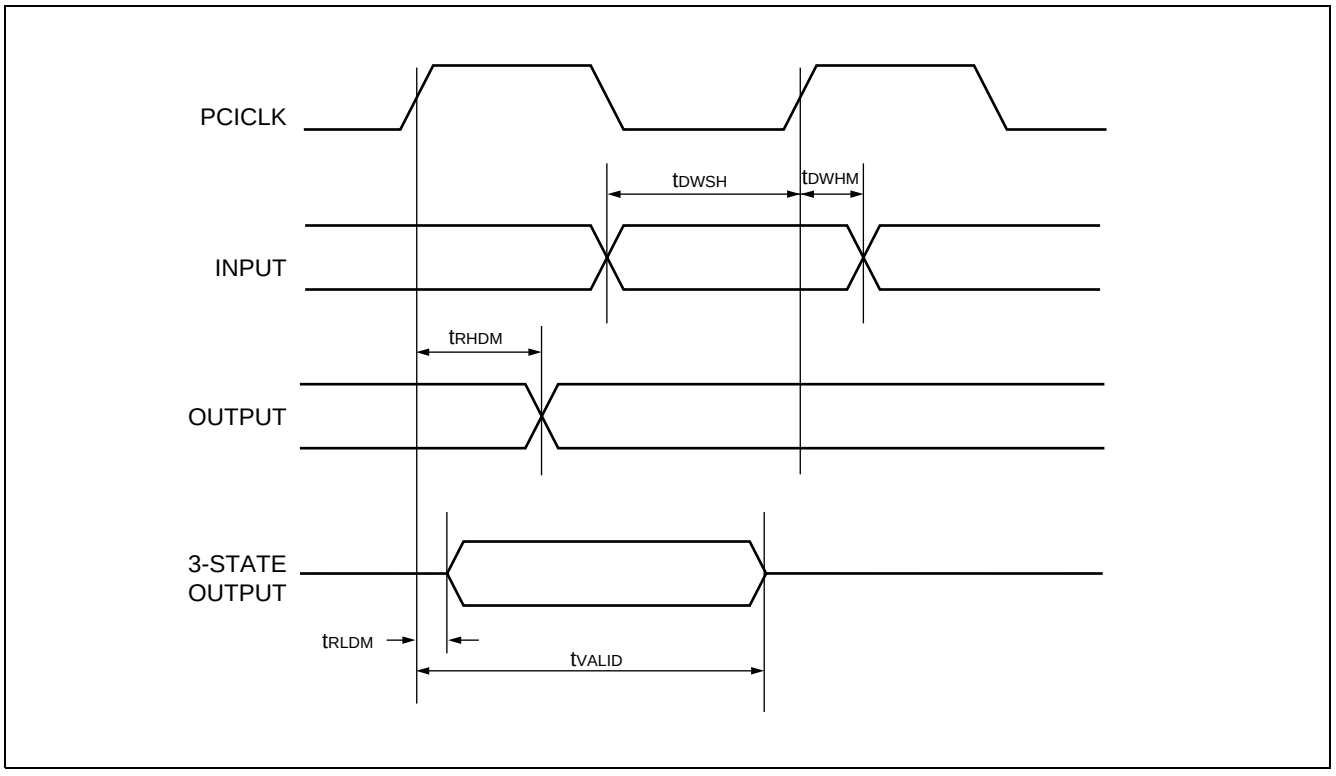
(5) Transceiver

Parameter	Symbol	Condition	Value		Unit
			Min.	Max.	
Transceiver rise time	T_R	10% to 90%	—	1.2	ns
Transceiver fall time	T_F	90% to 10%	—	1.2	ns
Sending output jitter	—	—	—	±0.15	ns
Sending output skew*	—	—	—	±0.10	ns

* : Skew between TPA pin and TPB pin.

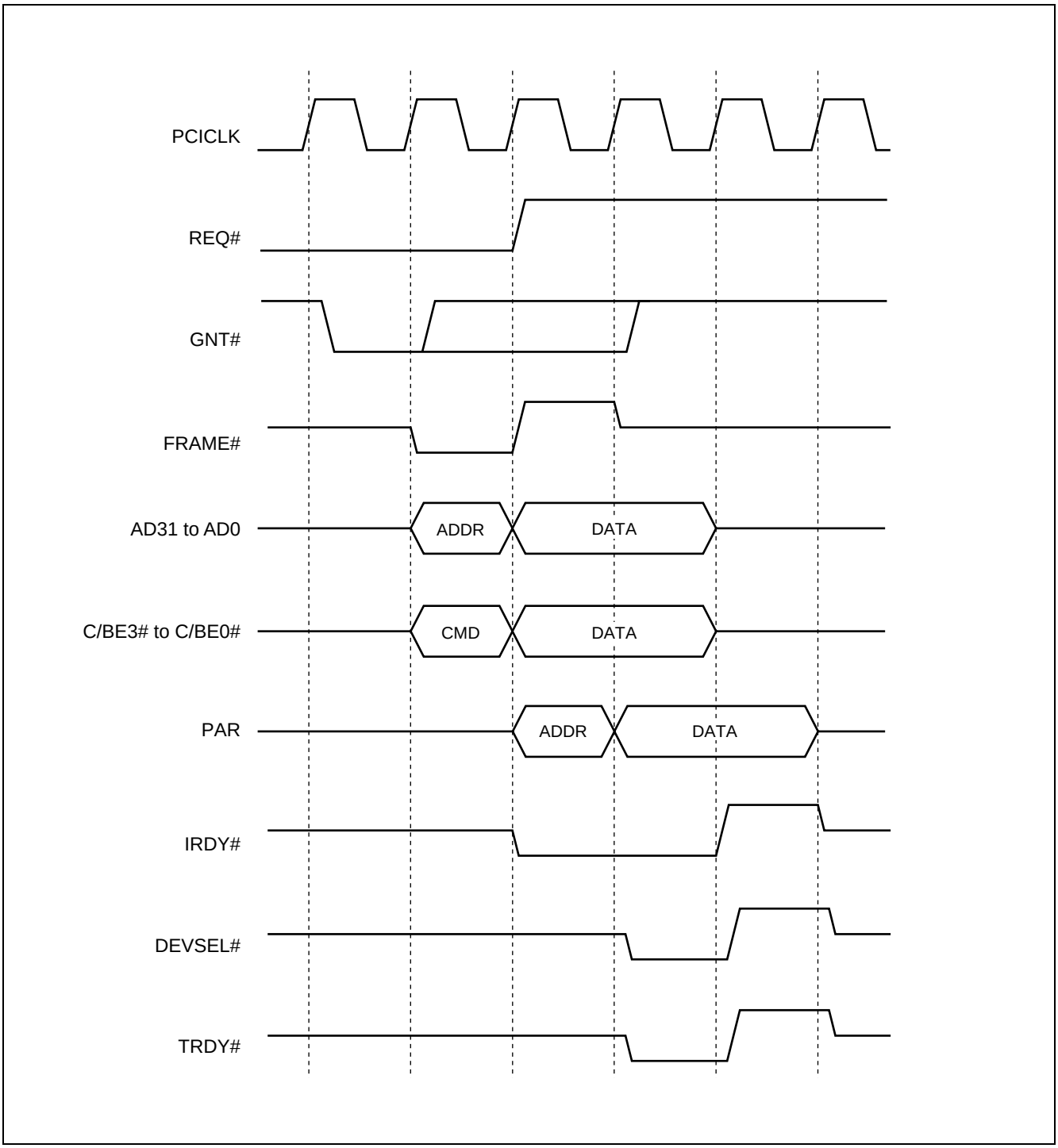
(6) PCI Bus

Parameter	Symbol	Condition	Value		Unit
			Min.	Max.	
Input data setup time	t_{DWSH}	—	7 (10) *	—	ns
Input data hold time	t_{DWHM}	—	1 (1) *	—	ns
Data output delay time	t_{RHDM}	—	2 (2) *	11 (12) *	ns
Output data verification time	t_{RLDM}	—	2	—	ns
Output data valid time	t_{VALID}	—	—	28	ns

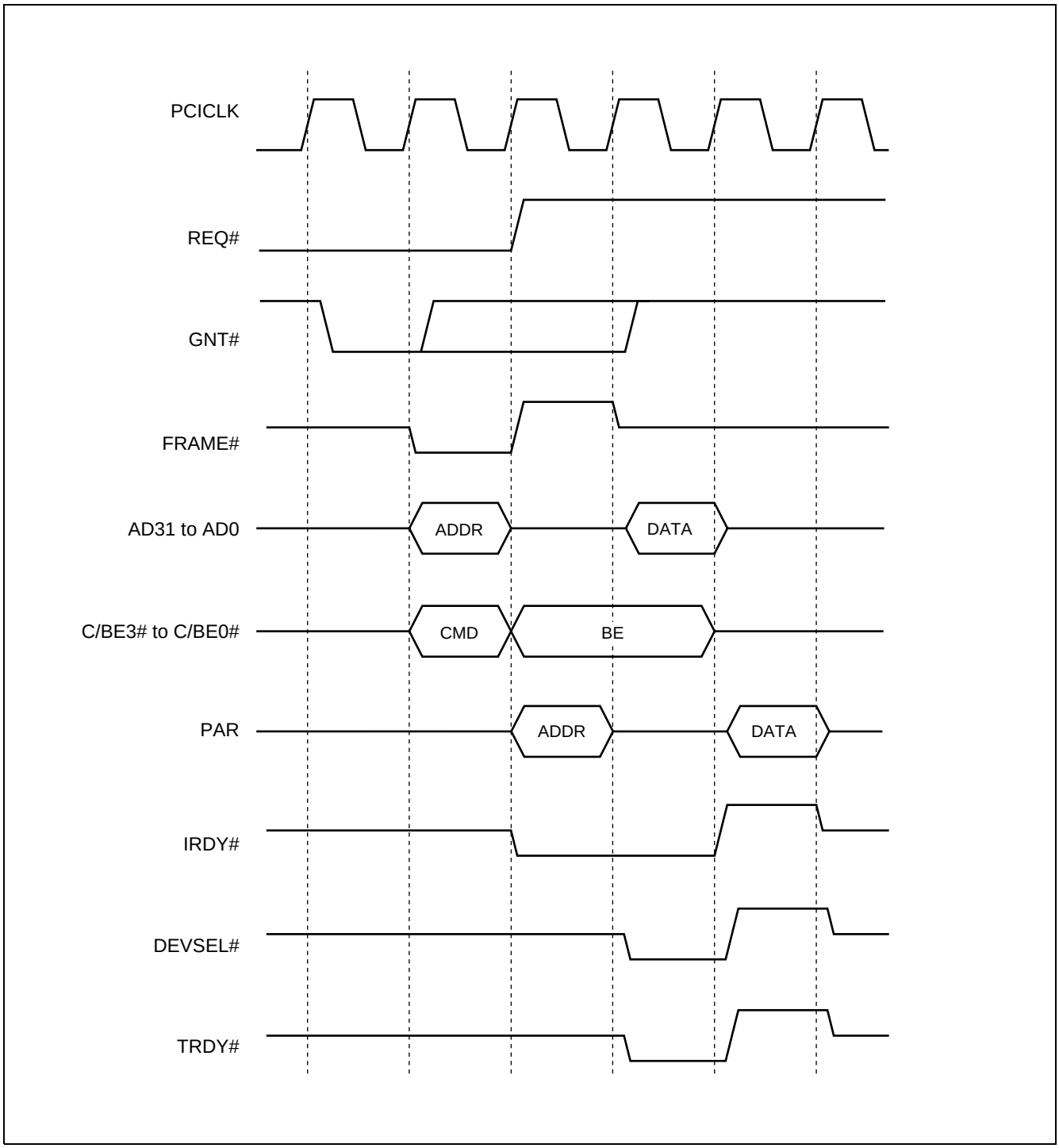


* : Between REQ# and GNT# pins.

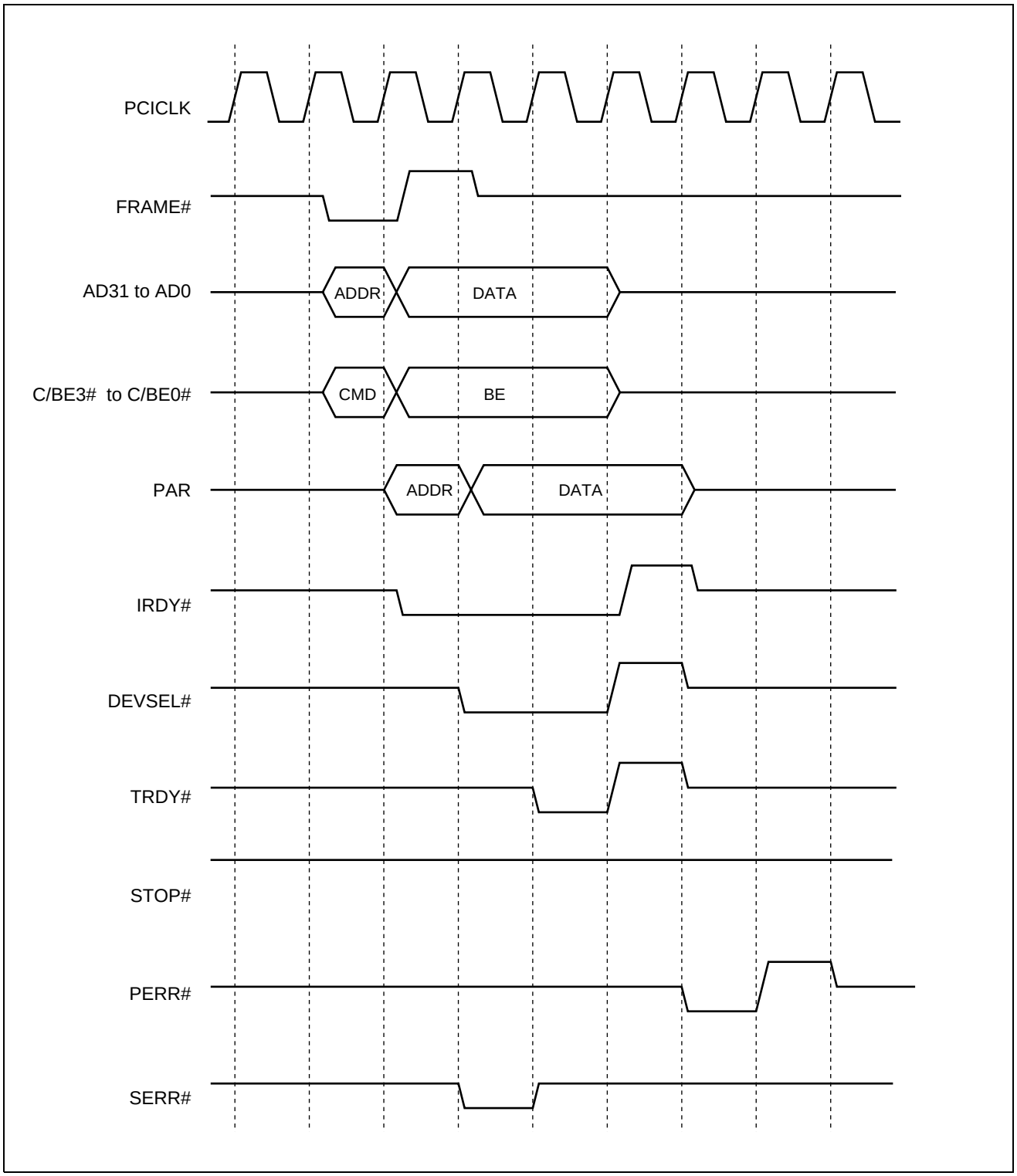
• **Bus Master Write Operation**



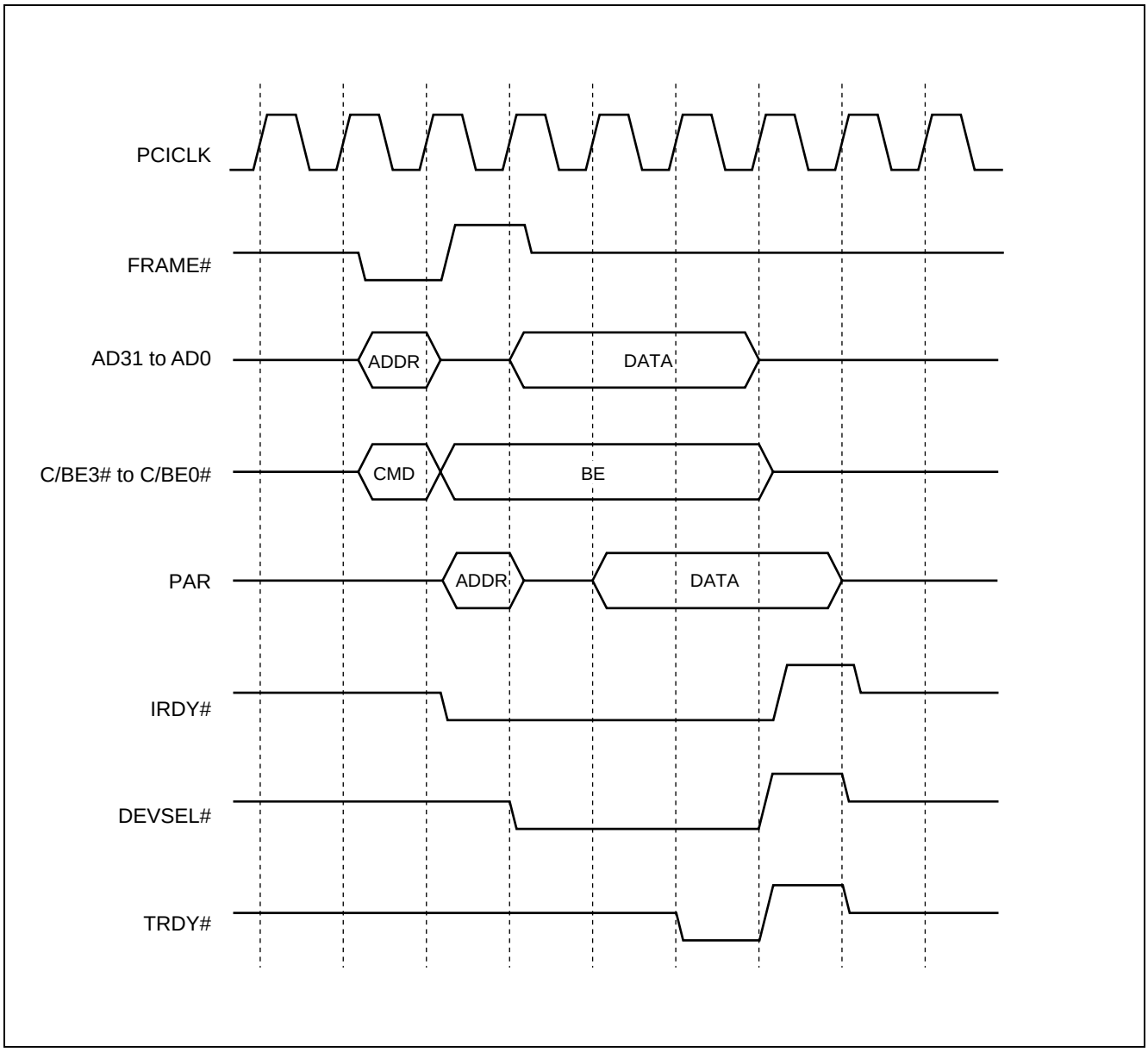
• **Bus Master Read Operation**



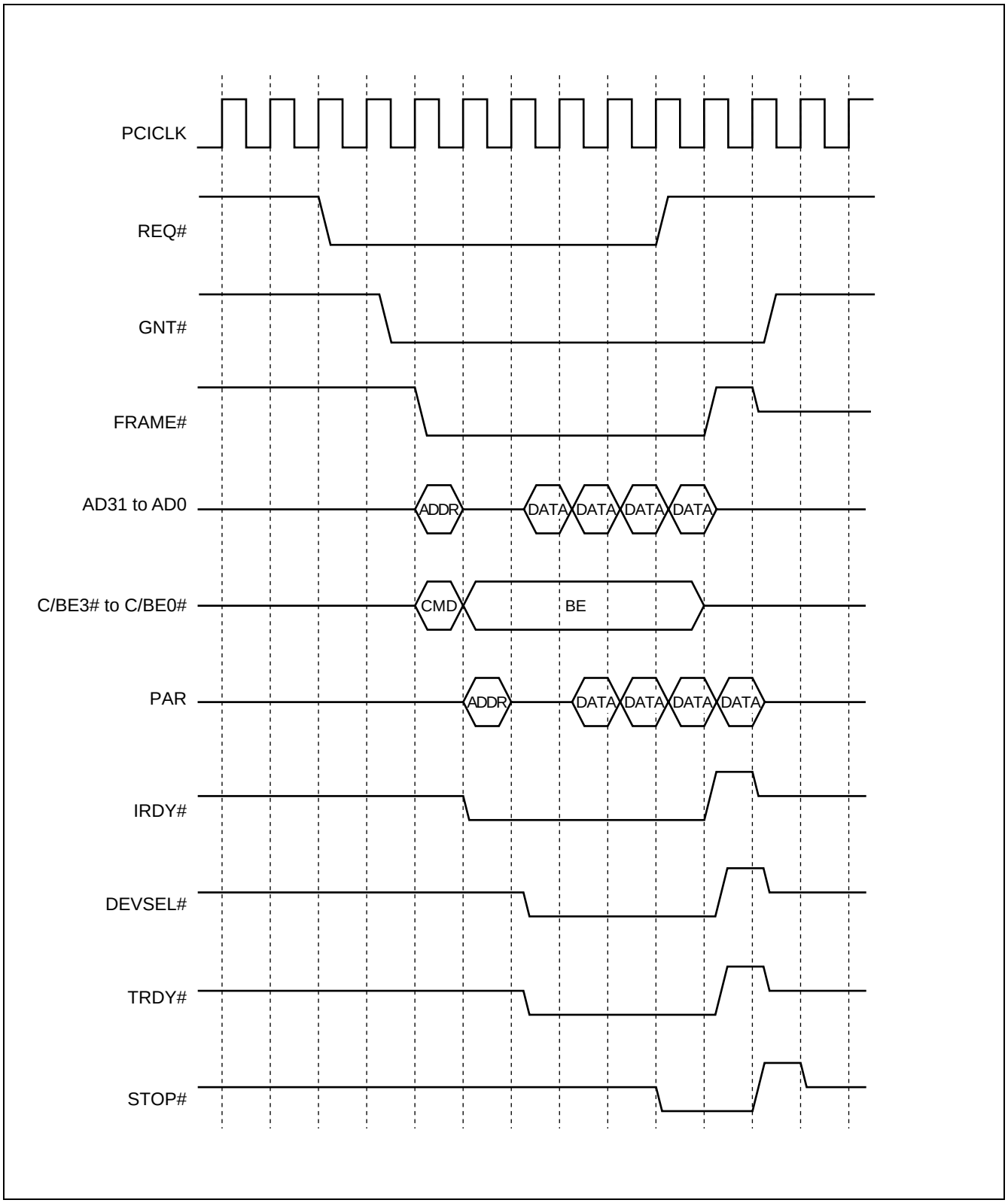
• **Slave Write Processing**



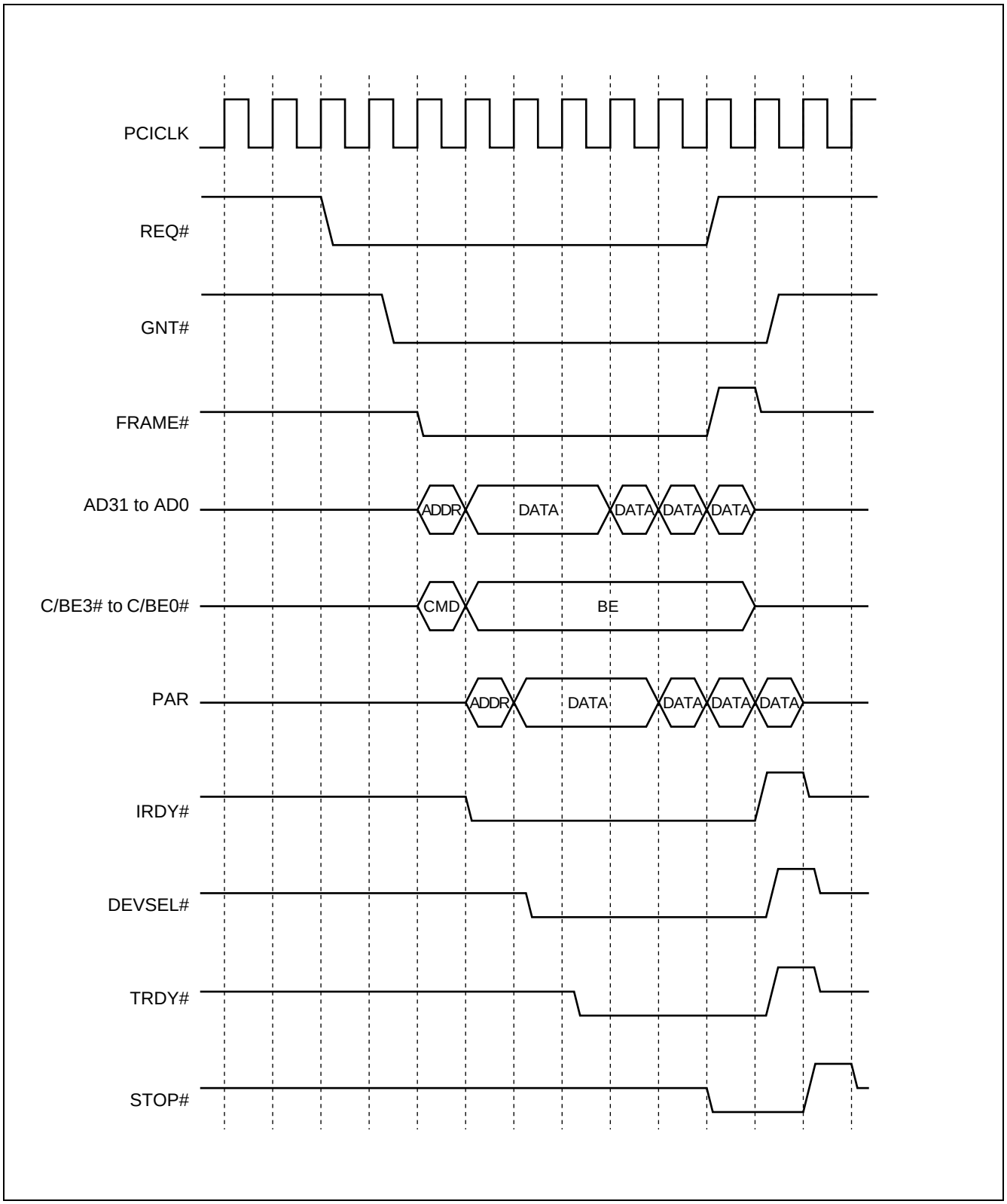
• **Slave Read Processing**



• **Bus Master Burst Read Processing**



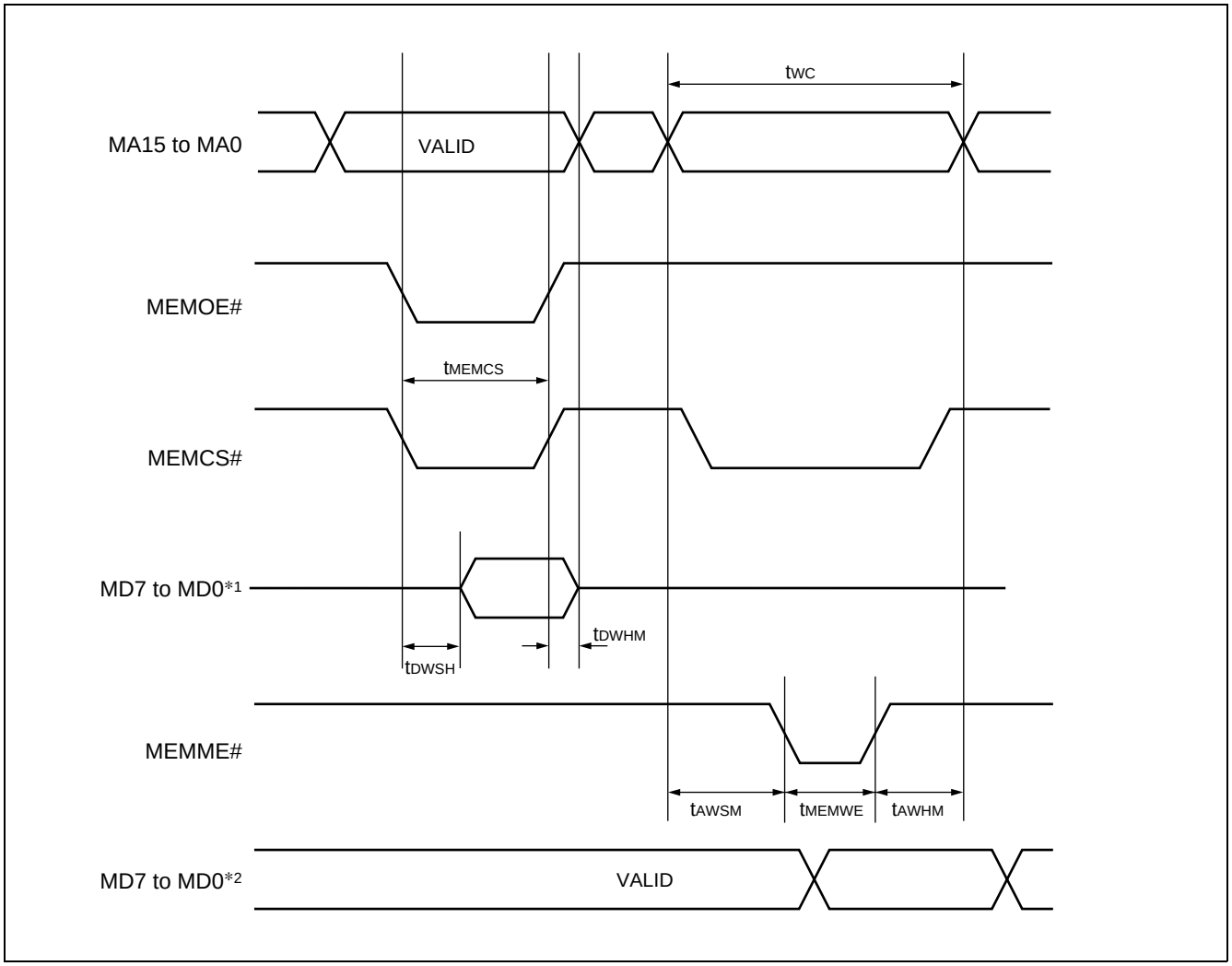
• **Bus Master Burst Write Processing**



(7) Memory Interface

• **EPROM**

Parameter	Symbol	Condition	Value		Unit
			Min.	Max.	
MEMCS# signal “L” level output time	t_{MEMCS}	—	—	50	ns
Input data definition time	t_{DWSH}	—	—	10	ns
Input data hold time	t_{DWHM}	—	—	10	ns
Write cycle time	t_{WC}	—	—	50	ns
Address setup time	t_{AWSM}	—	13	—	ns
Address hold time	t_{AWHM}	—	15	—	ns
MEMWE# signal pulse width	t_{MEMWE}	—	25	—	ns

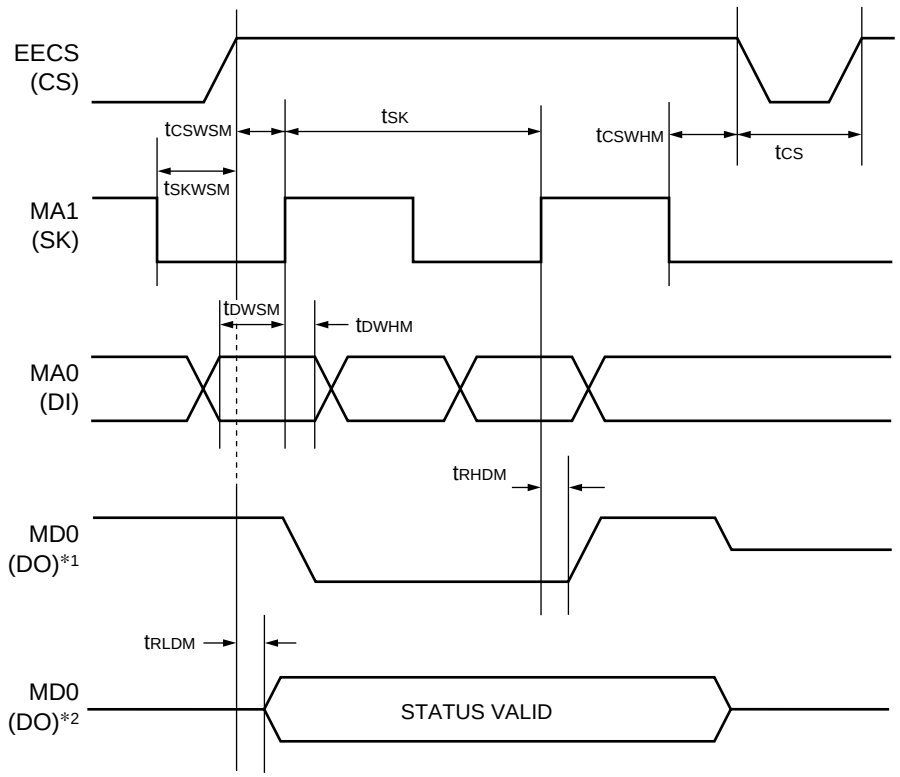


*1 : For EPROM read processing.

*2 : For EPROM write processing.

• **EEPROM**

Parameter	Symbol	Condition	Value		Unit
			Min.	Max.	
Clock cycle time	t_{SK}	—	1000	—	ns
CS signal setup time	t_{CSWSM}	—	50	—	ns
SK signal setup time	t_{SKWSM}	—	50	—	ns
CS signal “L” level output time	t_{CS}	—	250	—	ns
Data output hold time (for DO)	t_{RHDM}	—	20	—	ns
Input data setup time (for DI)	t_{DWSM}	—	100	—	ns
Input data hold time (DI)	t_{DWHM}	—	20	—	ns
CS signal hold time	t_{CSWHM}	—	0	—	ns
Status output definition time	t_{RLDM}	—	500	—	ns

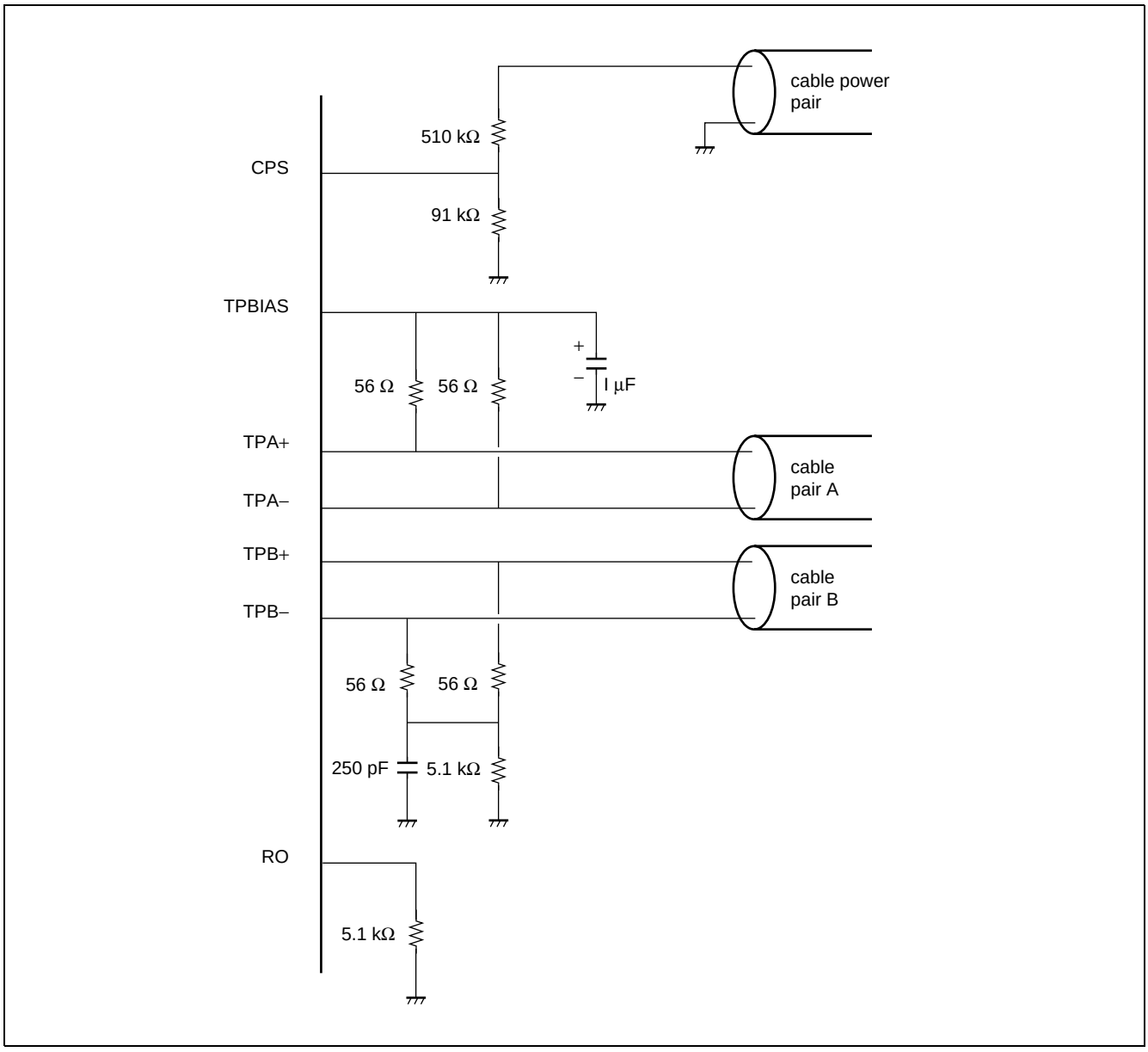


*1 : For EPROM read processing.

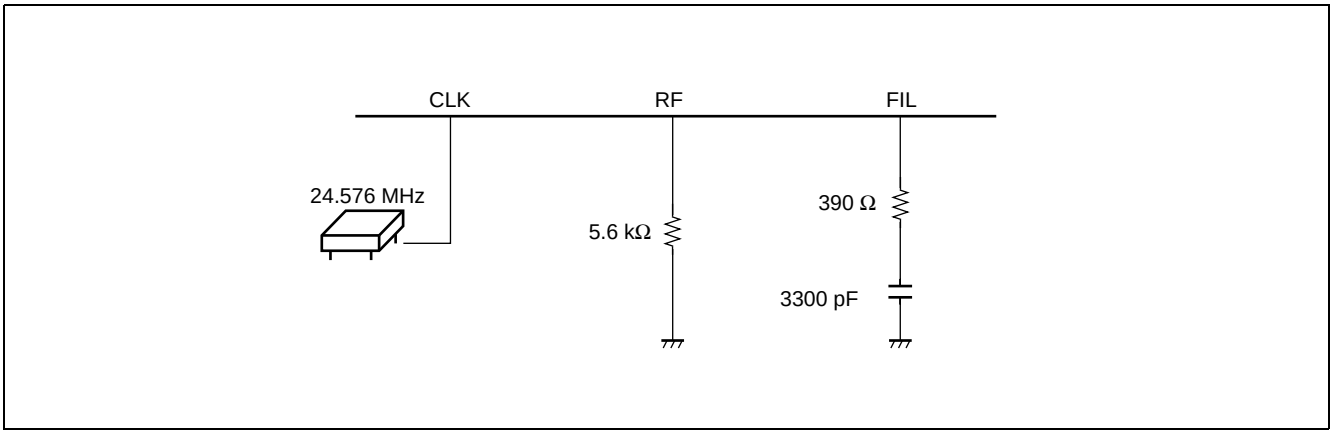
*2 : For EPROM write processing.

■ COMPONENT CONNECTION DIAGRAM

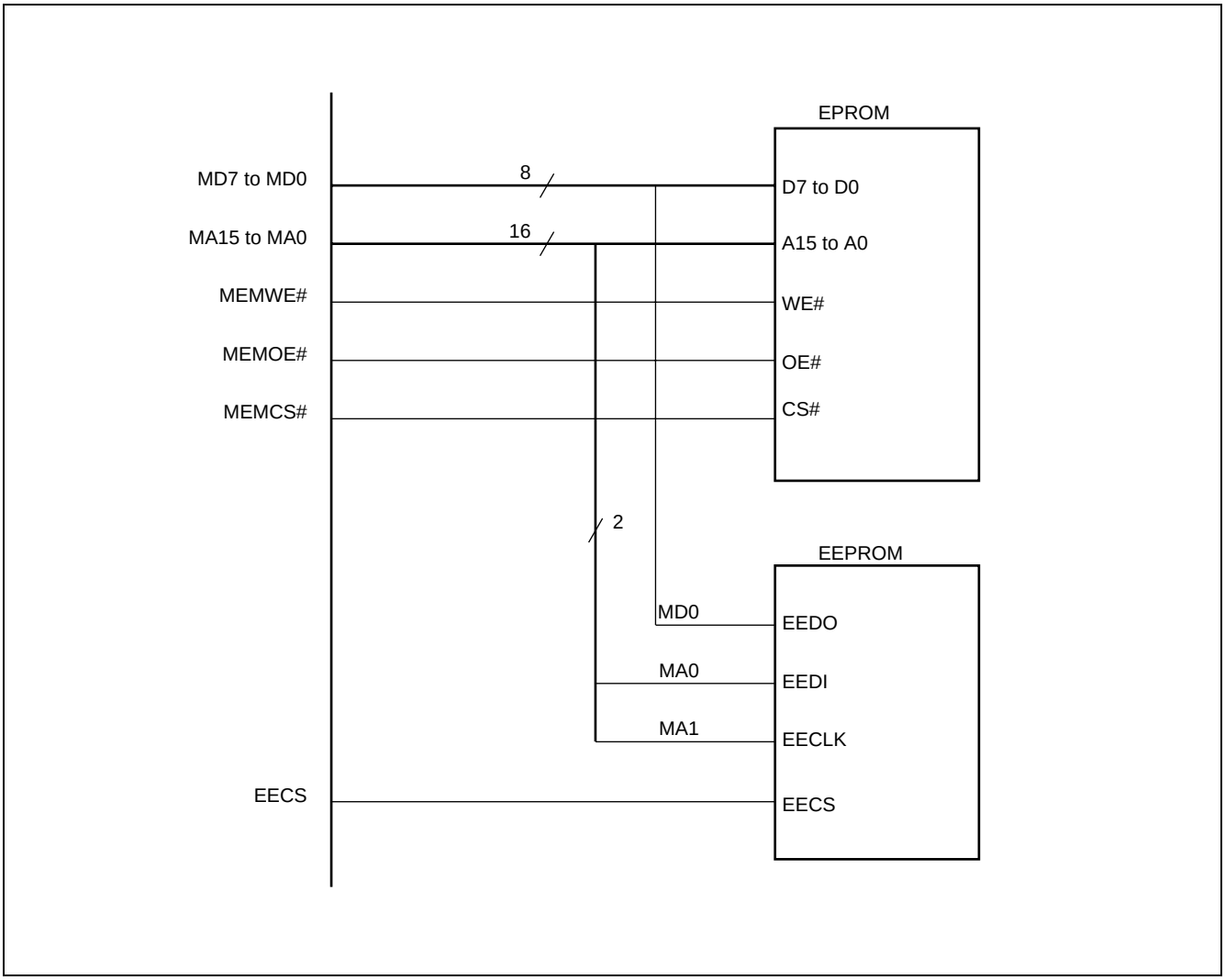
1. 1394 Port



2. Filter Circuit



3. Memory Interface

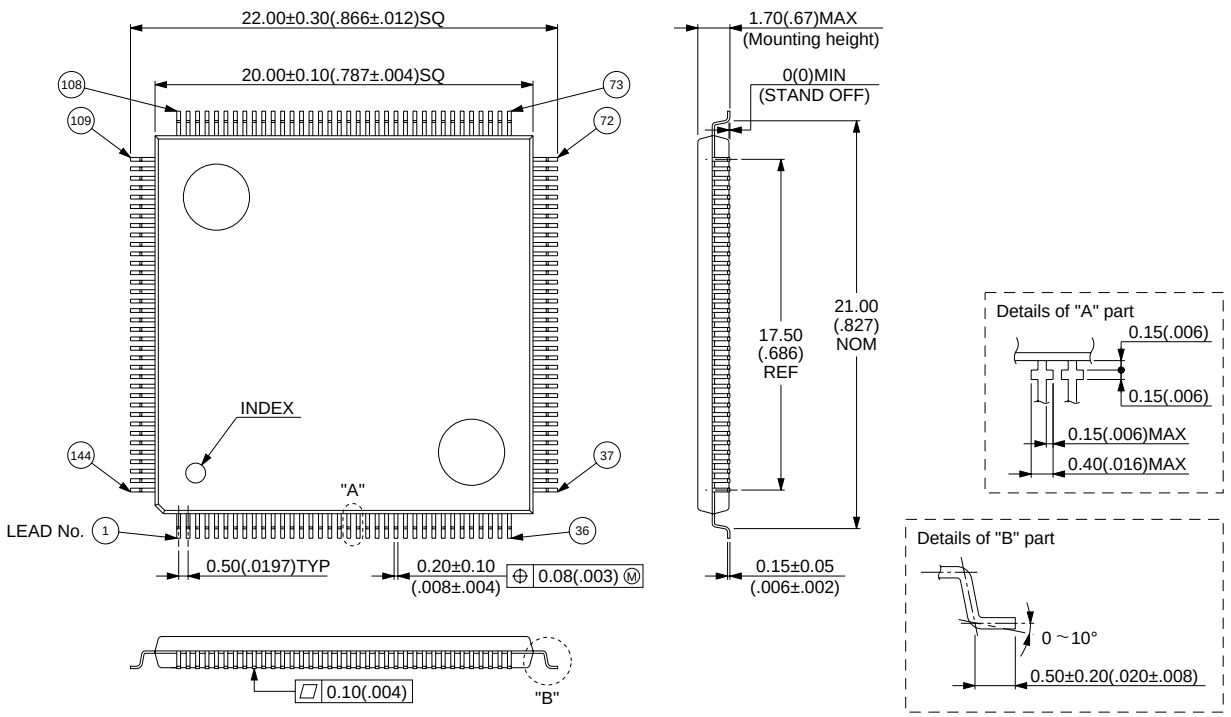


■ ORDERING INFORMATION

Part number	Package	Remark
MB86613PFV	144-pin Plastic LQFP (FPT-144P-M08)	
MB86613PBT	176-pin Plastic FBGA (BGA-176P-M02)	

■ PACKAGE DIMENSIONS

144-pin plastic LQFP
(FPT-144P-M08)



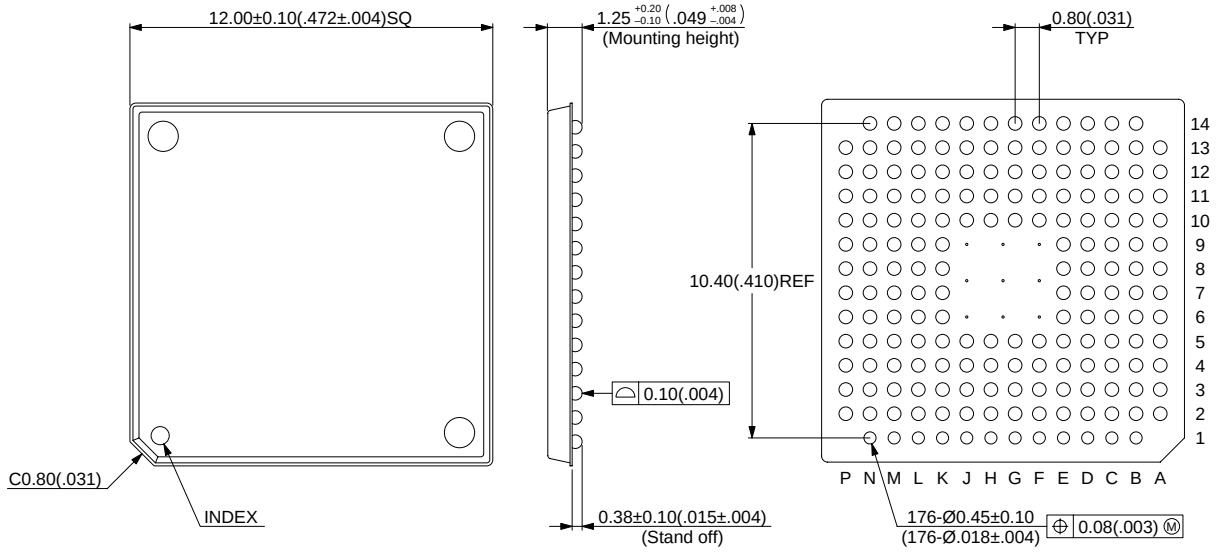
Dimensions in mm (inches)

(Continued)

(Continued)

176-pin plastic FBGA
(BGA-176P-M02)

Note : The actual shape of corners may differ from the dimension.



Dimensions in mm (inches)

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F0004

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